ENHANCED MODEL OF CONDUCTIVE FILAMENT-BASED MEMRISTOR AND ITS APPLICATION ON SOME CIRCUITS

By

Amr Mahmoud Hassan Mahmoud

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfilment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Physical Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2015

ENHANCED MODEL OF CONDUCTIVE FILAMENT-BASED MEMRISTOR AND ITS APPLICATION ON SOME CIRCUITS

By

Amr Mahmoud Hassan Mahmoud

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfilment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Physical Engineering

Under the Supervision of

Prof. Nadia H. Rafat
Professor
Engineering Mathematics and Physics Department
Faculty of Engineering, Cairo University

Prof. Hossam A. H. Fahmy
Professor
Electronics and Communications Engineering Department
Faculty of Engineering, Cairo University

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2015

ENHANCED MODEL OF CONDUCTIVE FILAMENT-BASED MEMRISTOR AND ITS APPLICATION ON SOME CIRCUITS

By

Amr Mahmoud Hassan Mahmoud

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfilment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Physical Engineering

Approved by the Examining Committee:

Prof. Nadia H. Rafat, Thesis Main Advisor

Prof. Hossam A. H. Fahmy, Thesis Advisor

Prof. Alaa K. Abdelmageed, Internal Examiner

Prof. Khaled A. Shehata, External Examiner
(Engineering College, Arab Academy for Science & Technology)

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
2015

Engineer's Name:	Amr Mahmoud Hassan Mahmoud
Date of Birth:	02/03/1989
Nationality:	Egyptian
E-mail:	a.m.hassan@ieee.org
Phone:	01001224334
Address:	Engineering Mathematics and Physics Department, Cairo University, Giza 12613, Egypt
Registration Date:	13/03/2012
Awarding Date:	..../..../....
Degree:	Master of Science
Department:	Engineering Mathematics and Physics

Supervisors:

Prof. Nadia H. Rafat
Prof. Hossam A. H. Fahmy

Examiners:

Prof. Nadia H. Rafat	(Thesis Main Advisor)
Prof. Hossam A. H. Fahmy	(Thesis Advisor)
Prof. Alaa K. Abdelmageed	(Internal Examiner)
Prof. Khaled A. Shehata	(External Examiner) (Engineering College, Arab Academy for Science & Technology)

Title of Thesis:

Enhanced Model of Conductive Filament-Based Memristor and its application on some Circuits

Key Words:
Memristors; Filament-based memristors; Trapezoidal barrier; Tunneling; Simmons tunneling model for dissimilar electrodes; Airy function; SPICE model.

Summary:
Memristors are considered as the fourth passive circuit element and they exhibit very promising features. This thesis aims to introduce a new approach to improve the current modeling of memristors by taking into account trapezoidal electron tunneling barrier. The research is conducted in two stages: device stage, and circuits stage. In the device stage, the proposed approach is applied and solved by two different methods. The two derived models are verified against published experimental data and the accuracy is improved significantly. In the circuits stage, the model is used to simulate some circuit applications by using Candence Virtuoso.

Acknowledgments

In the name of Allah the most merciful the most gracious; all thanks to Allah the Lord of the Heavens and Earth and peace be upon Mohamed and his companions.

First and foremost I would like to express my indebtedness and gratefulness to my academic advisors: Prof. Nadia H. Rafat and Dr. Hossam A. H. Fahmy. It has been a pleasure to work with them and learn from such extraordinary advisors. They have always made themselves available for help and advice with their boundless enthusiasm and positive thinking.

I am indebted to Dr. Nadia for the countless hours that she spent with me on discussing problems and making suggestions, and for many discussions that made my research possible. She showed great patience during my first period of research, which encouraged me to keep moving forward. In the past three years, she taught me invaluable skills such as communicating ideas effectively and logically, critical thinking, documentation and reporting.

I am also indebted to Dr. Hossam for his guidance and mentoring over the past three years. He was always pushing me forward and constantly provided me with new research ideas. His insight, enthusiasm and invaluable advises - not only in scientific research, but also in other aspects of life - have great impacts on me, personally and scientifically.

Special thanks to Prof. Ahmed Alaa Abouelsaood, Prof. Salah El Nahwy, Prof. Nadia Rafat, and Dr. Essam El Karamany for teaching such a great graduate courses at Cairo University. I benefited from the breadth of the courses that gave me comprehensive exposure to the core areas of Engineering Physics.

Special thanks to Mohamed El Neanaei and Ahmed El Sheikh for the very useful discussions that we had on some points of my research.

Thanks to my colleagues studying abroad: Hatem Osman, Ahmed Adel, Mamdouh Hassan, and Ahmed Hussein for helping to get the JAP and IOP research papers.

Special thanks to my colleagues at Cairo University; Mohamed Zaghloul, Tarek Ameen, Eslam Sayed, Islam Hashem, Ahmed Abdo, Mahmoud Taha, Mohamed Yehia, Ahmed Ibrahim, Mostafa Radwan, Ahmed Reda, and Hussein Mohamed for their continuous support and the great times we had together throughout my work as a teaching assistant at the Department of Engineering Mathematics and Physics at Cairo University. They made the graduate school a very enjoyable experience.

Last but not least, I am most grateful to my parents for their patience and love. It is a dream that come true to achieve this degree, which I share with them. Without them this work would never have come into existence (literally).

Amr M. H. Mahmoud

To my family and all my friends

Table of Contents

List of Figures

List of Symbols

$\mu_{\mathbf{v}}$	Aaverage charge mobility.
ε	Dielectric constant.
ε_o	Permittivity of free space.
φ	Potential barrier height.
Ψ	Wave function.
$\boldsymbol{\hbar}$	Reduced Planck's constant.
$\boldsymbol{a_{\mathbf{fb}}}$	Limiting width in forward bias.
$\boldsymbol{a_{\mathbf{rb}}}$	Limiting width in reverse bias.
$\boldsymbol{Ai}$	Airy function of the first kind.
$\boldsymbol{Bi}$	Airy function of the second kind.
$\boldsymbol{b}$	Fitting parameter.
$\boldsymbol{D}$	Memristor device length.
$\boldsymbol{E_{\mathbf{f}}}$	Fermi Level.
$\boldsymbol{e}$	Electron Charge.
$\boldsymbol{f_{\mathbf{c}}}$	Critical frequency.
$\boldsymbol{f_{\mathbf{fb}}}$	Gain factor in forward bias.
$\boldsymbol{f_{\mathbf{rb}}}$	Gain factor in reverse bias.
$\boldsymbol{h}$	Planck's constant.
$\boldsymbol{i_{\mathbf{fb}}}$	Threshold current in forward bias.
$\boldsymbol{i_{\mathbf{rb}}}$	Threshold current in reverse bias.
$\boldsymbol{J}$	Tunneling current density.
$\boldsymbol{k}$	Wave vector of the electron.
$\boldsymbol{m}$	Mass of electrons.

$T(E_x)$	Tunneling probability.
v_g	Voltage across tunneling barrier.
$w(t)$	Internal state variable.
w_c	Fitting parameter.
Ag	Silver.
Al	Aluminum.
Au	Gold.
Cd	Cadmium.
HfO_x	Hafnium x-oxide.
L	Memristor device thickness.
MnO_x	Manganese x-oxide.
Nb	Niobium.
Nb_2O_5	Niobium pentoxide.
Ni	Nickel.
NiO	Nickel oxide.
Pt	Platinum.
Ta	Tantalum.
Ta_2O_5	Tantalum pentoxide.
Ti	Titanium.
TiO_{2+x}	Excess oxygen atoms titanium dioxide.
TiO_{2-x}	Reduced titanium dioxide.
TiO_2	Titanium dioxide.
TiO_x	Titanium x-oxide.
W	Tungsten.

List of Acronyms

3D-IC	3 Dimensions Integrated Circuits.
AFM	Atomic Force Microscopy.
ChG	Chalcogenide Glass.
CMOS	Complementary Metal Oxide Semiconductor.
DRAM	Dynamic Random Access Memory.
FinFET	Fin Field Effect Transistor.
FPGA	Field-Programmable Gate Array.
ITRS	International Technology Roadmap of Semiconductors.
Memristor	Memory resistor.
MIM	Metal Insulator Metal.
MRLO	Memristor-Based Reactance-less Oscillators.
ReRAM	Resistive Random Access Memory.
SCM	Storage Class Memory.
STT-MRAM	Spin-Transfer Torque Magneto-resistive Random Access Memory.
WKB	Wentzel-Kramers-Brillouin.

Abstract

By approaching the limit of Moore's law, scientists are investigating new devices and structures that would allow us to go "beyond Moore's Law". One of the very promising devices that is being investigated nowadays is the memristor. Memristors (short for memory-resistors) are considered as the fourth passive circuit element, along with resistors, capacitors and inductors. They were first postulated by Leon chua in 1971 and first realized by HP labs in 2008. They exhibit very attractive features such as: hysteresis in the I-V characteristics curve, few nanometers in size, and the ability to retain their last resistance value when the bias is off (hence, the name memristor).

In this research, filament-based memristors are investigated and their current models are studied to improve them. We introduce a new approach to improve the current modeling of memristors by taking into account trapezoidal electron tunneling barrier. The research is conducted in two stages: device stage, and circuits stage.

In the device stage, the proposed approach is applied and solved by two different techniques. The first one uses the Airy function, while the second one utilizes the well known Simmons model for dissimilar electrodes. Then, the results of the two techniques are verified against published experimental data to prove their validity, and the accuracy is improved significantly. Moreover, we did a parametric study, using our model, on the dependence of the memristor I-V characteristics on different parameters such as the tunneling barrier height, and the shape, frequency and magnitude of the input signal. From each of these studies a result is concluded that would help the circuit designers.

In the circuits stage, SPICE and Verilog-A codes were implemented based on Simmons model for dissimilar electrodes. These models were used to simulate some circuit applications by using Cadence Virtuoso and their results are discussed.

Chapter 1

Introduction

Throughout history, new emerging physical devices were always the key to advancing from one technology node to another. Perhaps one of the greatest evidences of this fact is the transistor. The realization of the first transistor in 1947, by AT&T's Bell Labs, led to a new era in the electronic industry. Accurate modeling of transistors and continuous dimensions shrinking were the reasons why integrated circuits industry evolved significantly in the last 50 years. Not only this evolution yielded a huge increase in the number of processing and memory units per chip area, but also it provided great improvements in terms of speed and power consumption, and reduced the whole cost of the featured device. Gorden Moore predicted this evolution and encapsulated his prediction in what is known to us now as "Moore's Law". He stated that the number of transistors per square inch on integrated circuits would be doubled every two years since the integrated circuits were invented [1]. However, what actually happened was slightly different than what Moore predicted, since the number of transistors doubled every 18 months.

Unfortunately, Moore's law cannot hold forever. In 2006 [2], Thompson *et al.* discussed the issue of transistors hitting physical boundaries due to quantum effects and miniaturization problems. Additionally, power dissipation related problems arise nowadays in the field of computing [3]. Moreover, the enhancing rate of processors speed exceeds the enhancing rate of DRAM memories speed, thus holding back the overall performance of CPUs. This problem is widely known as the Memory Wall [4]. All these crippling issues have to be overcome by great investments in research to find out new devices and structures, that would allow us to keep the field of integrated circuits and computing evolutionary as it is now.

Scientists are working hard to explore different materials and approaches to overcome the issues mentioned above. One of the very promising solutions to the scaling problem of transistors is the new emerging devices such as spintronic devices and carbon nanotubes. Another practical solution is to blend between new technologies and standard CMOS. The later one is anticipated to keep the current growth rate over the coming couple of decades. Three dimensional integrated circuits, such as FinFETs and 3D-ICs [5], are considered as examples of the later solution and are now available in the market. Moreover, memristive devices, such as memristors (short for memory-resistors), are considered a new technology which will unleash new potentials when combined with existing CMOS technology. These devices will be the major focus of this thesis.

1.1 Memristors

1.1.1 Historical Background

In 1971 [6], Leon Chua first postulated the existence of memristor and later generalized its theory in 1976 [7]. According to his observations to the relations that govern the three passive circuit elements, namely resistor, inductor, and capacitor. Chua figured out that, for symmetry reasons, there has to be a fourth passive circuit element, he named it memristor.

To elaborate more, we have four fundamental circuit quantities, which are the electric charge Q, the current I, the magnetic flux Φ, and the voltage V. There are six possible relationships that connect these quantities together as shown in Fig. 1.1. The current I is the derivative with respect to time of the charge Q, and the voltage V is the derivative with respect to time of the magnetic flux Φ. The three known passive two-port circuit elements connect these quantities as follows: resistors relate current to voltage via Ohm's Law ($dV = R.dI$), inductors relate magnetic flux to current ($d\Phi = L.dI$), and finally capacitors relate voltage to charge ($dQ = C.dV$).

Chua hypothesized, for symmetry and completeness, a new passive two-port circuit element (memristor) which relates magnetic flux and charge ($d\Phi = M.dQ$). In addition, Chua proved that none of the three passive circuit elements could mimic the behavior of memristors. He also added that it would require a circuit with about 25 transistors to duplicate the hypothesized element [6].

It can be shown that [6]:

$$V(t) = M(Q(t)).I(t) \quad (1.1)$$

$$M(Q(t)) \equiv d\Phi(Q)/dQ \quad (1.2)$$

where M(Q(t)) is called the memristance and its unit is the same as that of resistance. It can be shown from eq. 1.2 that memristance M(Q(t)) is function of the charge Q or, in other words, the time integral of the current I flowing through the device. Thus, memristor can be thought of as a two-terminal passive device whose resistance is variable according to the current I passing through it. The memristance value is kept unchanged when the current is off (the integration of zero current would result in a constant charge, thus constant memristance). Thus, the memristor has a memory trait (hence the name memristor) which appears in retaining the last value of its resistance before the power is off.

Later in 1976, Chua *et al.* generalized the memristor definition to memristive devices [7]. Memristive devices are also two-port devices with varying memristance. The difference between memristive devices and memristors comes from the way the memristance changes. The memristance of memristive devices is function of an internal state $w \in R^n$ which, in turn, is a function of the past current that passes through the device. However, the memristance of memristors is a direct function of the magnetic flux or charge. The equations representing these nonlinear dynamical memristive devices are [7]:

$$V(t) = \mathcal{R}(w, I).I(t) \quad (1.3)$$

$$\frac{dw}{dt} = f(w, I) \quad (1.4)$$

where $\mathcal{R}(w, I)$ is the generalized resistance of the device, and w, as mentioned above, is an internal state. *f(w,I)* is a function of w and the current I.

1.1.2 Memristors Realization

Since 1976, memristive devices were just theoretical devices without any practical realization. It's not until 2008 when HP Labs made the connection between the hypothesized memristor and TiO_2-based devices [8].

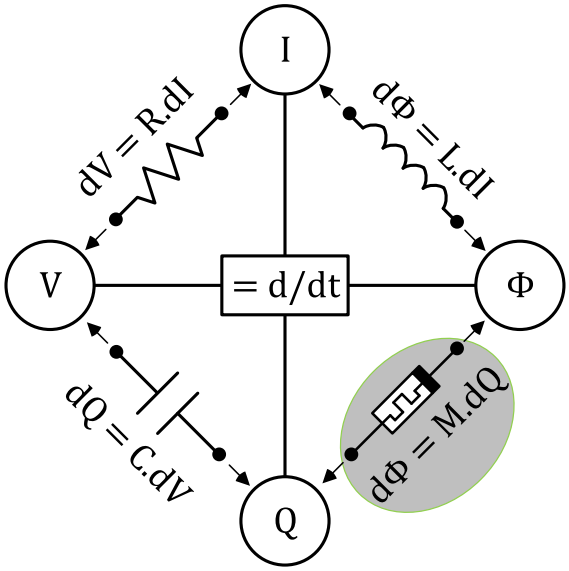


Figure 1.1: The four fundamental circuit quantities, namely charge Q, current I, magnetic flux Φ, and voltage V, along with the six relationships that connect them. The grey relation shows the missing circuit element, the memristor.

The structure of the device fabricated is shown in Fig. 1.2, which is composed of an undoped TiO_2 layer and another doped TiO_{2-x}layer (where the doping here represents the oxygen vacancies) sandwiched between two platinum electrodes. The internal state variable, *w*, in this device was taken as the width of the undoped TiO_2 layer. When a voltage signal is applied across the device, the oxygen vacancies moves in the same direction of the electric field, which in turn changes the doped layer thickness. This causes the resistance of the device to be changed. Upon removing the voltage signal, oxygen vacancies don't revert back to their original position due to their very low mobility [8].

The representation of eq. (1.3) and (1.4) are [8]:

$$V(t) = \left(R_{on}\frac{w(t)}{D} - R_{off}\left(1 - \frac{w(t)}{D}\right)\right).I(t) \tag{1.5}$$

$$\frac{dw}{dt} = \mu_v \frac{R_{on}}{D}.I(t) \tag{1.6}$$

where R_{off} is the resistance when $w(t) = 0$, and R_{on} is the resistance when $w(t) = D$. The internal state variable w(t) has the limits of $0 < w(t) < D$. μ_v is the average mobility of the dopants.

Since that discovery, memristor has gained the attention of different researches worldwide. Many universities and research entities around the world had adopted the

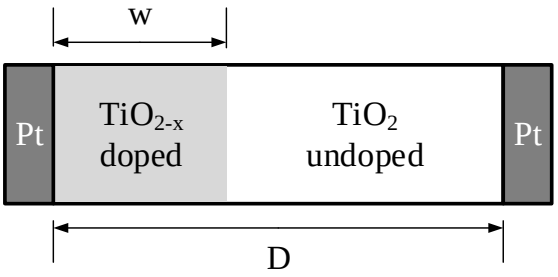


Figure 1.2: Memristor structure suggested by HP. It has two regions: doped and undoped. The total resistance is the sum of both regions' resistances.

memristor as a new emerging device and conducted countless experiments. A tremendous amount of articles have been published since 2008 and still going on. In 2009, Di Ventra and Chua expanded the definition of memristive systems to accommodate for meminductors and memcapacitors. Like memristor, the inductance and capacitance of meminductors and memcapacitors depend on the history of the applied signal and the state of these devices [9, 10].

1.1.3 Memristor Properties and Types

The most appealing trait of memristors is their ability to preserve their last resistance after the power is off. Thus, it is very likely that these devices will be used as memory elements to store data, represented by different values of resistances. Fortunately, memristors have other characteristics that will make them more attractive to different researchers and companies worldwide. Usually, memristors are fabricated as oxides sandwiched between two conducting electrodes (Metal-Insualtor-Metal, or MIM). They have a relatively small size (typically few nanometers), high endurance, and relatively short switching time (ranging from fractions of nanoseconds to few nanoseconds). In addition, the I-V characteristics of memristors shows a pinched hysteresis loop as shown in Fig. 1.3, where the area enclosed by the loop varies with the frequency of the applied signal. As the frequency increases, the hysteresis effect vanishes and the memristor approaches the behavior of a resistor.

Besides using TiO_2 as the oxide layer and Platinum as the conducting electrode, scientists have explored different types of oxides, such as TaO_x [11, 12], HfO_x [13], MnO_x [14] and NiO [15], and different types of electrodes such as Pd, Ag, Ti, W, Ni, Au, Nb, Ta, and Al [11, 12]. In all of these devices, they were trying to reach the desired characteristics in terms of switching time, endurance, and switching power.

Moreover, some other devices, not based on oxides, were found to exhibit the same memristive behavior such as the motion of silver dopants in [16, 17], and Spin-Transfer Torque Magneto-resistive RAM (STT-MRAM) [18]. As an emerging device which has seen a steady growth over the last two years, memristors now have a devoted part in the International Technology Roadmap of Semiconductors (ITRS 2013) for memories, under the name of memristors and resistive RAM (ReRAM) [19]. ITRS summarizes the published devices and their properties, and it also sets the required properties for memristors in order to be commercialized in products.

1.1.4 Memristor Applications

Extensive researches investigating the potential applications of memristors have been conducted recently. Due to their outstanding characteristics, memristors have acquired the attention of many scientists around the globe in different fields of technology. Most of these applications can be categorized into biomedical applications, analog circuits applications, and digital circuits applications.

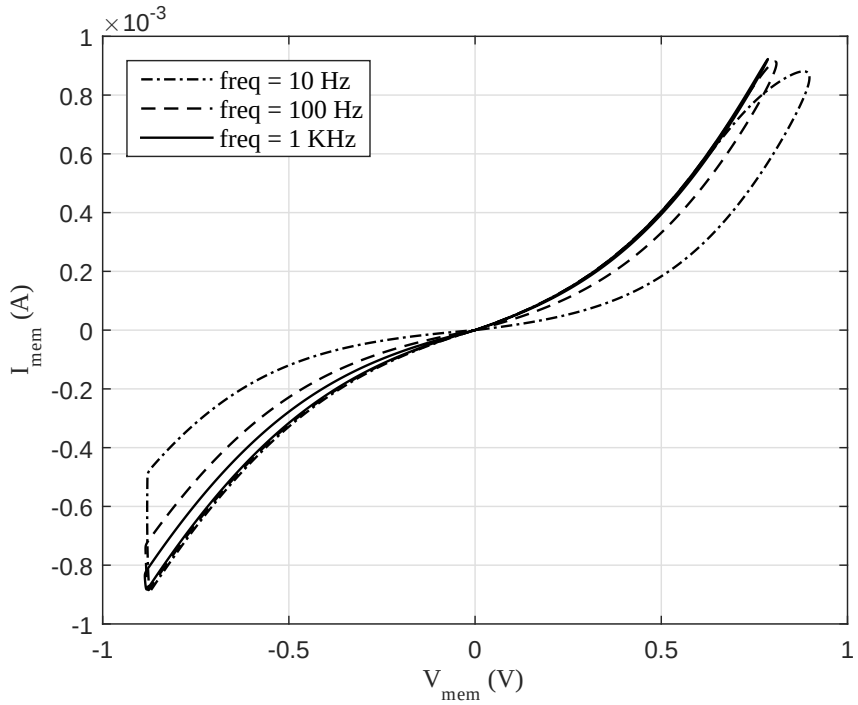


Figure 1.3: I-V characteristics of memristors for different frequencies.

1.1.4.1 Biomedical Applications

Memristor-based neuromorphic systems are considered very promising applications of memristor, in which the memristor is utilized to mimic the behavior of a synapse in the brain tissues [17, 20]. These types of applications make use of the dynamic behavior of memristor and its ability to keep the value of its resistance unchanged when the power is off. In a neural network, synapses are subjected to neural spikes which in return change their weight. Memristor can be used in a corresponding manner where voltage signals are used to change its resistance. Moreover, since these emerging devices are few nanometers in size, they can be used to fabricate high density and compact area chips which relatively approach the density of neural networks in a human brain. Memristors can also help to understand the behavior of some organic life form. Pershin *et al.* managed to design a circuit based on memristors that mimics the behavior of amoeba when exposed to a series of environmental changes [21].

1.1.4.2 Analog Circuits Applications

Recently, researchers used memristor to produce different analog circuits. Since memristors are compatible with CMOS technology, it was used to fabricate reactance-less oscillators [22, 23]. In these types of oscillators, memristors are used to mimic the behavior of reactive elements (e.g. capacitors and inductors), thus eliminating the need to use them in integrated circuits. Zidan *et al.* investigated a family of oscillators, named Memristor-Based Reactance-less Oscillators (MRLOs), derived closed form expressions for oscillating conditions, and presented the first realization of an MRLO [22]. Another analog application is reactance-less filters and adaptive filters. Driscoll *et al.* utilized memristor in LC circuits in such a way that the quality factor is improved upon application of certain frequency signals. So, the filter characteristics is adapted according to the input [24]. Moreover, Jameel *et al.* designed a bi-quadratic reactance-less filter based on memristor, where the cutoff frequency, quality factor, and bandwidth are functions of the memristor parameters [25].

1.1.4.3 Digital Circuits Applications

Digital circuits applications of memristor are countless and considered the most promising and applicable type of applications, ranging from non-volatile memory devices, to programmable and implication logic. Memristors can be used as storage elements, where logic one and zero can be represented by low and high resistances, respectively.

And for their small dimensions, memristors can be combined with CMOS technology to make crossbar-based memory chips, which are higher in density than the current technologies [26]. In addition, we are not restricted to binary representations anymore, we could use memristor as a multi-state memory element, thus achieving more dense memory chips [27]. And in order to take it to the next step, Micro and Sony plan to commercialize a memory stage in between DRAM and flash memory [28]. This memory stage is called Storage Class Memory (SCM) and is based on ReRAM, since it is required to be nonvolatile and high density.

Of course there are some problems that are facing these applications, for example, in crossbar-based memory chips, as shown in Fig. 1.4, memristor elements are arranged in a matrix form. An element is accessed by applying a read signal to the row and column that contains it [29]. However, other paths may contribute in this reading phase, thus giving a false data or even ruining it. This problem is called Sneak Paths problem. Fig. 1.4a shows the desired path, and Fig. 1.4b shows the desired path along with the undesired sneak paths. This problem was addressed by many researchers [29–31] and many solutions were developed in the last two years. One of the recent solutions is to use multiport reading technique instead single row and column technique [31]. Multiple readings were conducted through different ports to obtain a set of independent equations, then the value of the desired memristor is evaluated by simple addition and subtraction operations on the equations obtained. Fig. 1.4c shows the multiport technique along with its equivalent circuit. The device in blue represents the desired memristor, which its resistance is R_m, while the devices in green (R_r) and red (R_c) represent the row and column connected memristors with the desired memristor, respectively. The yellow memristors (R_a) represent the rest of the array. The equivalent circuit shows the connection between the equivalent resistances and the reading ports V_1 to V_4.

Another demonstration of digital applications is using memristors in logic operations. Many articles were published that exploit memristors in logic operations in different ways. Abdoli *et al.* combined memristors with CMOS in order to make an inverter [32]. In this family, the binary values are represented as voltage levels. Other applications involve the use of memristors as programmable switches for certain FPGA architectures [33]. In addition, the resistance of memristors can express the logical state, as mentioned earlier. In this case, memristor acts as the primitive building unit of the logic gates, where it can input, compute, output, and even store the signal. As a demonstration of this approach, Kvatinsky *et al.* utilized Material Implication logic gates (IMPLY logic gates [34]) to implement an 8-bit full adder [35]. The appealing trait of this approach is that it can be

integrated with memory crossbar arrays, in which they can perform logical operations and store data at the same time. This will open a new track towards powerful, complete, and very high density computing chips.

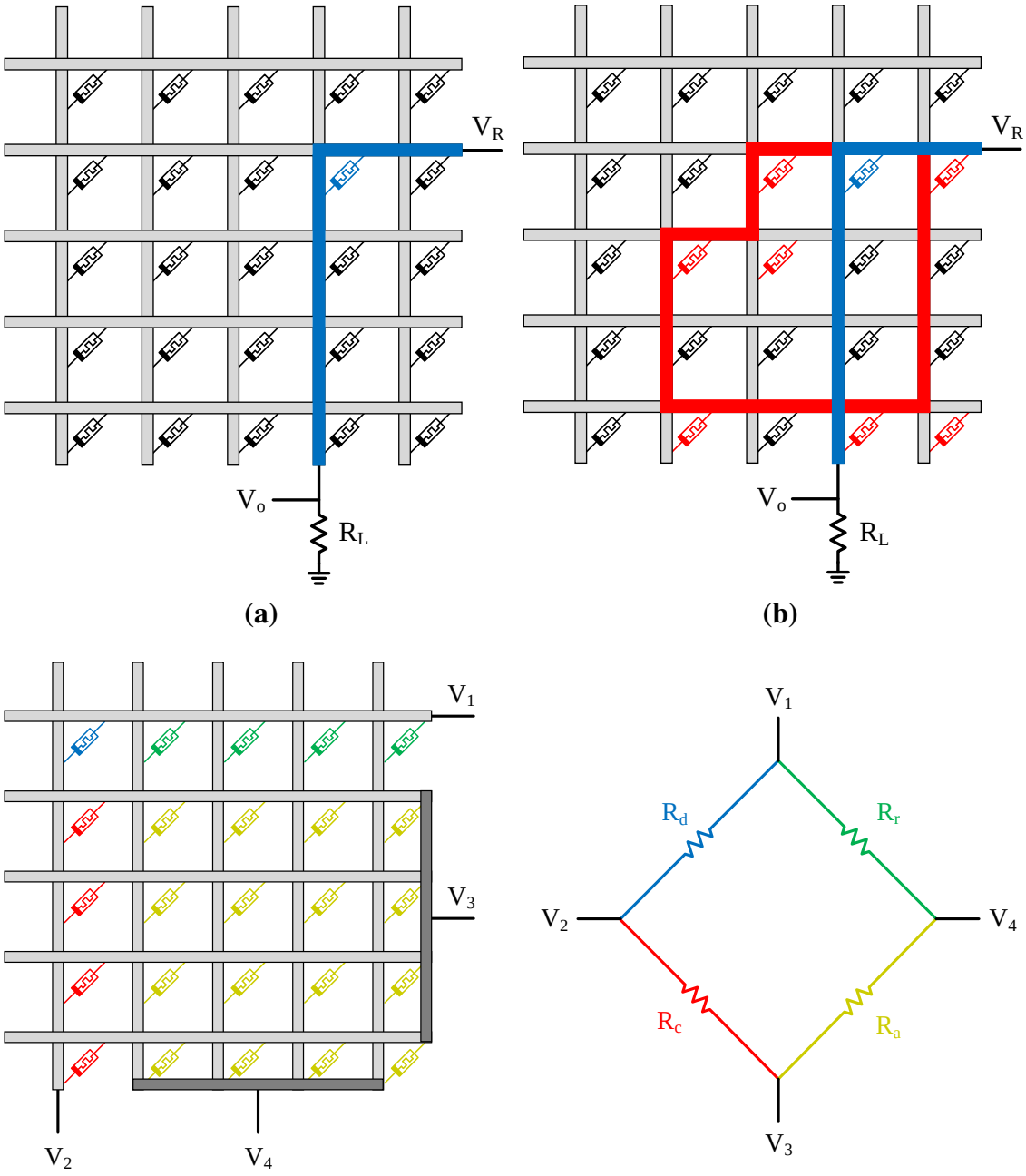


Figure 1.4: Crossbar memristors array. The blue path ((a) and (b)) shows the desired signal track in order to read the value stored in the blue memristor. The red paths (b) show the undesired tracks that the signal might flow in. (c) shows a potential solution by using multiport read out technique [31].

1.2 Thesis Goal and Methods

For maximizing the outcome of memristors, extensive studies have to be conducted in order to completely understand the mechanism behind it. Numerous researches are being published recently illustrating the physics behind the operation of memristors. Ionic migration and quantum electron tunneling are examples of these mechanisms. Physical models need to be constructed that accurately predict the behavior of memristors, and can produce results matching experimental data. Moreover, these models need to be capable of integration in circuit simulators, like SPICE, to be used for circuit designing and simulation. This requires the models to be relatively accurate (depending on the application), fast, and simple-enough to be converted to circuit models, like SPICE or Verilog-A code.

This thesis aims to introduce a new approach to improve the current modeling of memristors. This approach improves the accuracy and is verified against published models in terms of accuracy, simulation time, and density of simulation (number of memristors used in simulations). The research is conducted in two stages: device stage, and circuits stage. In the device stage, the proposed approach is applied and verified against published memristor experimental data to prove its validity. This was done using MATLAB. In the circuits stage, the physical model produced from our approach is implemented in SPICE and Verilog-A codes, then Candence Virtuoso is used in making circuit simulations.

1.3 Organization of the thesis

The Thesis is organized as follows: Chapter 2 sheds light extensively on the state of the art models of memristors and compares them against each other. Chapter 3 discusses our new approach in modeling, the physics behind it, and applying it using two different solving techniques. It also introduces SPICE and Verilog-A implementations to be used in circuit simulations. In chapter 4 the new approach are verified against experimental results to prove their accuracy. In addition, we study the use of our approach in some published digital and analog circuits. Finally, we conclude the thesis in chapter 5 with highlighting on the important outcomes we have reached and present some ideas that could be important as a future work.

Chapter 2

Literature Review

Since the discovery of memristors in 2008, researches around the world had reported memristive-like behaviors in different nanoscale devices. On the other hand, various physical models were developed over the last few years to help us understand the mechanism of conduction in memristive devices. In this chapter, we are going to shed some light over different types of memristors in literature and different fabrication techniques of memristive devices. In addition, we are going to review most of the versatile memristor models that are used nowadays by many circuit designers.

2.1 Memristors Categories

Without loosing generality, memristive devices can be categorized into two major categories: Molecular and Thin Film Memristive Devices, and Spintronic Memristive Devices [36]. As shown in Fig. 2.1, the Molecular and Thin Film Memristive Devices are composed of Oxide-Based Memristors and Ionic (Polymeric)-Based Memristors.

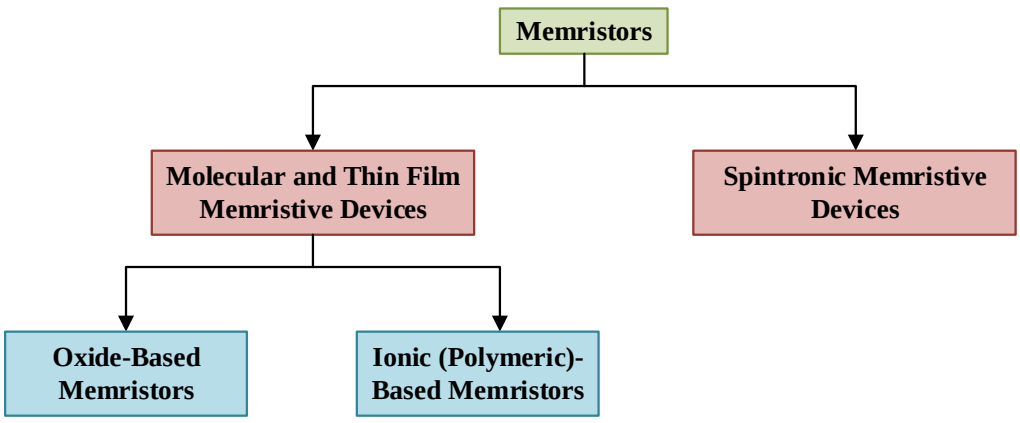


Figure 2.1: Memristors categories [36].

2.1.1 Spintronic Memristive Devices

The operation in this type of devices depends on altering the electron spin polarization to change the resistance of the device [18, 37]. To elaborate more, Fig. 2.2 shows a typical structure of a spintronic memristor, which is composed of two ferromagnetic layers: free layer and reference layer. The free layer is separated into two sections with opposite spin direction by a magnetic domain wall, while the reference layer has a fixed spin direction [37]. The relative spin direction between each segment and the reference layer determines the resistance of the device. Same (opposite) relative spin direction means low (high) resistance. The whole resistance of the device can be determined by eq. (2.1) [37]:

$$M(x) \quad = \quad (x.R_H + (D - x).R_L) \tag{2.1}$$

where R_H and R_L are the resistances per unit length for the high and low resistance states, respectively, D is the length of the device, and x is the position of the magnetic domain wall. The velocity of the domain wall motion depends on the the current density passing through the device. The interesting trait of this type of memristors is that its fabrication is relatively easy and requires similar fabrication technology like the one used in manufacturing the spin valve head of a hard disk drive [37].

2.1.2 Ionic (Polymeric)-Based Memristors

The memristance behavior in Ionic-Based memristors is exhibited via changing their electrical conductivity. This conductivity is changed via the motion of solid state ionics, cationic or anionic, through the device. Usually the device is structured as passive thin film layer sandwiched between an electrode and an active layer (acts as the source of

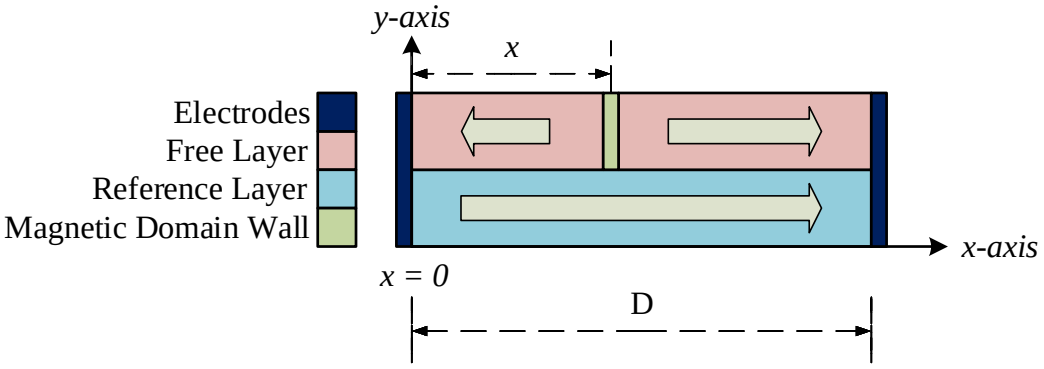


Figure 2.2: Device Structure of the spintronic memristor in [37].

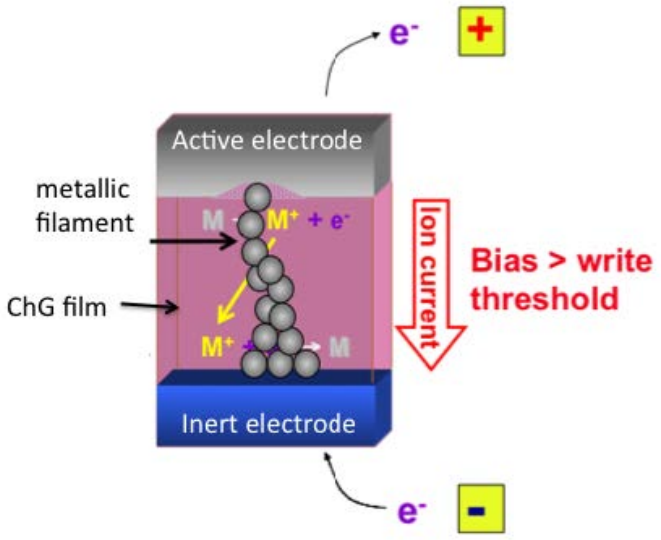


Figure 2.3: Device Structure of Ionic-Based memristor in [16].

ionics) [16, 38]. Fig. 2.3 shows an example of such a device. The Passive thin film here is made of Chalcogenide Glass (ChG) films and the active layer is Ag thin layer. Upon applying a bias above a certain voltage, Ag+ ions are formed at the active layer/ChG film interface and starts to flow through ChG film making a conducting filament. Thus the conductivity of the passive film is changed [16].

These types of devices have attractive characteristics that made them under extensive research the last few years [38]. Polymer materials are relatively low in cost, easily processed, and mechanically flexible. In addition, they can be handled via blade casting, dip and spray coating, and even ink-jet printing, thus adding more flexibility in way they are processed [38].

2.1.3 Oxide-Based Memristors

As mentioned in chapter 1, this type of memristors is fabricated as metal oxide films sandwiched between two metal electrodes. The conduction in these devices takes place via oxygen vacancies in the oxide, as charge carriers. Among all the oxides mentioned earlier, this thesis focus on TiO_x based memristors, as it is the widely studied one.

Creating the active layer in TiO_x memristors, the oxygen deficient layer or doped TiO_2 layer, has two forms, as discussed next.

2.1.3.1 Active Layer Deposition

The structure of TiO_2 memristors is shown in Fig. 2.4a, in which a doped TiO_{2-x} layer (rich in oxygen vacancies) is deposited on top of an undoped TiO_2 layer. These two layers are sandwiched between two platinum electrodes. An example of these structures can be found in [8, 39], where in the later one TiO_2/TiO_{2+x} is used instead of TiO_2/TiO_{2-x}. The only difference between the two bi-layers mentioned before is the charge carriers, where in TiO_2/TiO_{2+x} they are negatively charged oxygen ions, while in TiO_2/TiO_{2-x} they are positively charged oxygen vacancies [39]. A diagram illustrating the procedure, used in [39], of fabricating a device in this way is shown in Fig. 2.4b. The interface between the TiO_2/TiO_{2-x} (TiO_2/TiO_{2+x}) moves along with (opposite to) the electric field.

2.1.3.2 Electroforming

In this process, a layer of metal-oxide is sandwiched between two metal electrodes. The active layer of oxygen vacancies is formed in the device as thin conducting filaments that grow along most of the oxide thickness except for a small width *w*, as shown in Fig. 2.5. These filaments are rich in oxygen vacancies, thus, they represent the doped oxide layer. The filaments are formed by a process called *electroforming*, in which we apply a relatively large voltage bias (larger than the normal operating range) across the device. The formed filament in the device is permanent and is the reason for the change in device conductivity. Fig. 2.5a and Fig. 2.5b show the device structure before and after

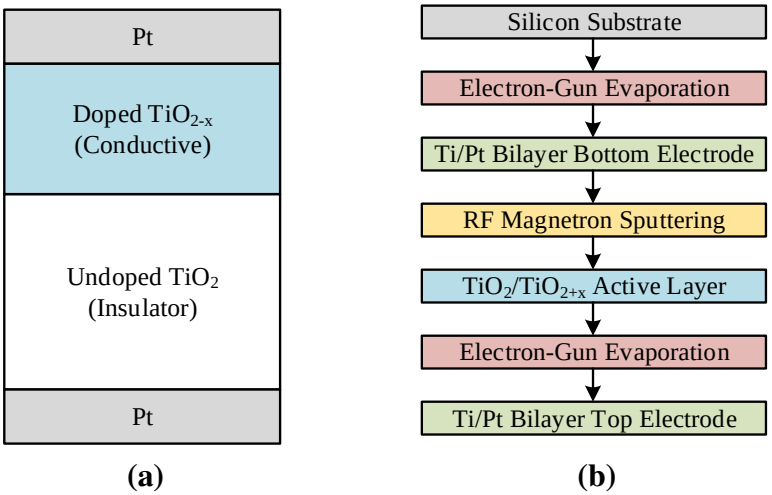


Figure 2.4: (a) Device structure based on TiO_{2-x} layer deposition. (b) Fabrication steps for making such a device in Fig. 2.4a.

Figure 2.5: Device structure (a) before and (b) after *electroforming*.

electroforming process, respectively, for a TiO_2 memristor in [40]. The filament length grows or shrinks according to the polarity of the applied bias, thus, changing the small width w, shown in Fig. 2.5b. Modulating the width w is the main reason for the change in the device resistance [40]. This thesis will focus on devices formed by this process.

Yang *et al.* [41] fabricated a TiO_2 memristor device with a typical structure of Si/SiO_x /Ti (5 nm)/Pt (15 nm)/TiO_2 (50 nm)/Pt (30 nm), where Si and SiO_x act as the substrate and Ti is deposited for improving the junction properties. Fig. 2.6a and 2.6b show Atomic Force Microscopy (AFM) images of the device before and after the electroforming process, respectively [41]. A dome-like physical deformation, representing the conductive filament, has appeared along the edge of the bottom electrode (Fig. 2.6b).

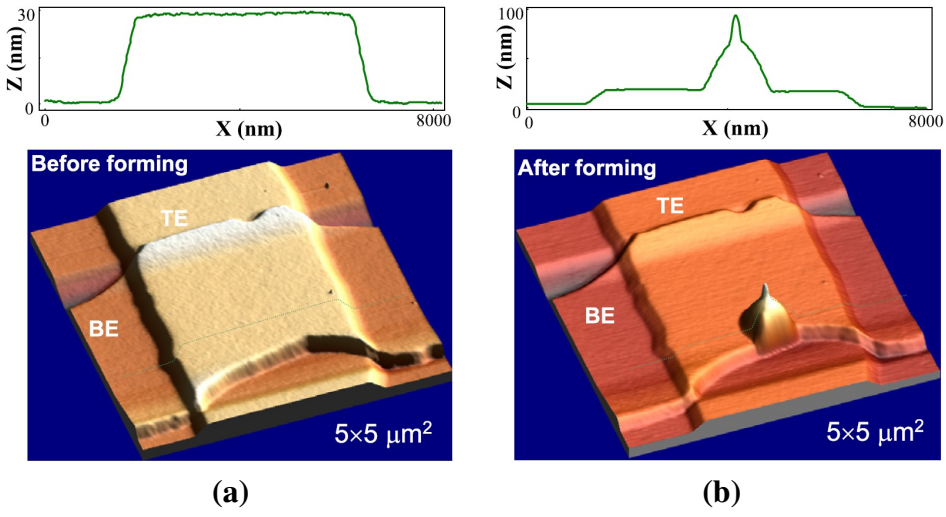


Figure 2.6: AFM images of the device in [41] before and after *electroforming*.

2.2 Different Memristor Models

Numerous models have been published in the last few years describing the conduction mechanisms in different memristors. These models were very simple at the beginning and they kept getting more complex by time. In this section we are going to mention some of the famous models that have been used by many researchers in the last period.

2.2.1 Linear Ion Drift Model

This was one of the earliest models that describe the memristor behavior. As discussed in chapter 1, It was proposed by Strukov *et al.* in [8]. Fig. 1.2 shows the structure of the device, which is composed of a highly doped region (TiO_{2-x}) of width w and another undoped region (TiO_2) of width D-w. The width of the TiO_{2-x} is changed according to the polarity of the applied voltage. Assuming ohmic conductance in the TiO_{2-x} region and linear ionic motion under uniform electric field, the equations governing this model are:

$$V(t) = \left(R_{on}\frac{w(t)}{D} - R_{off}\left(1 - \frac{w(t)}{D}\right)\right).I(t) \tag{2.2}$$

$$\frac{dw}{dt} = \mu_v \frac{R_{on}}{D}.I(t) \tag{2.3}$$

where R_{off} is the resistance when $w(t) = 0$, and R_{on} is the resistance when $w(t) = D$. μ_v is the average mobility of the dopants. The memristor can be thought of as two varying resistors in series with each other, as shown in Fig. 2.7. The left (right) resistor represents the doped (undoped) region in Fig. 1.2. Fig. 2.8 shows the I-V characteristics for a sinusoidal input of frequency $\omega_o = 1\ rad/s$.

The internal state variable $w(t)$ has the limits of $0 < w(t) < D$. To prevent it from extending beyond its limits, eq. (2.3) is multiplied by a window function $f(w)$. The

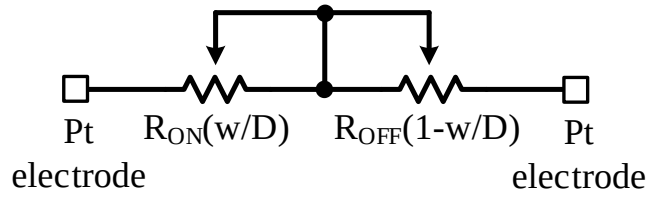


Figure 2.7: The memristor modeled as two varying resistors in series [8].

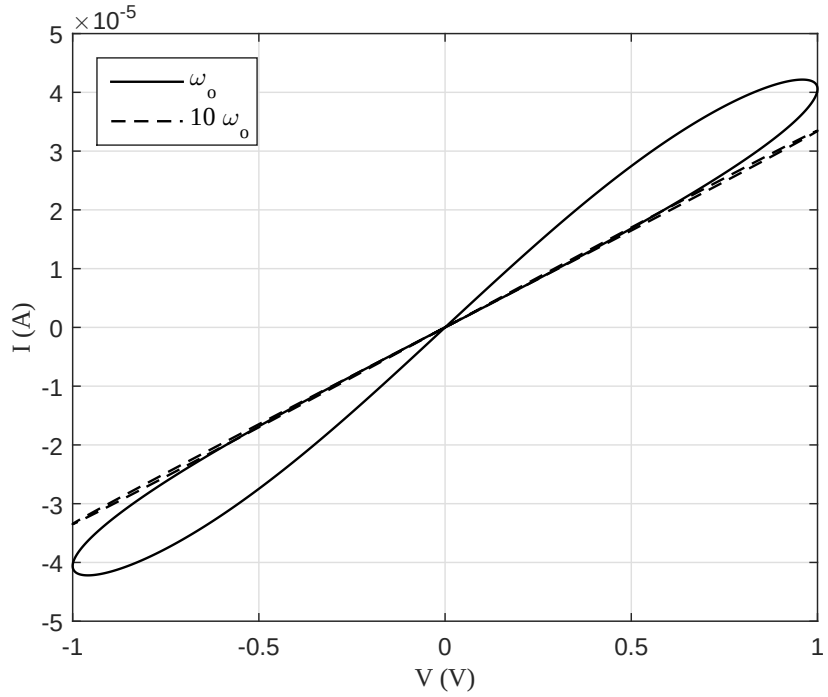


Figure 2.8: I-V characteristics for a sinusoidal input. The parameters used are: $R_{OFF} = 16\ k\Omega$, $R_{ON} = 100\ \Omega$, D = 10 nm, and $\mu_v = 10^{-14}\ m^2S^{-1}V^{-1}$.

purpose of this window function is to make the derivative vanishes when w reaches its bounds. Different window functions were proposed, the simplest of them is a rectangle window function, which:

$$f(w) = \begin{cases} 1, & 0 < w < D \\ 0, & w = \{0, D\} \end{cases} \tag{2.4}$$

Another more practical window function is the one derived in [42], in which nonlinear ionic drift is assumed. This function implements an obsereved phenomenon which the drift velocity of the ions,$\left(i.e.\ \frac{dw}{dt}\right)$, decreases as we approach the physical boundaries [42]. The equation is:

$$f(w) = 1 - \left(\frac{2w}{D} - 1\right)^{\alpha} \tag{2.5}$$

where α is a positive number. As shown in Fig. 2.9, as α increases, the window function approaches a rectangular one and the nonlinear effect vanishes.

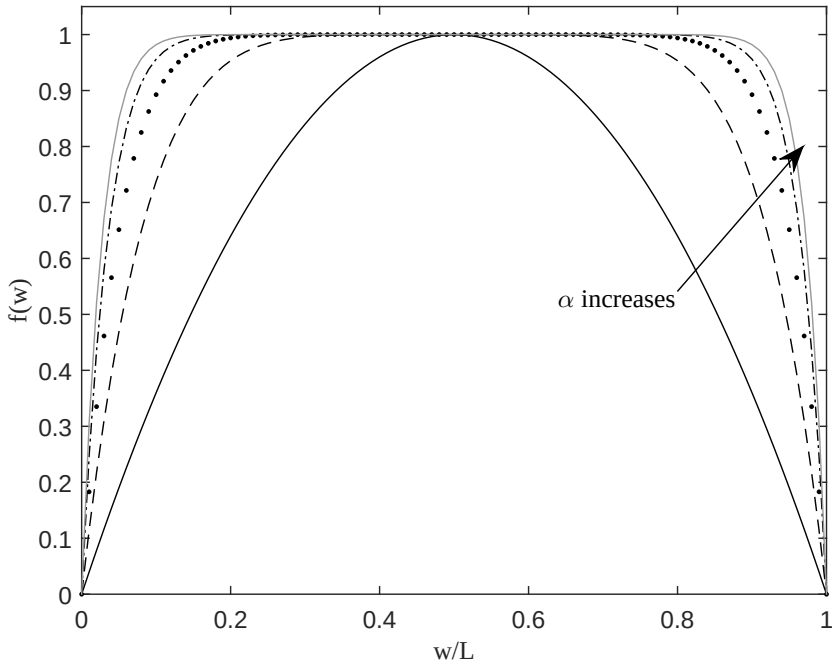


Figure 2.9: Window function described in [42] for several values of α.

However, this window function has a serious problem since the state variable w cannot change its value once it reached any of the boundaries. To solve this problem, Biolek *et al.* [43] suggested the following modification:

$$f(w) \quad = \quad 1 - \left(\frac{w}{D} - stp\,(-I) \right)^{\alpha} \tag{2.6}$$

where I is the current passing through the device and $stp(x)$ is the normal step function. Fig. 2.10 shows this window function.

The main issue of the linear ion drift model is that it ignores the nonlinear dependence of the internal state variable, w, on the current. This issue will be addressed by the following models.

2.2.2 Non Linear Ion Drift Model

The linear ion drift model captures the basic behavior of memristor qualitatively, however, it fails to follow the experimental results of many fabricated devices [44]. Due to the severe nonlinearity in the I-V characteristics, Lehtonen *at al.* [45] proposed a nonlinear model based on the experimental results in [44], where the I-V realtion is:

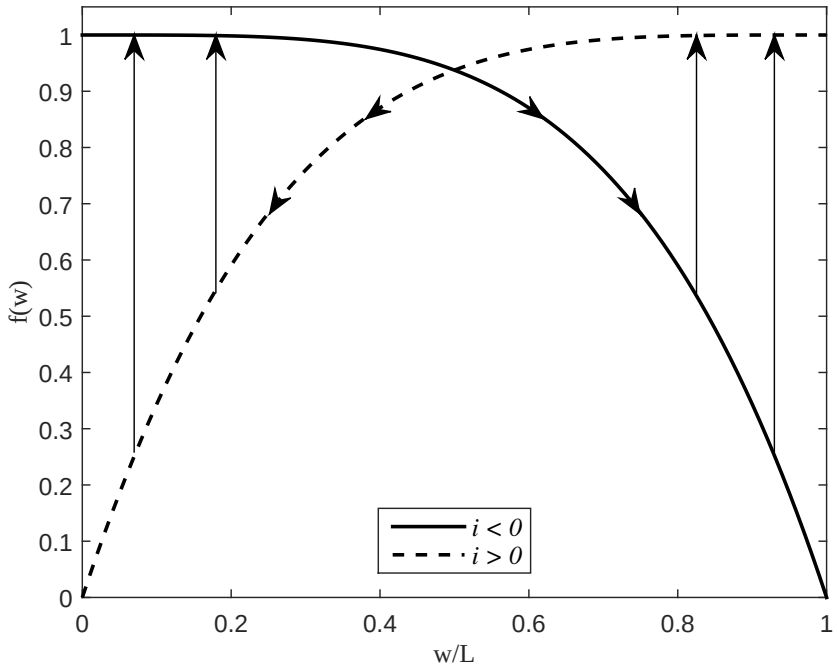


Figure 2.10: Modified window function according to [43].

$$I(t) \quad = \quad w(t)^n \beta sinh(\alpha V(t)) + \chi \left[e^{\gamma V(t)} - 1 \right] \tag{2.7}$$

where *I(t)* and *V(t)* are the current and the voltage through the device, respectively. α, β, γ, and χ are fitting parameters determined by the experimental results, and n is a parameter which determines the dependence of *I(t)* on the state variable *w(t)*. It is also important to mention that the state variable is normalized in this model, which it can only take any value between 0 and 1. In the ON state, w approaches the unity and the current is dominated by the term $\beta sinh(\alpha V(t))$, while in the OFF state the current is dominated by the second term $\chi \left[e^{\gamma V(t)} - 1 \right]$. The drift velocity in this model is:

$$\frac{dw}{dt} \quad = \quad a.f(w).[V(t)]^m \tag{2.8}$$

where a is a constant, m is an odd constant, and *f(w)* is the window function. Fig. 2.11 shows the I-V characteristics of the model for a sinusoidal input and different frequencies [45].

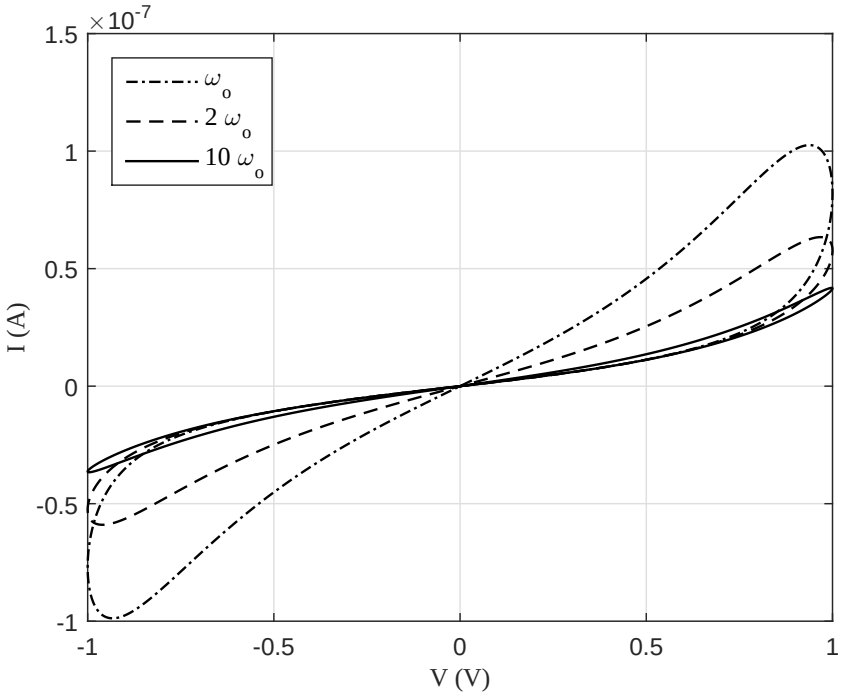


Figure 2.11: I-V characteristics for a sinusoidal input. The parameters used are: $m = 5$, $n = 2$, a = 1 $V^{-m}S^{-1}$, $\beta = 0.9$ μA, $\gamma = 4$ V^{-1}, $\chi = 10^{-4}$ μA, and $\alpha = 2$ V^{-1}.

2.2.3 Simmons Tunneling Model for Similar Electrodes

The previous two models were representing the memristor as two resistors in series and were mainly developed for memristors based on active layer deposition. For memristors based on electroforming, another model was developed in [40], where the memristor is modeled as a resistor in series with a rectangular electron tunneling barrier. Picket *et al.* [40] fabricated a memristor with the structure of Si/SiO_2 (100 nm)/Ti (5 nm)/Pt (15 nm)/TiO_2 (50 nm)/Pt (30 nm). After electroforming, a filament that shunts most of TiO_2 height is formed, as shown in Fig. 2.5b. The filament is very conductive compared to the oxide TiO_2 and is modeled as a resistor of value R_f, while the thin oxide layer of width w, between the filament and the top platinum electrode, is modeled as a rectangular potential barrier which electrons can tunnel through. The current passing though the potential barrier is modeled according to Simmons tunneling model for similar electrodes [46], and the equations are [47]:

$$i = \frac{eA}{2\pi h \Delta w^2}\left\{\overline{\varphi_o} e^{-B\sqrt{\overline{\varphi_o}}} + \left(\overline{\varphi_o} + e\left|v_g\right|\right) e^{-B\sqrt{\overline{\varphi_o}+e\left|v_g\right|}}\right\} \tag{2.9}$$

$$\overline{\varphi_o} = \varphi_o - e\left|v_g\right|\left(\frac{w_1 + w_2}{2w}\right) - \left(\frac{1.15\lambda w}{\Delta w}\right)\ln\left(\frac{w_2(w - w_1)}{w_1(w - w_2)}\right) \tag{2.10}$$

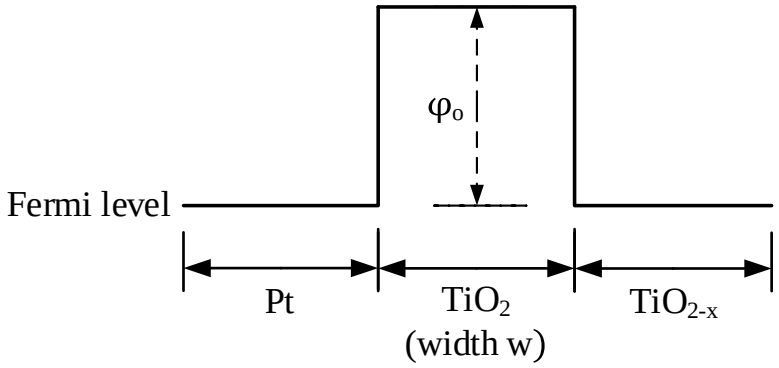


Figure 2.12: Band diagram describing the device after electroforming. φ_o is the tunneling barrier height.

$$w_2 = w_1 + w\left(1 - \frac{9.2\lambda}{3\varphi_o + 4\lambda - 2e|v_g|}\right) \tag{2.11}$$

$$w_1 = \frac{1.2\lambda w}{\varphi_o} \tag{2.12}$$

where

$$\Delta w = w_2 - w_1, \qquad B = \frac{2\pi\Delta w\sqrt{2m}}{h}, \qquad \lambda = \frac{e^2\ln(2)}{8\pi\varepsilon_r\varepsilon_o}w \tag{2.13}$$

and e is the electron charge, h is Planck's constant, A is the filament area of the memristor, m is the mass of the electron , i is the current passing through the device, v_g is the voltage drop across the tunnel barrier, ε_r is the dielectric constant of TiO_2, and φ_o is the barrier height. Fig. 2.12 shows the energy band diagram, assumed in [40], that describes the memristor device. Let V_{mem} denote the voltage across the whole device, thus $V_{\text{mem}} = v_{\text{g}} + iR_{\text{f}}$. B, λ, w_1, and w_2 are parameters from Simmons tunneling model for similar electrodes [46].

The tunneling width is the internal state variable and its rate of change is modeled as [47]:

$$\frac{dw}{dt} = \begin{cases} f_{fb}\sinh\left(\frac{i}{i_{fb}}\right)\exp\left(-\exp\left(\frac{w-a_{fb}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right), & i > 0 \\ f_{rb}\sinh\left(\frac{i}{i_{rb}}\right)\exp\left(-\exp\left(\frac{a_{rb}-w}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right), & i < 0 \end{cases} \tag{2.14}$$

where f_{fb}, f_{rb}, i_{fb}, i_{rb}, a_{fb}, a_{rb}, w_c, and b are the fitting parameters.

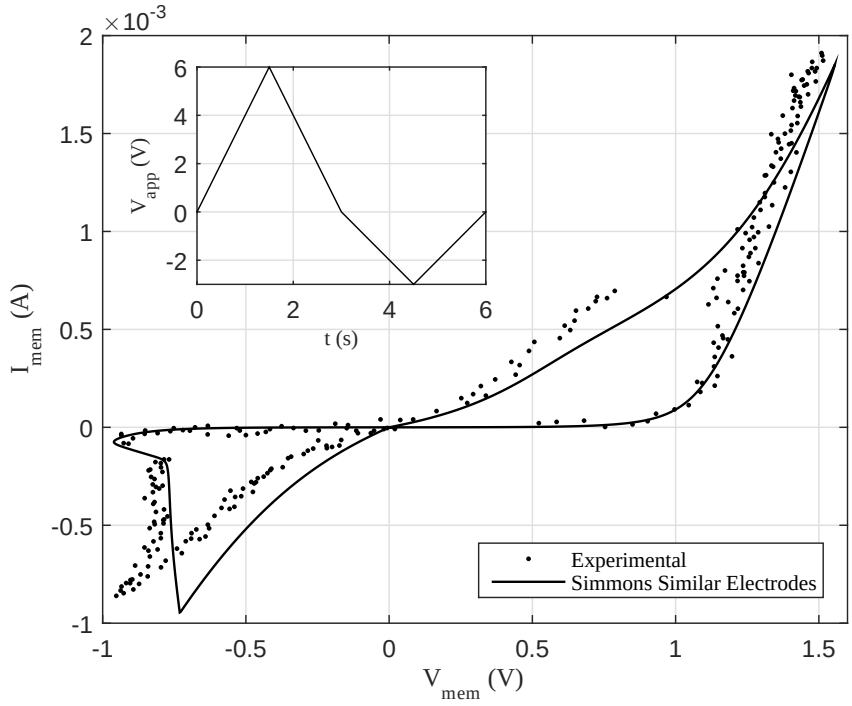


Figure 2.13: I-V characteristics of Simmons model of similar electrodes. The parameter used are $A = 10^4$ nm^2, $\varepsilon = 5$, $\varphi_o = 0.95$ eV, $R_f = 215\ \Omega$, $f_{fb} = 3.5\ \mu m$, $f_{rb} = 40\ \mu m$, $i_{fb} = 115\ \mu A$, $i_{rb} = 8.9\ \mu A$, $a_{fb} = 1.2$ nm, $a_{rb} = 1.8$ nm, $w_c = 107$ pm and $b = 500\ \mu A$.

Practically, the OFF switching is lower than the ON switching [48]. The parameters f_{fb} and f_{rb} control the magnitude of the change in ω, while i_{fb} and i_{rb} act as thresholds in which the rate of change beyond them is negligible.

Fig. 2.13 shows the I-V characteristics of the Simmons model for similar electrodes upon applying a triangular wave form as shown in the inset of the figure. The solid line represent the theoretical model and the dots represent the experimental data of [47].

2.2.4 Varying Filament Area Model

Another recent model based on electroformed memristors is the one proposed by Strachan *et al.* in [49]. They fabricated a Ta_2O_5 memristor device, structured as Pt/Ta_2O_5/Ta. The device structure after electroforming is shown in Fig. 2.14. The device is composed of a conducting filament, Ta(O), which is considered of linear I-V dependence, and the region surrounding the conducting filament, TaO_x, which has different oxygen vacancies concentration. Taking y, the ratio between the area of the conductive filament to the area of the whole channel, as the internal state variable, the

current through the device can be modeled as two different transport mechanism in parallel to each other. A metallic conducting channel (i.e. linear I-V relation) of fraction y and another insulating with nonlinear transport of fraction 1-y [49]. Thus, the current equation is:

$$i = v\left(yG_m + (1-y)\,ae^{b\sqrt{|v|}}\right) \tag{2.15}$$

where G_m, a, and b are constants that depends of the properties of a particular device. G_m represents the conductance of the device when the metallic filament, Ta(O), fill all the channel, thus, $y = 1$. The other term represents Frenkel–Poole relationship when the other region, TaO_x, fills all the channel, thus, $y = 0$ [49]. The dynamical state equation representing the rate of change of the internal state variable y is:

$$\frac{dy}{dt} = \begin{cases} A.sinh\left(\frac{v}{\sigma_{off}}\right)e^{-\left(\frac{y_{off}}{y}\right)^2}e^{\left(\frac{1}{1+\beta p}\right)}, & v < 0 \\ B.sinh\left(\frac{v}{\sigma_{on}}\right)e^{-\left(\frac{y}{y_{on}}\right)^2}e^{\left(\frac{p}{\sigma p}\right)}, & v > 0 \end{cases} \tag{2.16}$$

where A, B, σ_{off}, σ_{on}, y_{off}, y_{on}, p, σ_p, and β are fitting parameters for a particular device properties.

Fig. 2.15 shows the I-V characteristics of the varying filament area model upon applying triangular voltage cycle with different sweep rates [49]. The total cycle time

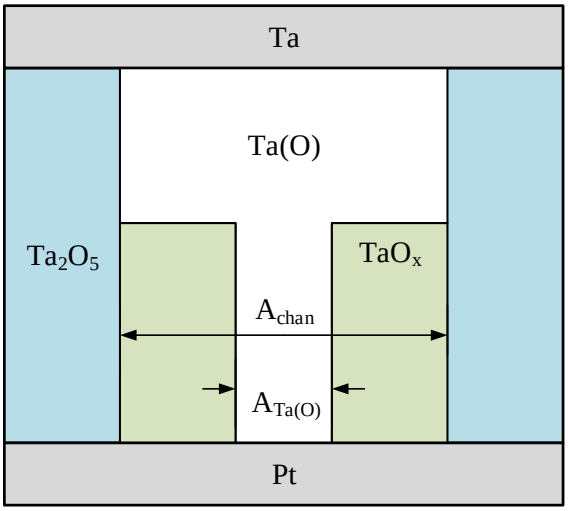


Figure 2.14: The device structure as proposed in [49].

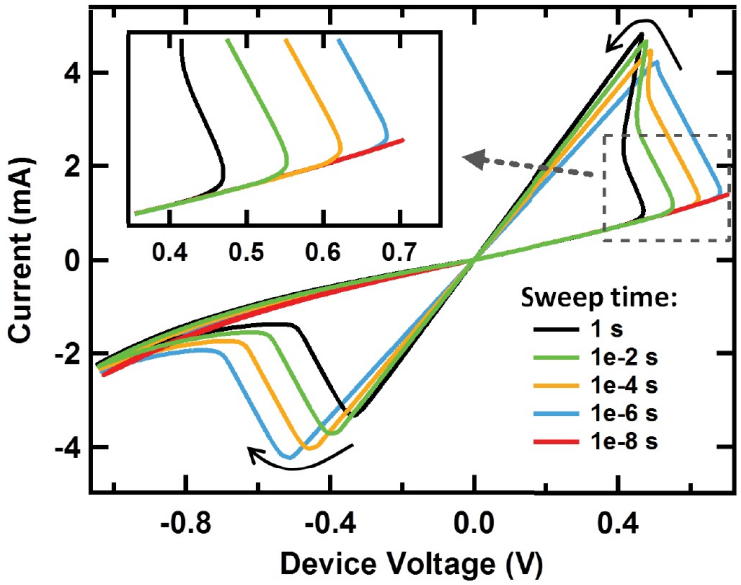


Figure 2.15: I-V characteristics of the studied model upon applying a triangular voltage cycle of different frequencies. The voltage sequence is 0, 0.8, 0, −1.2, and 0 V, while the fitting parameters can be found in [49].

was varied from 1 s to 10 ns, with an initial OFF state in all cases. The inset shows that the device has a switching voltage threshold that is directly proportional to the bias frequency.

2.2.5 Generalized Models

All the above models were developed after fabricating a memristor device. Other researchers have made good effort trying to produce generalized models with more fitting parameters to be adjusted for every memristor device. In this section, we are going to investigate some of them.

2.2.5.1 University of Dayton Model

Yakopcic *et al.* [50] introduced a generalized model and implemented it in SPICE code. The I-V relation for this model are [50]:

$$I(t) = \begin{cases} a_1 x(t) \sinh(bV(t)), & V(t) \geqslant 0 \\ a_2 x(t) \sinh(bV(t)), & V(t) < 0 \end{cases} \tag{2.17}$$

where *I(t)* and *V(t)* are the current and voltage across the memristor, respectively, and a_1, a_2, and b are fitting parameters to fit the model to different memristors. *x(t)* is the state variable of the device.

The state dynamics equation is determined by:

$$\frac{dx}{dt} = g(V(t)).f(x(t)) \tag{2.18}$$

where *g(V(t))* is a function which represents the dependence of the state variable on the applied voltage. It also implements the threshold voltage which the applied signal has to cross in order for the state variable to change. *g(V(t))* is:

$$g(V(t)) = \begin{cases} A_p\left(e^{V(t)} - e^{V_{pt}}\right), & V(t) > V_{pt} \\ 0, & V_{nt} \leqslant V(t) \leqslant V_{pt} \\ -A_n\left(e^{-V(t)} - e^{V_{nt}}\right), & V(t) < V_{nt} \end{cases} \tag{2.19}$$

where A_p and A_n are fitting parameters determining the magnitude of the function, and V_{pt} and V_{nt} are the positive and negative threshold voltages, respectively.

f(x(t)) is the function implementing the dependence of the derivative on the state variable and is:

$$f(x) = \begin{cases} \begin{cases} e^{-\alpha_p(x-x_p)} w_p\left(x, x_p\right), & x \geqslant x_p \\ 1, & x < x_p \end{cases} \\ \begin{cases} e^{\alpha_n(x+x_n-1)} w_n(x, x_n), & x \leqslant 1 - x_n \\ 1, & x > 1 - x_n \end{cases} \end{cases} \tag{2.20}$$

where α_p and α_n are parameters representing the decaying rate of the exponential, and x_p and x_n are the limits where beyond them the internal state variable velocity is constant (i.e. doesn't depend on x).

$w_n(x, x_n)$ and $w_p\left(x, x_p\right)$ are window function represented as:

$$w_p\left(x, x_p\right) = \frac{x_p - x}{1 - x_p} + 1 \tag{2.21}$$

$$w_n(x, x_n) = \frac{x}{1 - x_n} \tag{2.22}$$

The results of applying this model to the experimental data published in [44], is shown in Fig. 2.16. The fitting parameters were [50]: $A_p = 5$, $A_n = 30$, $V_p = 1.2$ V, $V_n = 0.6$ V, $\alpha_p = 4$, $\alpha_n = 24$, $x_p = 0.7$, $x_n = 0.8$, b = 1, $a_1 = 2.3{\times}10^{-4}$, $a_2 = 3.8{\times}10^{-4}$, and $\mathrm{x_o} = 0.02$.

Although this model fits some of the published experimental data, but it is not based on a physical concept.

2.2.5.2 TEAM Model

Another generalized model is the ThrEshold Adaptive Memristor (TEAM) model [51]. The states dynamics equations in this model are:

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}\left(\frac{i(t)}{i_{off}} - 1\right)^{\alpha_{off}} f_{off}(w), & i_{off} < i \\ 0, & i_{on} < i < i_{off} \\ k_{on}\left(\frac{i(t)}{i_{on}} - 1\right)^{\alpha_{on}} f_{on}(w), & i < i_{on} \end{cases} \tag{2.23}$$

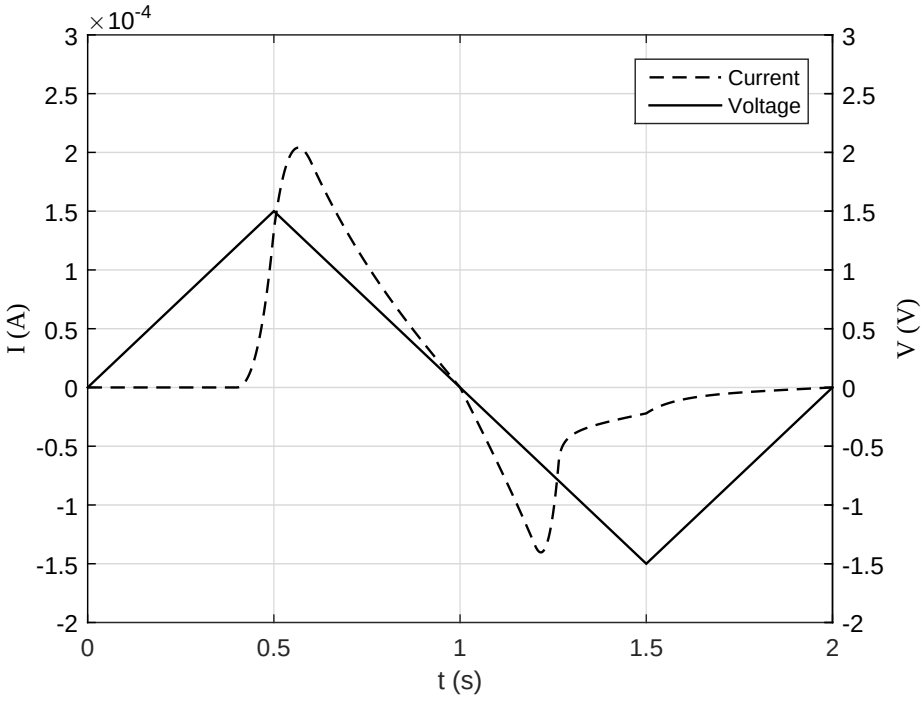
where k_{off}, k_{on}, α_{off}, and α_{on} are fitting parameters to be adjusted with each device, i_{off} and i_{on} are current thresholds in the off and on switching, respectively. and w is the internal state variable of the device. $f_{off}(w)$ and $f_{on}(w)$ are the window functions that limit the internal state variable to its limits and take the form:

$$f_{off}(w) = \exp\left(-\exp\left(\frac{w - a_{off}}{w_c}\right)\right) \tag{2.24}$$

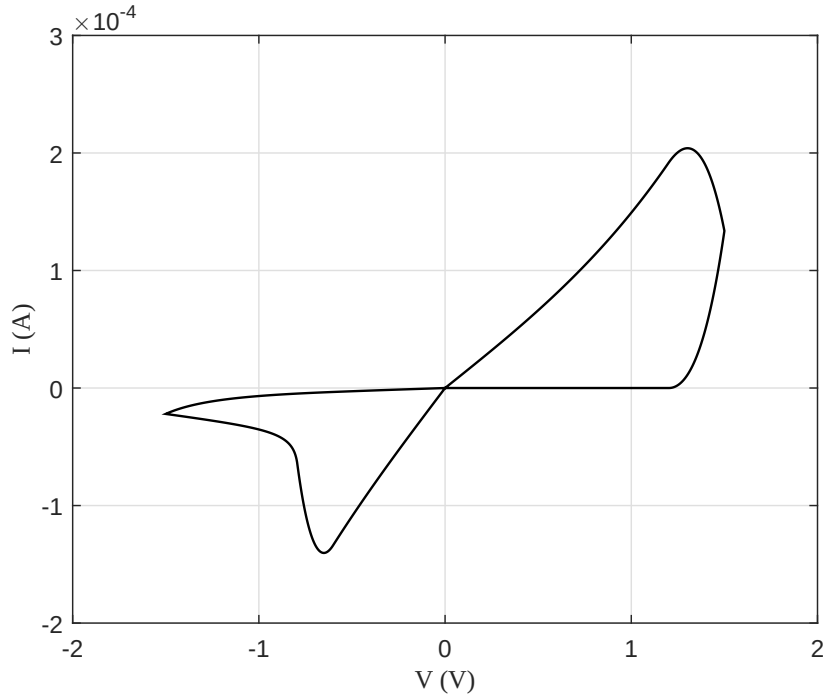
$$f_{on}(w) = \exp\left(-\exp\left(\frac{a_{on} - w}{w_c}\right)\right) \tag{2.25}$$

where a_{off}, a_{on} are the parameters that approximately nullifies the derivative around them in the off and on switching, respectively. As we can see, eq. (2.24) and (2.25) are similar to the exponential part of eq. (2.14). They have proved that mathematically in [51] that the state dynamics equations in TEAM model approaches their counterpart in Simmons tunneling model for similar electrodes.

Unlike all the previous models, the I-V relationship in this model is undefined and can be chosen freely from any other I-V relationships. For example, for the case of linear ionic drift, the I-V realtion takes the form:



(a)



(b)

Figure 2.16: Simulation results of applying Yakopcic mode to the results in [44]. (a) shows the current and voltage versus time, and (b) shows the I-V characteristics.

$$v(t) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{w_{off} - w_{on}}.(w - w_{on})\right] i(t) \tag{2.26}$$

another I-V relationship, that can be used to reproduce the same I-V characteristics in case of Simmons model for similar electrodes, is:

$$v(t) = R_{ON} e^{\left(\frac{\lambda}{w_{off} - w_{on}}\right)(w - w_{on})}.i(t) \tag{2.27}$$

$$e^{\lambda} = \frac{R_{ON}}{R_{OFF}} \tag{2.28}$$

where λ is a fitting parameter satisfying eq. (2.28), R_{ON} and R_{OFF} are the effective resistances when w reaches its boundaries w_{on} and w_{off}, respectively. The simulation results of applying a sinusoidal input of 1 volt are shows in Fig. 2.17 for the following parameters: R_{ON} = 50 Ω, R_{OFF} = 1 KΩ, k_{off} = 1.46 nm/s, k_{on} = -4.68e-4 nm/s, α_{off} = 10, α_{on} = 10, i_{off} = 115 μA, i_{on} = 8.9 μA, a_{off} = 1.2 nm, a_{on} = 1.8 nm, and w_c = 107 pm.

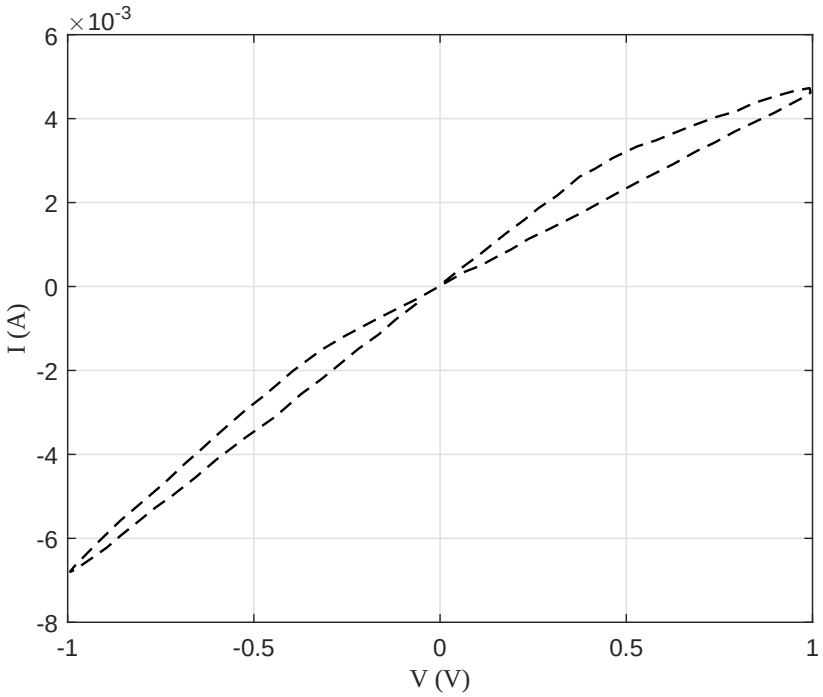
The above model is called current controlled model, where the internal state variable changes only above certain current thresholds for the off and on switching. Other experimental results have reported memristors behavior with voltage threshold [8, 52], such that state variable is changed above certain voltage thresholds. A modified version of the above model called Voltage TEAM (VTEAM) model is published in [53], where the state dynamics equations are:

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}\left(\frac{v(t)}{v_{off}} - 1\right)^{\alpha_{off}} f_{off}(w), & v_{off} < v \\ 0, & v_{on} < v < v_{off} \\ k_{on}\left(\frac{v(t)}{v_{on}} - 1\right)^{\alpha_{on}} f_{on}(w), & v < v_{on} \end{cases} \tag{2.29}$$

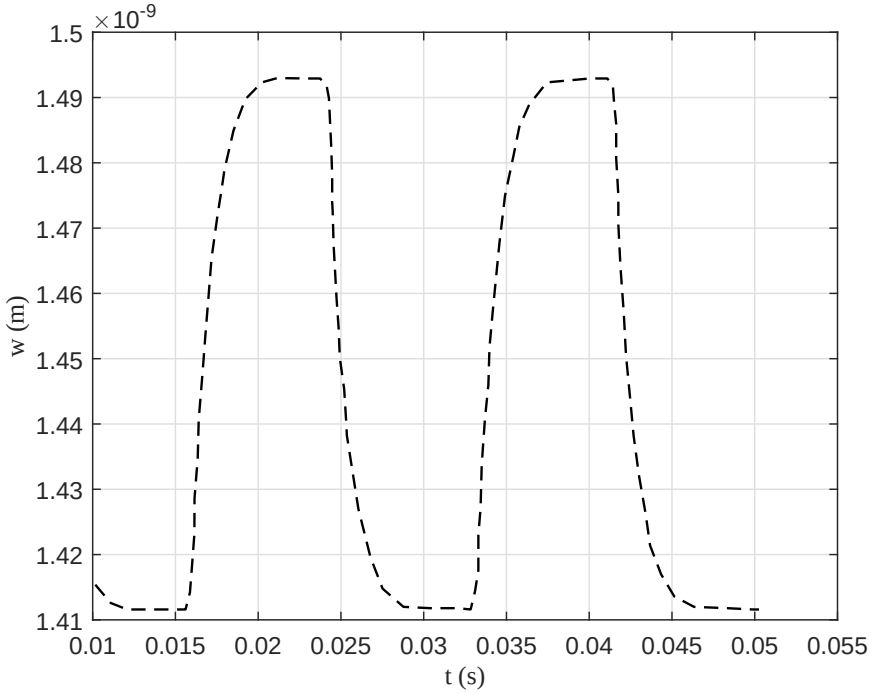
where v_{off} and v_{on} are the voltage thresholds in case of the off and on switching, respectively, while the I-V relations becomes:

$$i(t) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{w_{off} - w_{on}}.(w - w_{on})\right]^{-1} v(t) \tag{2.30}$$

in case of linear ionic drift, and:



(a)



(b)

Figure 2.17: Simulation results of applying a sinusoidal input of 1 volt to TEAM model. (a) shows the I-V characteristics, and (b) shows the change of the state variable with time.

$$i(t) = \frac{e^{-\left(\frac{\lambda}{w_{off}-w_{on}}\right)(w-w_{on})}}{R_{ON}}.v(t) \tag{2.31}$$

in case of nonlinear ionic drift.

2.3 Summary

As we presented above, models are developed rapidly in order to provide a predictive, compact, and accurate-enough model to maximize utilizing memristors. For the sake of referencing, another models based on different conduction mechanism was presented in [54, 55], however these models are not widely used. In the next chapter, we are going to enhance the Simmons tunneling model for similar electrodes by a new approach we propose.

Chapter 3

Memristor Modeling taking into account Trapezoidal Barrier

In this work, we consider a structure of a TiO_2 memristive device similar to HP lab ones [40]. We study the behavior of such device via analytic modeling and numerical simulation taking into considerations many several points and parameters not included in previously published work.

Pickett *et al.* [40] fabricated a titanium dioxide memristive device and studied its switching dynamics. Then later, Abdalla and Pickett [47] did SPICE simulations to that previously suggested device based on Simmons tunneling model for similar electrodes [46]. Although the tunneling phenomenon happens, in the suggested device [40], between two different electrodes, they assumed, in their simulation, two similar electrodes. Here we present a new approach, based on trapezoidal electron tunneling barrier, which provides a new model and improves the overall accuracy. In order to make our model more beneficial, we implemented a SPICE model to use it in any circuit simulator. The SPICE model is compact and simple as will be introduced in the following sections.

The memristor structure, suggested by [40] and [47], is shown in Fig. 3.1. It is composed of top and bottom electrodes made of Platinum, and a TiO_2 layer sandwiched between them. Upon *electroforming*, a conductive filament of TiO_{2-x}, which is very rich in oxygen vacancies, shunts most of the insulator thickness except for a width w. This insulating width, w, forms a potential barrier in front of electrons in the two conducting surrounding regions, namely; Pt and TiO_{2-x}. As w is thin enough, tunneling can take place between Platinum and the conducting filament TiO_{2-x} via TiO_2 insulator. Fig. 3.2 shows the band diagram of such layers at thermal equilibrium, where there exists a trapezoidal barrier to electrons tunneling between two asymmetric conductors, namely; Platinum and

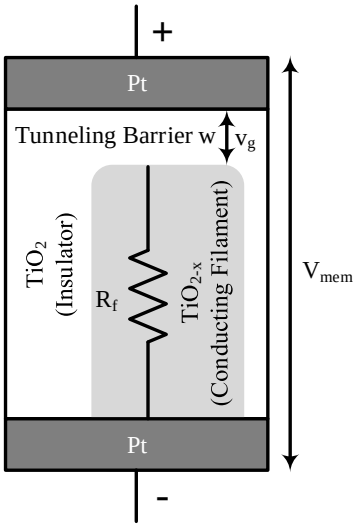


Figure 3.1: The device structure of the memristor. After an *electroforming* process [40], a filament is formed which is very rich in oxygen vacancies (TiO_{2-x}).

TiO_{2-x}. It is clear that the tunneling occurs between two different electrodes of different work functions which implies the importance of the new model. The tunneling width, w, changes according to the polarity of the applied voltage across the device.

The memristor behavior, as a non-linear time-varying device, can be modeled generally by the two coupled equations [8]:

$$i = G(w, v)v \tag{3.1}$$

$$\frac{dw}{dt} = f(w, i) \tag{3.2}$$

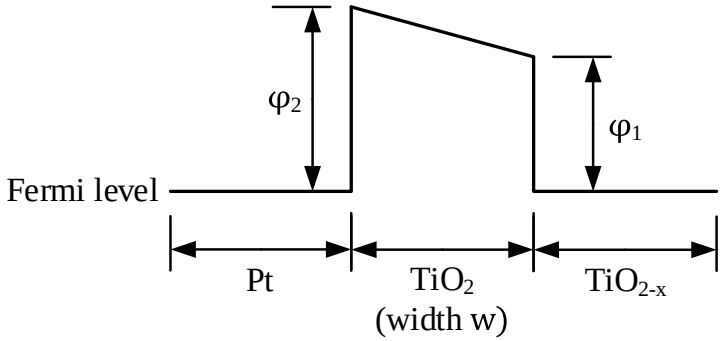


Figure 3.2: Energy Band Diagram of the memristor device at thermal equilibrium. Due to the different work functions of Platinum and TiO_{2-x}, a trapezoidal barrier arises. φ_2 and φ_1 are the barrier heights between Pt/TiO_2 and TiO_2/TiO_{2-x}respectively.

where i and v are the current through and voltage across the memristor, respectively. G is the generalized conductance and it depends on both the state variable w and the voltage across the device. The state variable w, the TiO_2 region width, is time-varying and its derivative is function of the current i and w itself [8]. For naming conventions, we will refer to the forward direction when the Platinum electrode, shown in Fig. 3.2, is positively biased, and the reverse direction when the Platinum electrode is negatively biased. The representations of eq. (3.2) for the forward and reverse directions are [47]:

1) Forward Direction:

$$\frac{dw}{dt} = f_{fb} \sinh\left(\frac{|i|}{i_{fb}}\right) \exp\left(-\exp\left(\frac{w - a_{fb}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right) \tag{3.3}$$

2) Reverse Direction:

$$\frac{dw}{dt} = f_{rb} \sinh\left(\frac{|i|}{i_{rb}}\right) \exp\left(-\exp\left(\frac{a_{rb} - w}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right) \tag{3.4}$$

where f_{fb}, f_{rb}, i_{fb}, i_{rb}, a_{fb}, a_{rb}, w_c, and b are the fitting parameters. These representations depend on the experimental results of the state variable in [40]. These results were analyzed and found that they exhibit very non linear behavior, which led to the double exponential dependence as shown in eq. (3.3) and (3.4).

In this chapter, we will focus on deriving the i-v relation shown in eq. 3.1 by modeling the trapezoidal barrier using two different techniques. First, we will solve 1-D time independent Schrödinger wave equation for the band diagram shown in Fig. 3.2, using Airy Functions [56], calculate the transmission probability, then, derive an expression for the current passing through the memristor. Second, we will apply Simmons tunneling model between dissimilar electrodes [57] to get an expression for the current passing through the memristor.

Later on, we will generalize the model by taking the capacitance of the tunneling barrier into consideration, by assuming a parallel plate capacitor between $Pt/TiO_2/TiO_{2-x}$.

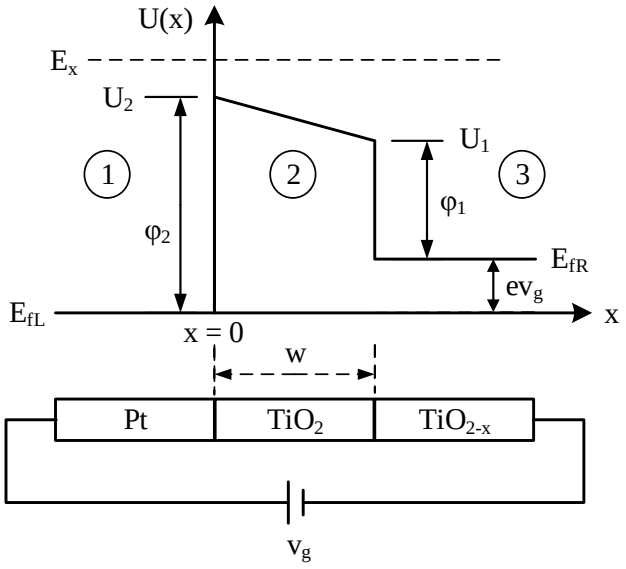


Figure 3.3: The band diagram of the memristor under bias $v_g$in the general case. E_{fL} and E_{fR} are the fermi level of Platinum and TiO_{2-x}, respectively.

3.1 Modeling using Airy Function

Fig. 3.3 shows the band diagram of the structure under bias. we are going to solve 1-D time independent Schrödinger wave equation in each of the three regions.

3.1.1 Solving 1-D time independent Schrödinger wave equation for the general case ($U_1 \neq U_2$)

1) Region 1 ($x < 0$):

The 1-D time independent Schrödinger wave equation in region 1 is:

$$\frac{-\hbar^2}{2m}\frac{d^2\Psi_1(x)}{dx^2} + U(x)\Psi_1(x) = E_x\Psi_1(x) \tag{3.5}$$

where $\Psi_1(x)$ is the wave function in region 1, m is the electron mass, $\hbar$ is the reduced Planck's constant, U(x) is the potential energy, and E_x is the energy of electron moving along the x-axis. Taking the platinum quasi-Fermi level E_{fL}, as the potential reference of the device, thus U(x) in this region equals zero. It follows that:

$$\frac{d^2\Psi_1(x)}{dx^2} = \frac{-2mE_x}{\hbar^2}\Psi_1(x) \tag{3.6}$$

We can write the spatial wave function $\Psi_1(x)$ in region 1 as:

$$\Psi_1(x) = A_1 e^{ik_1 x} + B_1 e^{-ik_1 x} \tag{3.7}$$

$$k_1 = \frac{\sqrt{2mE_x}}{\hbar} \tag{3.8}$$

where k_1 is the wave vector in region 1.

2) Region 2 ($0 < x < w$):

In this region, the potential is a linear function in x and it can be written as:

$$U(x) = U_2 + \frac{U_1 - U_2}{w} x \tag{3.9}$$

where U_2 and U_1 are the potential heights at $x = 0$ and $x = 1$, respectively, and ω is the width of TiO_2 region. In order to simplify the equation writing, let

$$F = \frac{U_1 - U_2}{w} \tag{3.10}$$

$$S = sgn(F) \tag{3.11}$$

Now, the 1-D time independent Schrödinger wave equation in region 2 can be rewritten as:

$$\frac{d^2\Psi_2(x)}{dx^2} - \frac{2m}{\hbar^2} S\,|F| \left(\frac{U_2 - E_x}{F} + x \right) \Psi_2(x) = 0 \tag{3.12}$$

where $\Psi_2(x)$ is the wave equation in region 2. We will solve the above equation using the transformation:

$$u(x) = S \sqrt[3]{\frac{2m}{\hbar^2}|F|} \left(\frac{U_2 - E_x}{F} + x \right) \tag{3.13}$$

Thus, eq. (3.12) can be rewritten as:

$$\frac{d^2\Psi_2(u)}{du^2} - u\Psi_2(u) = 0 \tag{3.14}$$

This is the well known Airy differential equation [56] and its solution can be described in terms of the Airy functions as:

$$\Psi_2(x) = A_2 Ai(u(x)) + B_2 Bi(u(x)) \tag{3.15}$$

where Ai and Bi are the Airy functions of the first and second kind, respectively [56].

3) Region 3 ($x > w$):

Similar to region 1, the spatial wave function $\Psi_3(x)$ in region 3 can be written as:

$$\Psi_3(x) = A_3 e^{ik_3 x} + B_3 e^{-ik_3 x} \tag{3.16}$$

$$k_3 = \frac{\sqrt{2m\left(E_x - ev_g\right)}}{\hbar} \tag{3.17}$$

where k_3 is the wave vector in region 3, e is the magnitude of electron charge, and v_g is the applied voltage. It's worth mentioning here that E_x spans all the possible values of energy for an electron tunneling along the x-axis. So, we have two cases: $E_x > ev_g$ (in this case k_3 will be real), or $E_x < ev_g$ (in this case k_3 will be imaginary). Both cases won't change the form of eq. 3.16 and are considered in the coding.

In order to derive the transmission probability, we need to apply the boundary conditions at the two interfaces in Fig. 3.3. Applying the continuity of the wave functions boundary condition at the two interfaces yields eq. (3.18) and (3.19) for the left and right interfaces respectively:

$$A_2 Ai(u_1) + B_2 Bi(u_1) = A_1 + B_1 \tag{3.18}$$

$$A_2 Ai(u_2) + B_2 Bi(u_2) = A_3 e^{ik_3 w} + B_3 e^{-ik_3 w} \tag{3.19}$$

while applying the mass multiplied spatial derivative $\left(i.e. \quad \frac{1}{m}\frac{d\Psi}{dx}\right)$ boundary condition, at the two interfaces yielded eq. (3.20) and (3.21) for the left and right interfaces respectively:

$$u^{\backslash}\left(A_2 Ai^{\backslash}(u_1) + B_2 Bi^{\backslash}(u_1)\right) = ik_1 (A_1 - B_1) \tag{3.20}$$

$$u^{\backslash}\left(A_2 Ai^{\backslash}(u_2) + B_2 Bi^{\backslash}(u_2)\right) = ik_3(A_3 - B_3) \tag{3.21}$$

where u_1 and u_2 are the evaluation of eq. (3.13) at *x=0* and *x=w*, respectively, and the '$\backslash$' symbol denotes the spatial derivative.

The previous four equations can be rewritten in the form of

$$\begin{pmatrix} A_1 \\ B_1 \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix}\begin{pmatrix} A_3 \\ B_3 \end{pmatrix} \tag{3.22}$$

where

$$\begin{aligned} \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} = C &\begin{pmatrix} 1 & \frac{m}{ik_1} \\ 1 & \frac{m}{ik_1} \end{pmatrix}\begin{pmatrix} Ai(u_1) & Bi(u_1) \\ \frac{u^{\backslash}}{m}Ai^{\backslash}(u_1) & \frac{u^{\backslash}}{m}Bi^{\backslash}(u_1) \end{pmatrix} \\ &\begin{pmatrix} Bi^{\backslash}(u_2) & -\frac{m}{u^{\backslash}}Bi(u_2) \\ -Ai^{\backslash}(u_2) & \frac{m}{u^{\backslash}}Ai(u_2) \end{pmatrix}\begin{pmatrix} e^{ik_3 w} & e^{-ik_3 w} \\ \frac{ik_3 e^{ik_3 w}}{m} & -\frac{ik_3 e^{-ik_3 w}}{m} \end{pmatrix} \end{aligned} \tag{3.23}$$

$$C = \frac{1}{2\left[Ai(u_2)Bi^{\backslash}(u_2) - Ai^{\backslash}(u_2)B_2 Bi(u_2)\right]} \tag{3.24}$$

3.1.2 Solving 1-D time independent Schrödinger wave equation for the special case ($U_1 = U_2$)

When the applied voltage $v_g = \varphi_2 - \varphi_1$, then the potential barrier will be flat as shown in Fig. 3.4. It follows that the solutions of the 1-D time independent Schrödinger wave equation in regions 1 and 3 are:

$$\Psi_1(x) = A_1 e^{ik_1 x} + B_1 e^{-ik_1 x}, \quad x < 0 \tag{3.25}$$

$$\Psi_3(x) = A_3 e^{ik_3 x} + B_3 e^{-ik_3 x}, \quad x > w \tag{3.26}$$

where

$$k_1 = \frac{\sqrt{2mE_x}}{\hbar} \tag{3.27}$$

$$k_3 = \frac{\sqrt{2m\left(E_x - ev_g\right)}}{\hbar} \tag{3.28}$$

For region 2, the solution depend on the following two cases:

1) $\mathbf{E_x \neq U_f}$

$$\Psi_2(x) = A_2 e^{ik_2 x} + B_2 e^{-ik_2 x}, \quad 0 < x < w \tag{3.29}$$

$$k_2 = \frac{\sqrt{2m\left(E_x - U_f\right)}}{\hbar} \tag{3.30}$$

and U_f is the potential barrier height in region 2. Again, E_x spans all the possible values of energy for an electron tunneling along the x-axis. So, we have three cases: $E_x < ev_g$ (in this case k_2 and k_3 will be imaginary), $ev_g < E_x < U_f$ (in this case k_2 will be imaginary and k_3 will be real), or $E_x > U_f$ (in this case k_2 and k_3 will be real). All the cases won't change the form of eq. (3.26) and eq. (3.29), and are considered in the coding.

In this case, eq. (3.23) takes the form:

$$\begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} = \frac{1}{4k_1k_2} \begin{pmatrix} k_1+k_2 & k_1-k_2 \\ k_1-k_2 & k_1+k_2 \end{pmatrix} \begin{pmatrix} (k_2+k_3)e^{i(k_3-k_2)w} & (k_2-k_3)e^{-i(k_2+k_3)w} \\ (k_2-k_3)e^{i(k_2+k_3)w} & (k_2+k_3)e^{i(k_2-k_3)w} \end{pmatrix} \tag{3.31}$$

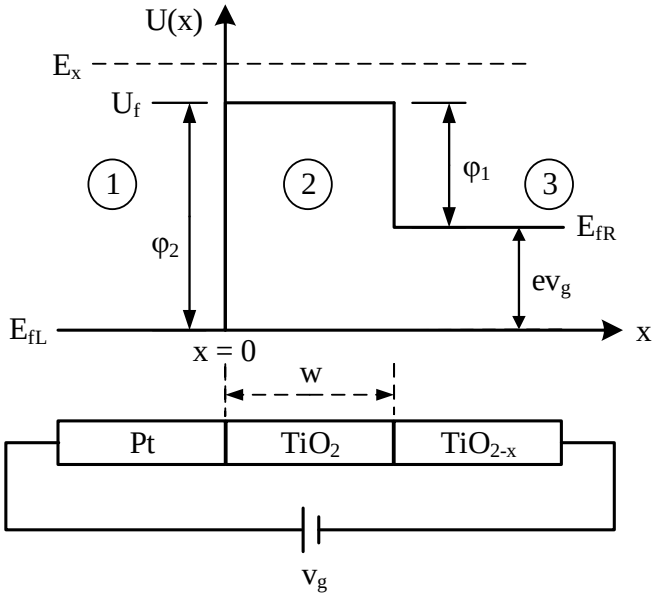


Figure 3.4: The band diagram of the memristor under bias v_g in the special case. E_{fL} and E_{fR} are the fermi level of Platinum and TiO_{2-x}, respectively.

2) $E_x = U_f$

In this case, the 1-D time independent Schrödinger wave equation becomes

$$\frac{-\hbar^2}{2m}\frac{d^2\Psi_2(x)}{dx^2} = 0, \quad 0 < x < w \tag{3.32}$$

$$\Psi_2(x) = A_2 + B_2 x \tag{3.33}$$

and eq. (3.23) becomes:

$$\begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} = \frac{-1}{2ik_1}\begin{pmatrix} -ik_1 & -1 \\ -ik_1 & 1 \end{pmatrix}\begin{pmatrix} (1-i\omega k_3)e^{ik_3\omega} & (1+i\omega k_3)e^{-ik_3\omega} \\ ik_3 e^{ik_3\omega} & -ik_3 e^{-ik_3\omega} \end{pmatrix} \tag{3.34}$$

3.1.3 Deriving the tunneling transmission probability

To get an expression for the tunneling transmission probability $T(E_x)$, we apply the following initial conditions. Electrons are incident from left (i.e. region 1) with $A_1 = 1$, and no reflected wave in region 3 (i.e. $B_3 = 0$). Thus

$$A_3 = \frac{1}{T_{11}} \tag{3.35}$$

$$T(E_x) = \left|\frac{k_3}{k_1}\frac{1}{|T_{11}|^2}\right| \tag{3.36}$$

where

$$T_{11} = \begin{cases} evaluated\ from\ eq.\ (3.23) & U_1 \neq U_2 \\ \frac{1}{2k_1}\left(k_1(1-iwk_3)+k_3\right)e^{ik_3 w} & U_1 = U_2, \quad E_x = U_f \\ \frac{1}{4k_1k_2}\Big\{(k_1+k_2)(k_2+k_3)e^{i(k_3-k_2)w} & \\ \quad +(k_1-k_2)(k_2-k_3)e^{i(k_3+k_2)w}\Big\} & U_1 = U_2, \quad E_x \neq U_f \end{cases}$$

In order to calculate current density J, we use the formula [58]:

$$J = \frac{4\pi me}{h^3}\int_0^{E_m} T(E_x)\left[\int_0^{\infty}\left\{f_1(E) - f_3\left(E - ev_g\right)\right\}dE\right]dE_x \tag{3.37}$$

where E is the total energy of the electrons, f_1 and f_3 are the Fermi-Dirac distributions at region 1 and region 3, respectively. The current passing through the memristor is:

$$i = J.A \tag{3.38}$$

where A is the cross sectional area of the filament shown in Fig. (3.1).

3.2 Modeling using Simmons Tunneling Model for Dissimilar Electrodes

3.2.1 Proposed technique

The current is modeled upon the WKB approximation [57] of tunneling probability for dissimilar electrodes.

The equations governing the tunneling current i through dissimilar electrodes are [57]:

1) Forward Direction:

$$i = \frac{eA}{2\pi h \Delta w^2}\left\{\overline{\varphi_2}e^{-B\sqrt{\overline{\varphi_2}}} + \left(\overline{\varphi_2} + e\left|v_g\right|\right)e^{-B\sqrt{\overline{\varphi_2}+e\left|v_g\right|}}\right\} \tag{3.39}$$

$$\overline{\varphi_2} = \varphi_2 - \left(e\left|v_g\right| + \Delta\varphi\right)\left(\frac{w_1+w_2}{2w}\right) - \left(\frac{1.15\lambda w}{\Delta w}\right)\ln\left(\frac{w_2(w-w_1)}{w_1(w-w_2)}\right) \tag{3.40}$$

$$w_2 = w_1 + w\left(1 - \frac{9.2\lambda}{3\varphi_2 + 4\lambda - 2\left(e\left|v_g\right| + \Delta\varphi\right)}\right) \tag{3.41}$$

$$w_1 = \frac{1.2\lambda w}{\varphi_2} \tag{3.42}$$

2) Reverse Direction:

$$i = \frac{eA}{2\pi h \Delta w^2}\left\{\overline{\varphi_1}e^{-B\sqrt{\overline{\varphi_1}}} + \left(\overline{\varphi_1} + e\left|v_g\right|\right)e^{-B\sqrt{\overline{\varphi_1}+e\left|v_g\right|}}\right\} \tag{3.43}$$

$$\overline{\varphi_1} = \varphi_1 - \left(\left|ev_g\right| - \Delta\varphi\right)\left(\frac{w_1+w_2}{2w}\right) - \left(\frac{1.15\lambda w}{\Delta w}\right)\ln\left(\frac{w_2(w-w_1)}{w_1(w-w_2)}\right) \tag{3.44}$$

$$w_1 = \frac{9.2\lambda w}{3\varphi_1 + 4\lambda - 2\left(e\left|v_g\right| - \Delta\varphi\right)} - \frac{1.2\lambda w}{\varphi_2 - e\left|v_g\right|} \tag{3.45}$$

$$w_2 = w - \frac{1.2\lambda w}{\varphi_2 - e\left|v_g\right|} \tag{3.46}$$

where

$$\Delta w = w_2 - w_1, \quad \Delta\varphi = \varphi_2 - \varphi_1 \tag{3.47}$$

$$B = \frac{2\pi\Delta w\sqrt{2m}}{h}, \quad \lambda = \frac{e^2\ln(2)}{8\pi\varepsilon_r\varepsilon_o}w \tag{3.48}$$

and e is the electron charge, h is Planck's constant, A is the filament area of the memristor, m is the mass of the electron , v_g is the voltage drop across the tunnel barrier, ε is the dielectric constant of TiO_2, and φ_2 and φ_1 are the barrier height in electron volts of Pt/TiO_2 and TiO_2/TiO_{2-x} respectively. As shown, there are some differences between the equations governing the forward and reverse directions. This agrees with the nature of the asymmetric tunneling barrier and will be shown later in the simulation results.

Fig. 3.5a shows the symbol used for memristor. Since the device is asymmetric, a polarity is assigned to the symbol to indicate how it is connected in the circuit. The black rectangle replicates the Platinum electrode shown in Fig. 3.2. The device structure shown in Fig. 3.1 is modeled as a potential barrier in series with an ohmic resistance R_f, which represents the conducting filament. Fig. 3.5b shows this implementation, where the tunneling potential barrier is represented by a voltage controlled current source in series with a resistor R_f.

3.2.2 SPICE and Verilog-A Models

3.2.2.1 Simple Model

In this section, we are going to introduce a SPICE model for Simmons-based model to be used in any SPICE-based circuit simulator. Fig. 3.6 shows the circuit implementation of the proposed model. The memristor is best described by a Voltage Controlled Current Source (VCCS), which implements the current flowing through the memristor, in series with a resistor. $i_{forward}$ represents the current flowing in the forward direction, eq (3.39), while $i_{reverse}$ represents the current flowing in the reverse direction, eq (3.43). The voltage across the current sources represents the voltage drop across the tunneling barrier, v_g. The series resistor R_f represents the resistance of the conductive channel formed upon electroforming and the voltage across it is v_f.

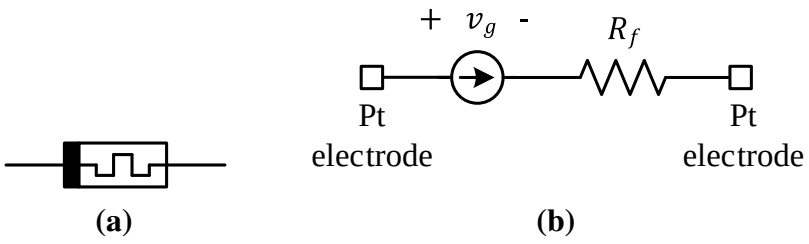


Figure 3.5: (a) The symbol of the memristor device. A polarity is assigned to the device to indicate its asymmetric behavior. (b) The circuit representing the device structure shown in Fig. 3.1.

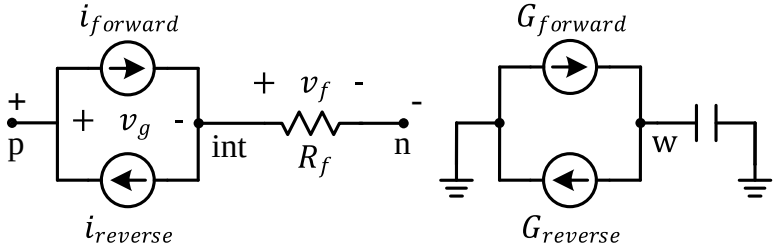


Figure 3.6: SPICE model of the proposed model.

The model is defined as a two-port device, namely **p** and **n**, while **int** is an internal node that is not accessible. The whole voltage across the memristor device is $v_g + v_f$. And since the voltage across a capacitor is the time integral of the current passing through it, the tunnel barrier width w can best be described by the voltage across a capacitor fed by current sources. $G_{forward}$ represents the forward direction and eq (3.3), while $G_{reverse}$ represents the reverse direction and eq (3.4). The initial condition of w is implemented as the initial voltage of the capacitor. The value of the capacitor was set to 1 nF to represent w in nm. All the values of the other related parameters were adjusted to account for that condition.

3.2.2.2 Generalized Model

Since the tunneling region in Fig. 3.1 can be best described as an insulator (TiO_2) between two conductive layers (Pt and TiO_{2-x}), it can be modeled as a parallel plate capacitor whose capacitance is:

$$C(w) = \frac{\varepsilon_o \varepsilon_r A}{w} \tag{3.49}$$

where A is the filament area, w is the insulator width, ε_o is the free space permittivity, and ε_r is the relative permittivity of TiO_2. Since the internal state variable, w, changes over time, the capacitance is written as a function of that variable $C(w)$. Thus, the memristor can be modeled as VCCS in series with a resistor R_f, and in parallel with a capacitor C_{tun}, as shown in Fig. 3.7.

The SPICE and Verilog-A models of the simple and generalized models are given in appendix A in section A.1 and A.2, respectively.

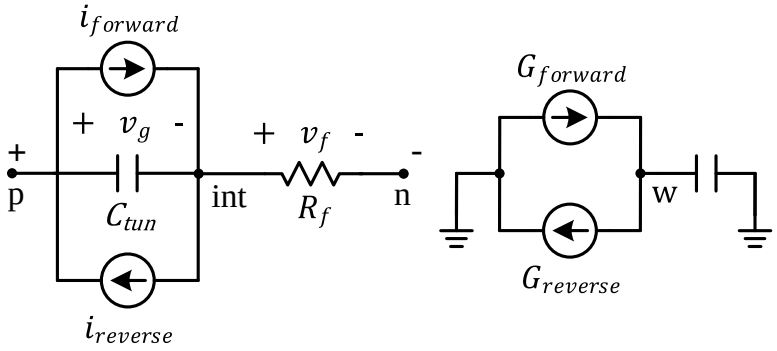


Figure 3.7: SPICE model of the proposed model.

Chapter 4

Model Verification and Circuit Simulations

This chapter is divided into two major sections. First, we are going to verify the models developed in chapter 3 against the experimental results of the TiO_2 memristor in [40]. In addition, we conduct a parametric study on some of the models parameters and discuss the results from a physical point of view. Second, the SPICE model is used to simulate some circuits published in the literature. The results obtained from these simulations are discussed and compared with their published counterparts.

4.1 Models Verification

In order to compare our models with the experimental results published in [40], the test circuit shown in Fig. 4.1 is used. This circuit represents the setup of the experiment in which the fabricated memristor is measured. The resistor R_c implements the electrode resistance of the device used in measuring the I-V characteristics of the memristor. The machine used for all simulations in this chapter has Intel Core i7 Processor running at 2.9 GHz and 8 GB of RAM.

4.1.1 Airy Function Based Model

The memristor in Fig. 4.1 is modeled by Airy function based model developed earlier, and the test circuit was excited by a +6V/-3V triangular waveform of 6 seconds period as shown in the inset of Fig. 4.2. φ_2 was set to 1.4 eV as in [59], φ_1 was varied from 0.2 eV to 0.65 eV and was chosen to be 0.6 eV.

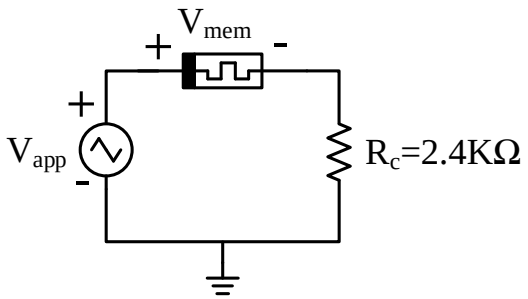


Figure 4.1: The test circuit used in validating the proposed models. The resistor R_c implements the electrode resistance of the experiment setup in [40].

The values for the parameters are f_{fb} = 3.5 μm, f_{rb} = 40 μm, i_{fb} = 115 μA, i_{rb} = 8.9 μA, a_{fb} = 1.2 nm, and a_{rb} = 1.8 nm [47]. The value of w_c was varied from 97 pm to 110 pm, and b was varied from 550 μA to 700 μA. However, it was found that w_c = 100 pm and b = 650 μA gives the best result. The simulation was done using MATLAB and the simulation took ~ 80 seconds. The initial condition for w was 1.2 nm and the time step was 5 ms.

Fig. 4.2 shows the I-V characteristics of the simulated circuit under the applied triangular voltage (shown in the inset). The figure shows a better matching between the proposed model, based on Airy function, (solid line) and the experimental results (black dots). Our model succeeded in capturing the behavior of the memristor, qualitatively and quantitatively, even in some ranges closer to experiments than HP's model (dashed line), especially in the third quadrant of the graph. However, the simulation time of our model is almost triple that of HP's model. As an explanation, our model, based on airy function, is slow because it takes a lot of time in multiplying huge matrices to calculate the transmission probability (such as eq. 3.23).

4.1.2 Simmons Tunneling between Dissimilar Electrodes Based Model

The memristor in Fig. 4.1 is modeled by Simmons tunneling model between dissimilar electrodes, and the test circuit was excited by a +6V/-3V triangular waveform of 6 seconds period as shown in the inset of Fig. 4.3. φ_2 was set to 1.4 eV as in [59], φ_1 was varied from 0.2 eV to 0.65 eV and was chosen to be 0.6 eV. The value of ε was set to 5 as in [40]. The value of the filament area A was varied from 0.9×10^4 nm^2 to 2.1×10^4 nm^2, and was chosen to be 2×10^4nm^2 which doesn't vary much from the extreme mentioned in [40].

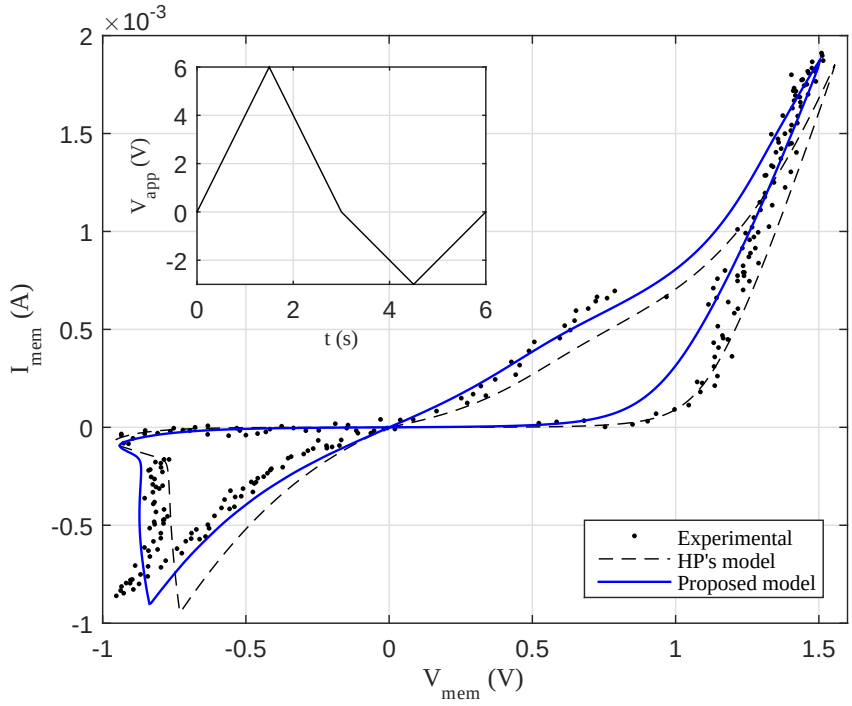


Figure 4.2: The I-V characteristics of the memristor device based on Airy function model. It shows the simulated I-V curve of HP's model (dashed line) [47], the simulated I-V curve of the proposed model (solid line), and the experimental results (dots) [40]. I_{mem} is the current through the memristor while V_{mem} is the voltage across it. The inset shows the waveform of the applied voltage signal.

The values for the parameters are f_{fb} = 3.5 μm, f_{rb} = 40 μm, i_{fb} = 115 μA, i_{rb} = 8.9 μA, a_{fb} = 1.2 nm, and a_{rb} = 1.8 nm [47]. The value of w_c was varied from 100 pm to 110 pm, and b was varied from 480 μA to 600 μA. However, it was found that w_c = 102 pm and b = 590 μA gives the best result. The simulation was done using MATLAB and the simulation took ~ 30 seconds. The initial condition for w was 1.2 nm and the time step was 2 ms.

Fig. 4.3 shows the I-V characteristics of the simulated circuit under the applied triangular voltage (shown in the inset). The figure shows a close matching between the proposed model (solid blue line) based on Simmons tunneling model for dissimilar electrodes and the experimental results (black dots). The new model succeeded in capturing the behavior of the memristor, qualitatively and quantitatively, even in some ranges closer to experiments than HP's model (solid black line), especially in the third quadrant of the graph. The simulation time of the new model is almost the same as that of HP's model, thus achieving higher accuracy with the same simulation time.

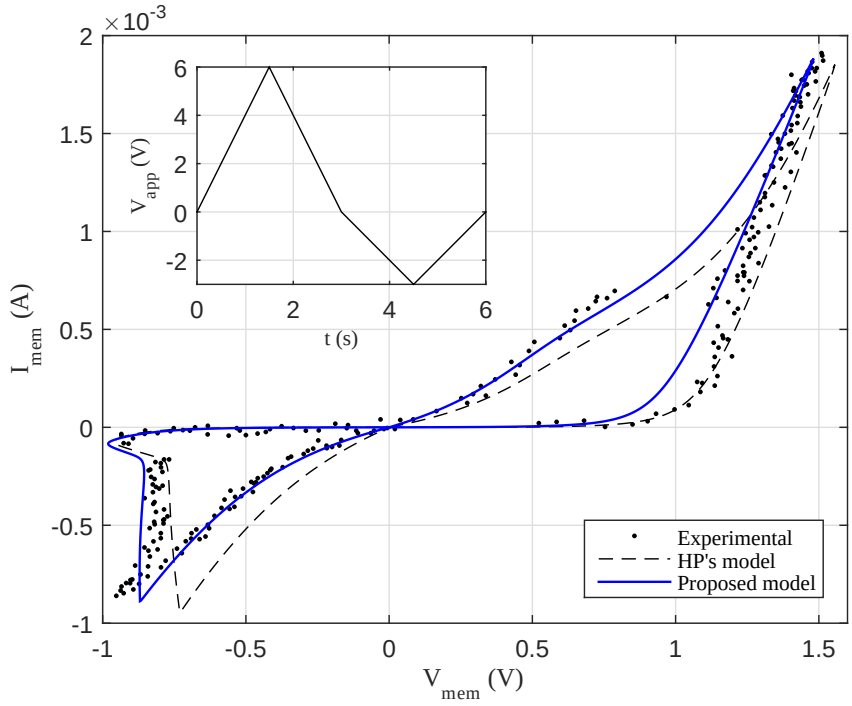


Figure 4.3: The I-V characteristics of the memristor device based on Simmons tunneling model for dissimilar electrodes. It shows the simulated I-V curve of HP's model (dashed line) [47], the simulated I-V curve of the proposed model (solid line), and the experimental results (dots) [40]. I_{mem} is the current through the memristor while V_{mem} is the voltage across it. The inset shows the waveform of the applied voltage signal.

In order to calculate the discrepancy between utilizing the trapezoidal barrier model and the rectangular barrier model, we adopted eq (4.1) to calculate the error between these two models:

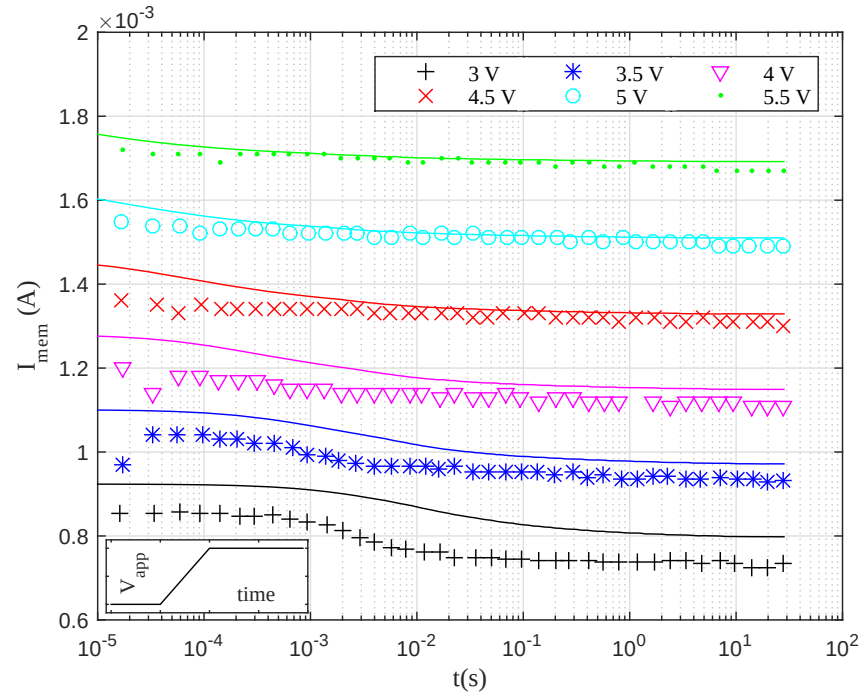
$$e = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\frac{\left|V_{i,RB}-V_{i,TB}\right|^2+\left|I_{i,RB}-I_{i,TB}\right|^2}{V_{i,TB}^2+I_{i,TB}^2}} \tag{4.1}$$

where e is the error between the two models, N is the number of samples, $V_{i,RB}$ and $V_{i,TB}$ are the voltage, referenced to 1 V, of the i-sample of the rectangular and trapezoidal barrier respectively, $I_{i,RB}$ and $I_{i,TB}$ are the current, referenced to 1 mA, of the i-sample of the rectangular and trapezoidal barrier respectively. The accuracy was improved by 12.1% upon using the trapezoidal barrier model.

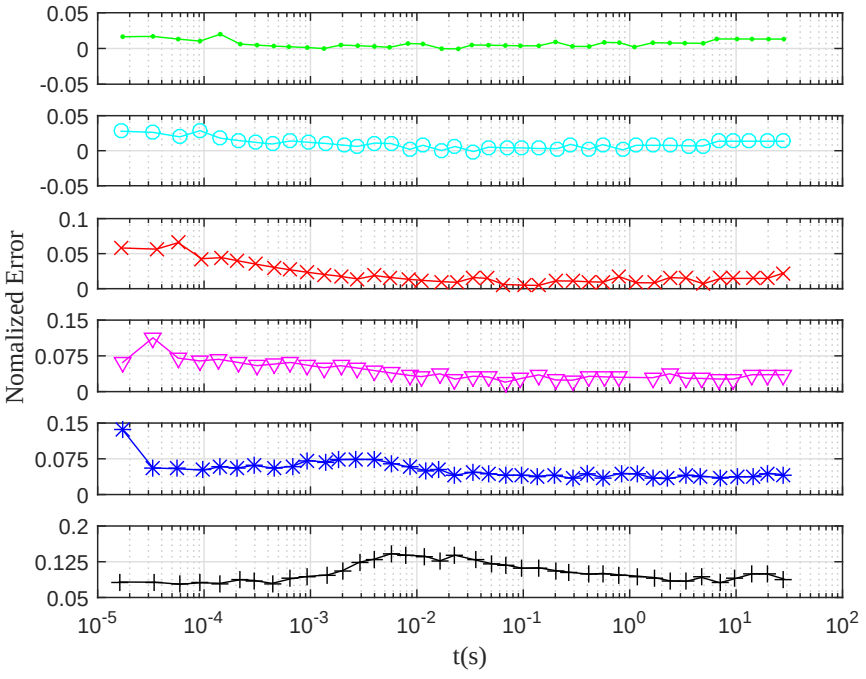
Fig. 4.4 shows the response of the memristor upon applying forward voltage steps of different amplitudes. The current through the memristor I_{mem} versus time for forward

steps is shown in Fig. 4.4a for six different voltage amplitudes. As we can see the simulated results (solid lines) approaches the experimental results (dots) as the magnitude of the voltage step is increased. The normalized error between experimental results and the new model versus time is shown in Fig. 4.4b, where the maximum error is about 12.5% when the voltage amplitude is 3V, and decreases as the voltage amplitude increases.

Fig. 4.5 shows the response of the memristor upon applying reverse voltage steps of different amplitudes. The current through the memristor I_{mem} versus time for reverse steps is shown in Fig. 4.5a for two different voltage amplitudes. As we can see the simulated results (solid lines) capture the behavior of the experimental data qualitatively, but it's not in a good agreement as in the forward steps. This is due to the highly nonlinearity associated with the reverse switching mechanism in eq. (3.4), where any small error in the current gets amplified quickly and causes the memristor to switch faster than it really does [47]. The normalized error between experimental results and the new model versus time is shown in Fig. 4.5b, where the maximum error is about 28% when the voltage amplitude is -1.4V.

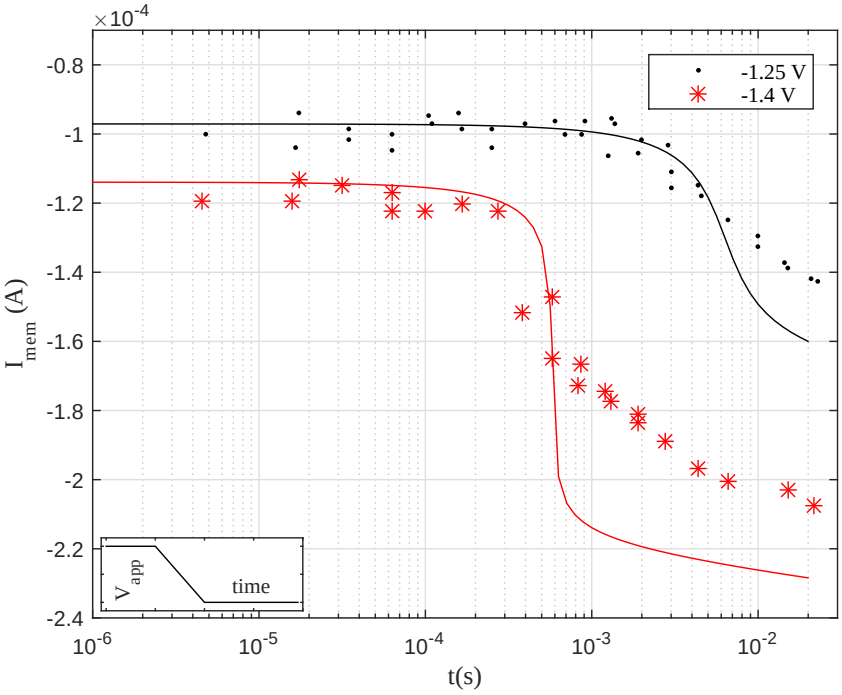


(a)

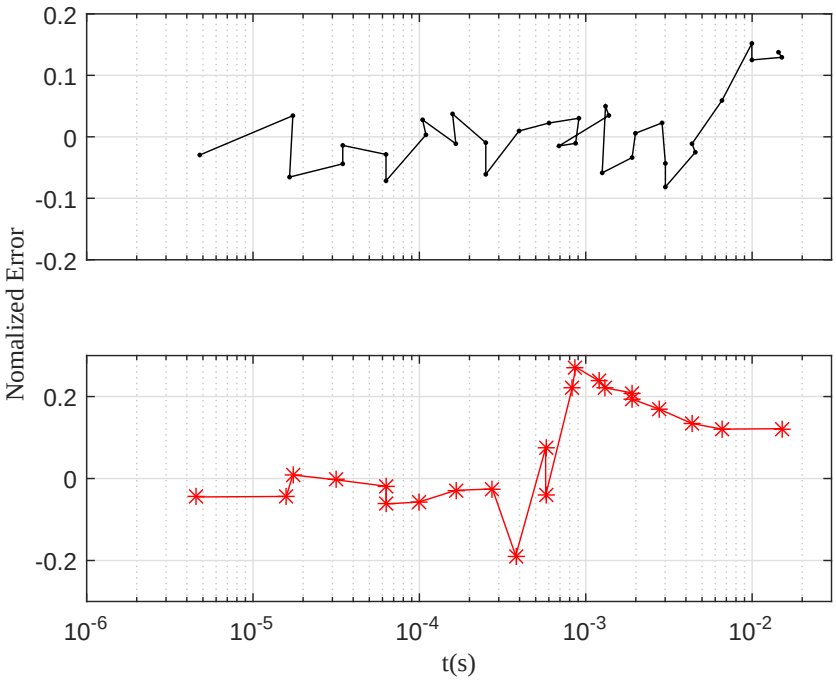


(b)

Figure 4.4: (a) The memristor response to forward voltage steps of different amplitudes (100 ns rise time). I_{mem} is the current through the memristor. The solid line represents the proposed model and the dots represents the data published in [40]. The inset shows a sketch of the applied voltage. (b) The normalized error between experimental data and our model.



(a)



(b)

Figure 4.5: (a) The memristor response to reverse voltage steps of different amplitudes (100 ns rise time). I_{mem} is the current through the memristor. The solid line represents the proposed model and the dots represents the data published in [40]. The inset shows a sketch of the applied voltage. (b) The normalized error between experimental data and our model.

4.2 Parametric Study

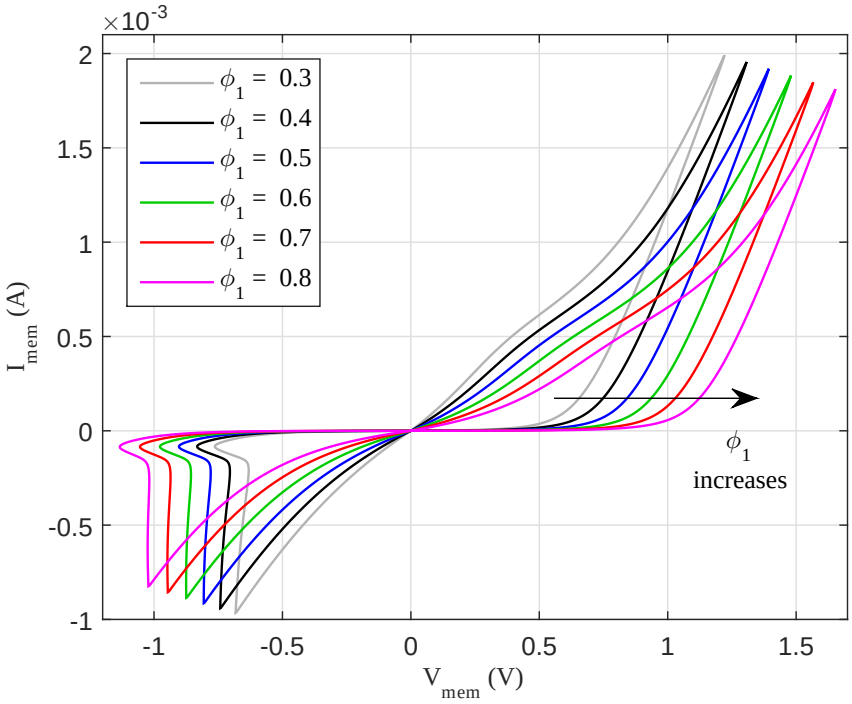
In this section we are going to study the effect of some parameters, such as: tunneling barrier height, and input signal frequency, shape, amplitude, on the I-V characteristics of the memristor.

4.2.1 Dependence of I-V Characteristics on φ_1 and φ_2

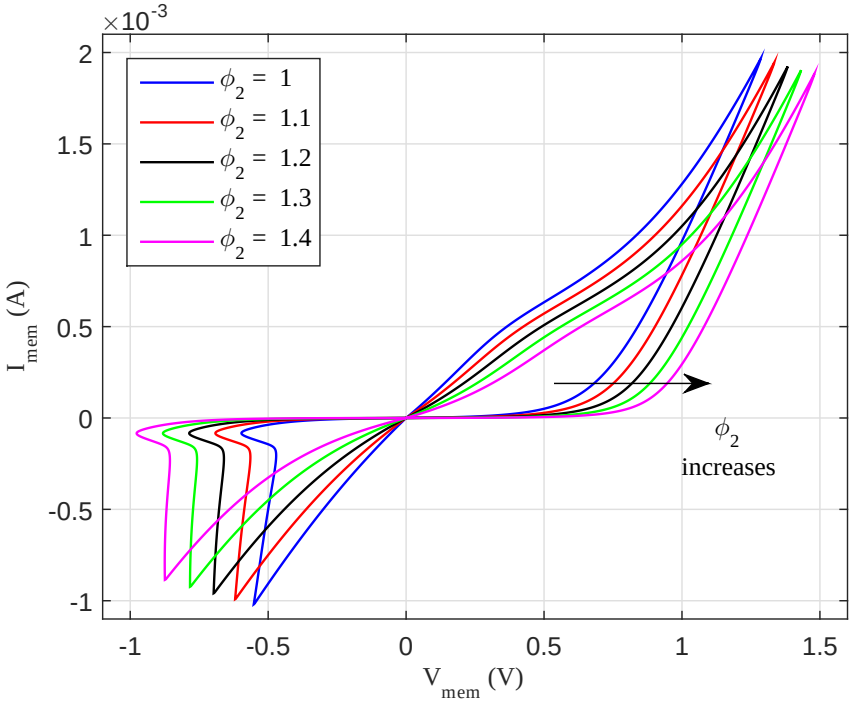
The dependence of the I-V characteristics on the barrier height, φ_1, at the TiO_2/TiO_{2-x} interface, (shown in Fig. 3.2), is studied. It has been proved before [59] that the Fermi-level depends strongly on the number of oxygen vacancies in TiO_{2-x}. Therefore, increasing the number of oxygen vacancies in TiO_{2-x} filament makes it more conductive, and increases the barrier height at TiO_2/TiO_{2-x} interface. Fig. 4.6a shows the I-V characteristics for different values of φ_1. The results show that as we increase the barrier height, the whole memristor device tends to be more resistive. Tunneling in the trapezoidal barrier is assisted by the internal electric field due to different barrier heights. So, one of the possible explanation is that increasing the barrier height φ_1 makes the trapezoidal barrier approaches a rectangular one. It is much easier for the electrons to tunnel though a trapezoidal barrier than a rectangular one.

Since the number of oxygen vacancies depends on the amplitude of the applied voltage during the electroforming process, the amount of vacancies can be controlled to produce a certain I-V characteristics that matches characteristics needed for the end application. For example, in memory applications, memristors are usually fabricated in a crossbar array configuration, as shown in Fig. 4.7. The array before *electroforming* is shown in Fig. 4.7a. After *electroforming* with different amplitudes, we can get memristors with different characteristics, which are shown in red, blue, green in Fig. 4.7b. Thus, having memristors with different characteristics without any extra fabrication processes, which is considered an advantage in mass production. This also shows the advantage of the new model which can account for such variance in the device characteristics.

Fig. 4.6b shows the I-V characteristics for different values of φ_2. As in the case of φ_1, the device tends to be more resistive as we increase the barrier height φ_2. Changing the barrier height φ_2 corresponds to using different metal and/or different oxide other than platinum and TiO_2. Now we have two degree of freedoms that can be chosen to shape the I-V characteristics as we need exactly.

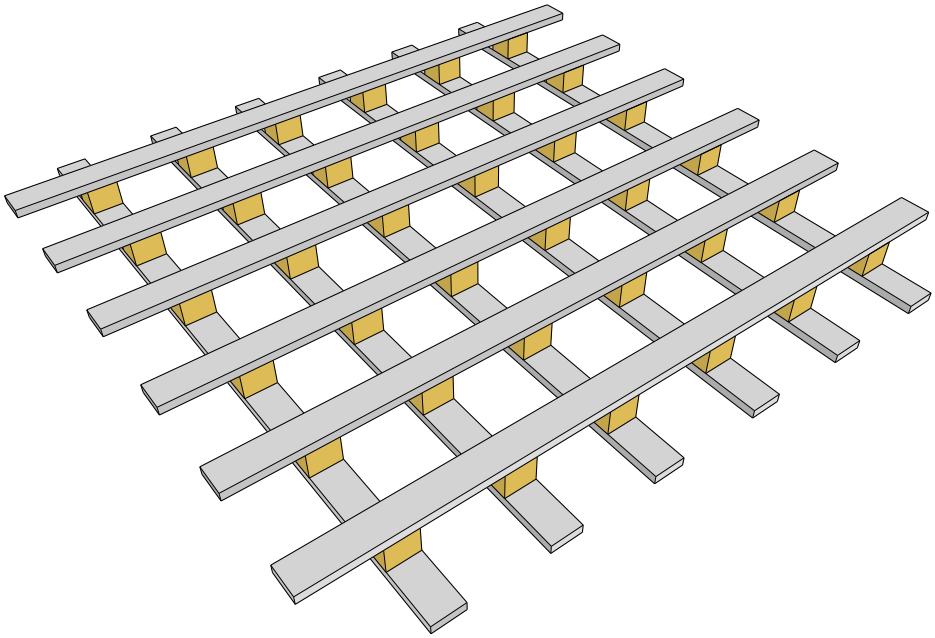


(a)

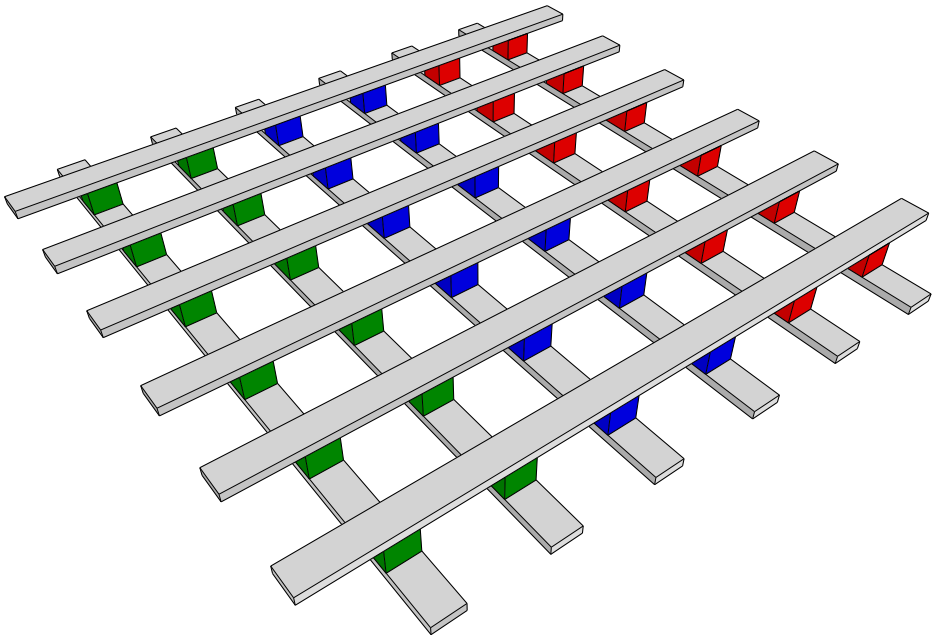


(b)

Figure 4.6: I-V characteristics for different φ_1 (a) and φ_2 (b). The arrow shows the direction where the φ_1 and φ_2 increases. This figure was produced using the circuit shown in Fig. 4.1, and the applied voltage was the inset of Fig. 4.3.



(a)



(b)

Figure 4.7: Crossbar array of memristors after fabrication (a) before electroforming (b) after electroforming with different pulse amplitudes giving different memristor characteristics.

4.2.2 Dependence of I-V Characteristics on Frequency

It is well known that the hysteresis disappears from the I-V characteristics of memristors at relatively high frequency [8]. In this section we are going to study the I-V characteristics dependence on frequency.

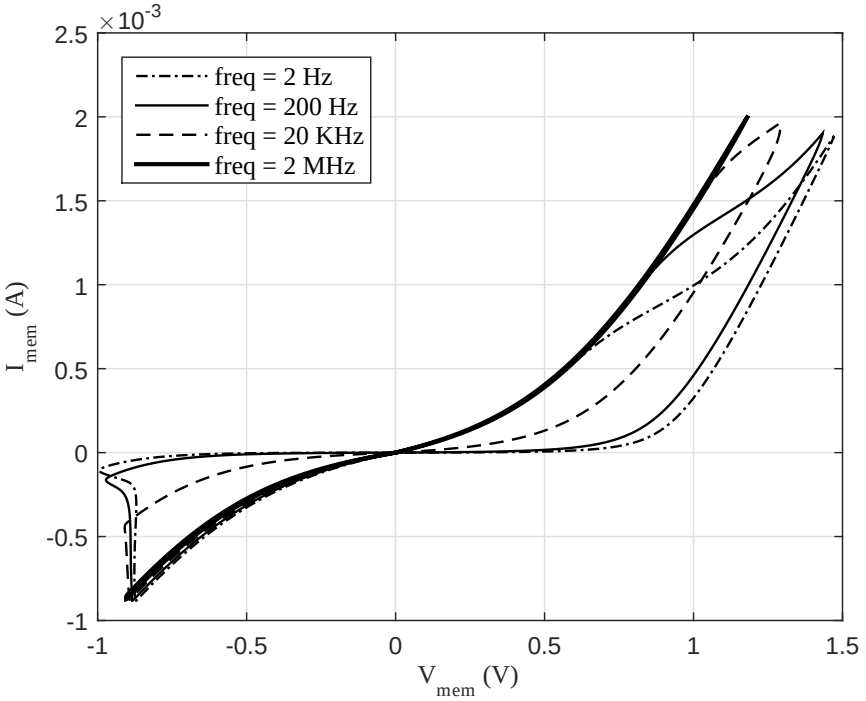
Fig. 4.8a shows the I-V characteristics for different frequencies from 2 Hz to 2 MHz. The applied voltage signal was the same as the inset of Fig. 4.3. The critical frequency, which the hysteresis vanishes above, was found to be about 2 MHz (solid line in Fig. 4.8a).

Fig. 4.8b shows the I-V characteristics for different frequencies from 10 Hz to 1 KHz for a sinusoidal input of amplitude 1 V. The critical frequency was found to be about 1 KHz (solid line in Fig. 4.8b).

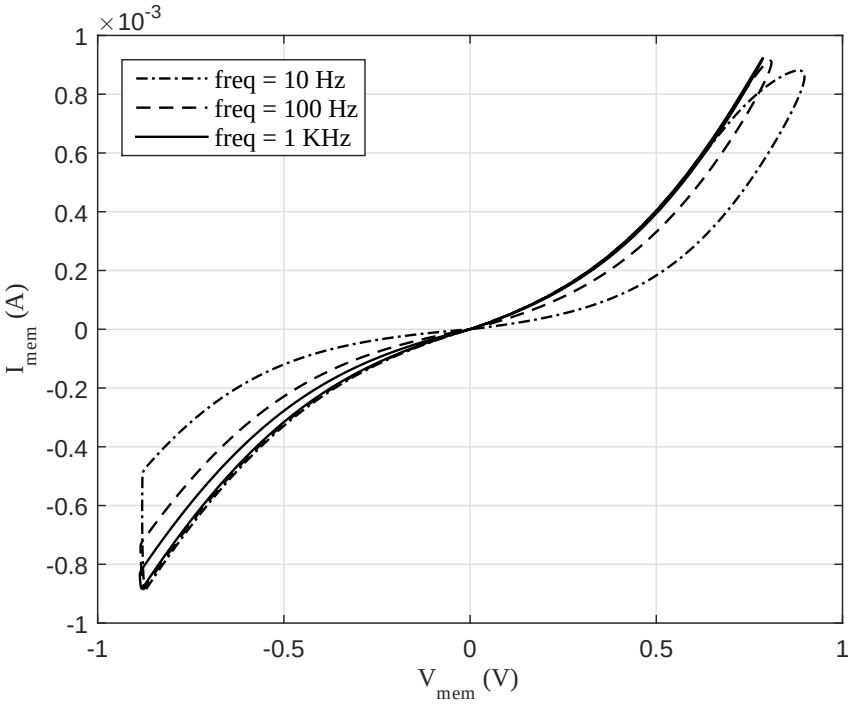
It can be deduced from Fig. 4.8 that the hysteresis loop and the critical frequency are both function of the applied signal shape and amplitude. Such property is very important to be extensively studied, especially for circuits designers who design circuits at high frequencies. It would help them decide the critical frequency at which their application will no longer behave as desired. Thus, we provide here a study for the critical frequency dependence on the applied voltage amplitude, for sinusoidal and triangular wave forms.

Fig. 4.9 shows the critical frequency f_c versus v_o for two applied voltage signals, as shown in the inset of Fig. 4.9a and 4.9b. The applied voltage amplitude is varied and the critical frequency, at which the hysteresis vanishes, is measured. Although both figures show exponential dependence on v_o, the slope of Fig. 4.9b is about triple that of Fig. 4.9a.

As an explanation, for the same v_o the frequency components of the triangular wave, as expanded by Fourier series, is higher than that of the sinusoidal wave, which is single tone. Thus, the hysteresis vanishes in the triangular wave at lower f_c as opposed to the sinusoidal wave. The region below the curve in Fig. 4.9 represent the range of frequencies and voltages where there is a hysteresis in the I-V curve, while the region above the curve represents the range of frequencies and voltages where the hysteresis vanishes from the I-V curve. Such a conclusion will be very useful when discussing the circuit simulations.

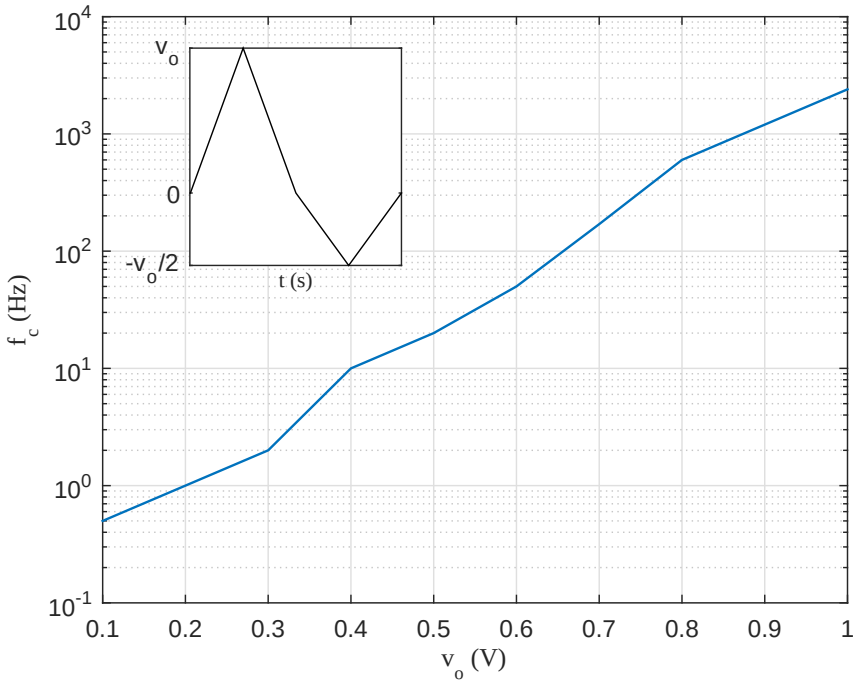


(a)

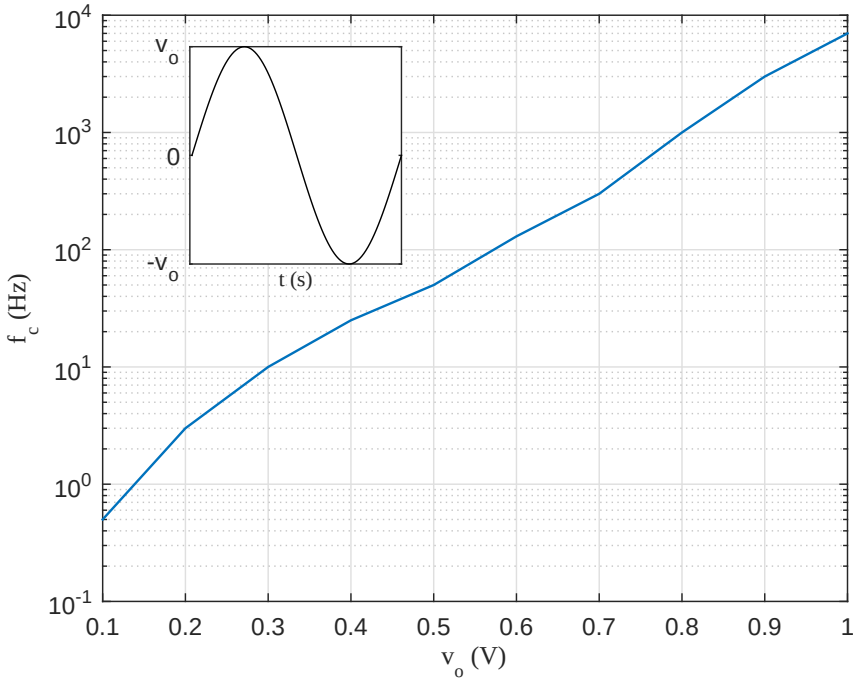


(b)

Figure 4.8: I-V characteristics for different frequencies for (a) a triangular wave, shown in the inset of Fig. 4.3, and (b) a sine wave of amplitude 3 V.



(a)



(b)

Figure 4.9: Critical frequency f_c versus applied voltage amplitude v_o for (a) a triangular wave and (b) a sine wave. The inset of both figures shows the wave form of the applied voltage.

4.3 Generalized Model Simulations

In this section, we are going to use the generalized model developed in chapter 3 in a frequency sweep simulation. A sinusoidal input of 2 volts amplitude is applied to the circuit shown in Fig. 4.1. It was found during the frequency sweep that there are three important regions that will be discussed next.

1. Hysteresis (Frequency Range 1 Hz to 25 MHz)

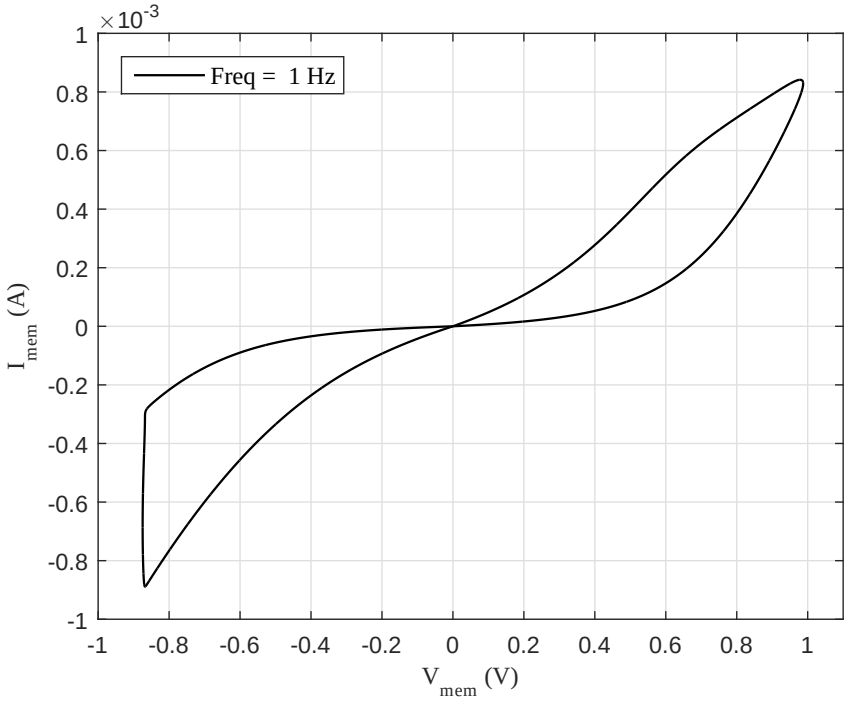
In this region, the I-V curves of the memristor is hysterical upon applying a sinusoidal input. Sample of these I-V curves is shown in Fig. 4.10 and 4.11. As can be deduced from Fig. 4.11a, the hysteresis in the first quadrant vanishes at about 2 KHz, while the hysteresis in the third quadrant still exists. This can be explained from the fact that for this particular device the reverse switching is faster than the forward switching, thus, the hysteresis during the reverse switching lasts longer until it completely vanishes at about 25 MHz as shown in Fig. 4.11b.

2. No Hysteresis (Frequency Range 25 MHz to 500 MHz)

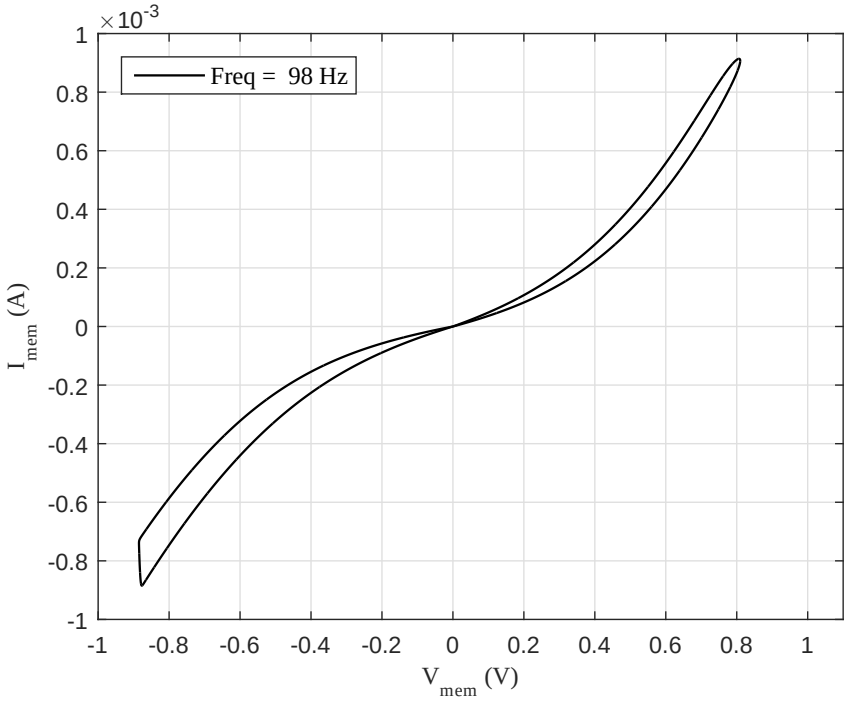
In this region, the hysteresis vanishes upon applying a sinusoidal input in the specified range. The I-V curve at 500 MHz is shown in Fig. 4.12. The memristor acts as a nonlinear resistance, which its current is exponentially dependent on the applied voltage.

3. Capacitance effect (Frequency Range 500 MHz to 100 GHz)

In this region, the hysteresis loop in the I-V curves of the memristor appears again but this time not passing by the origin indicating the presence of a capacitance. Sample of these I-V curves is shown in Fig. 4.13 and Fig. 4.14. It is well known that the I-V curve of an ideal capacitor is a circle with its center at the origin, while the I-V curve of a capacitor in parallel with a resistor is an ellipse. The inclination and shape of this ellipse depends on the value of the capacitor and resistor. It can be deduced from Fig. 4.14a and Fig. 4.14b that the memristor in this region can be modeled as a non-linear resistor in parallel with a varying capacitor (its value changes according to the value of the internal state variable w). From the inclination and the shape of the loop, one can deduce that the memristor behavior is dominant by the value of the non-linear resistor. The loop passes by the origin only at start up due to the zero initial conditions.

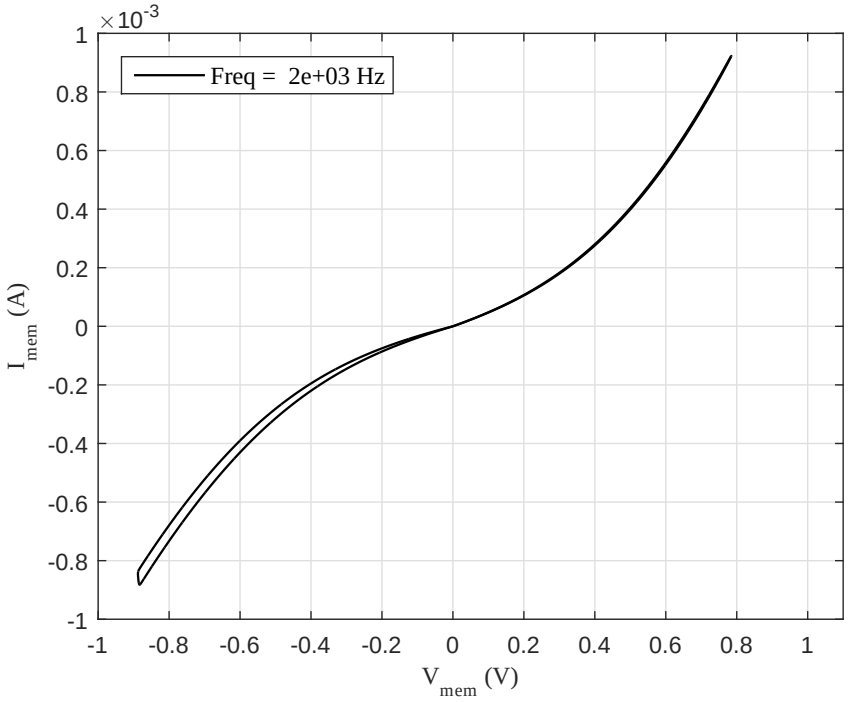


(a)

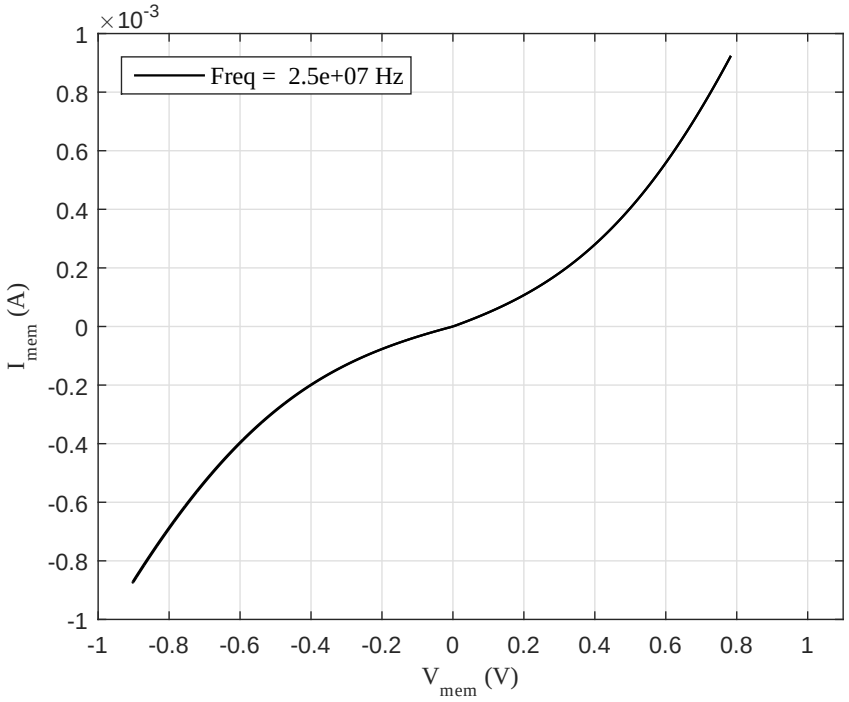


(b)

Figure 4.10: Frequency sweep from 1 Hz to 25 MHz for a sinusoidal input of 2 volt amplitude. (a) 1 Hz, (b) 98 Hz.



(a)



(b)

Figure 4.11: Frequency sweep from 1 Hz to 25 MHz for a sinusoidal input of 2 volt amplitude. (a) 2 KHz, (b) 25 MHz.

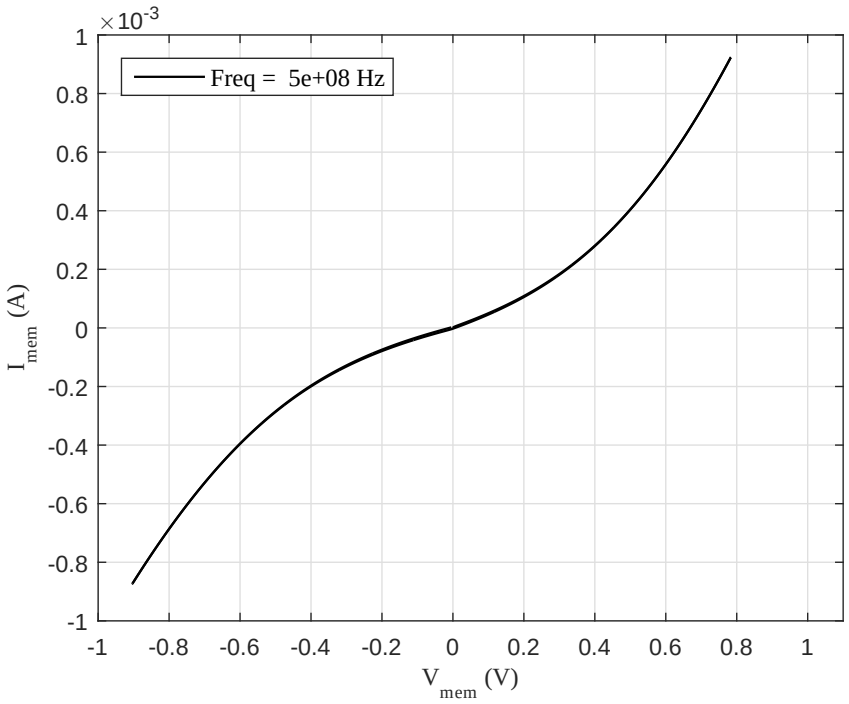


Figure 4.12: Frequency sweep from 25 MHz to 500 MHz for a sinusoidal input of 2 volt amplitude.

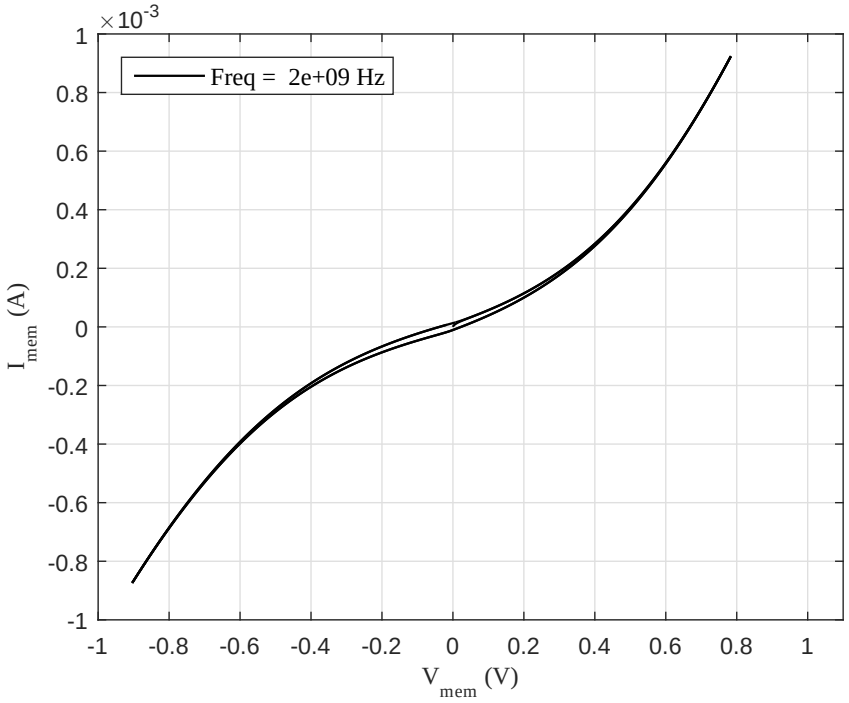
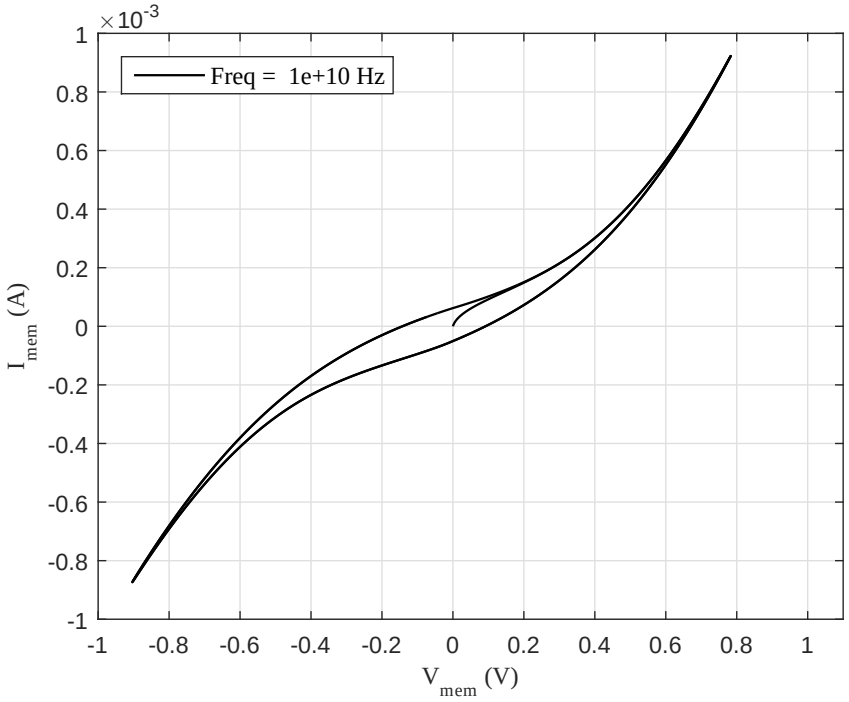
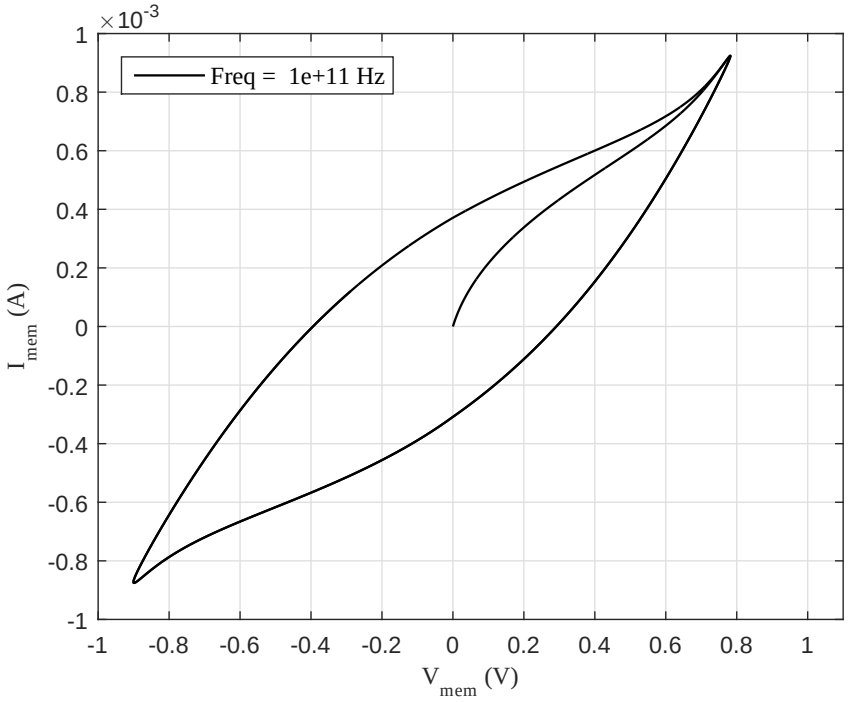


Figure 4.13: Frequency sweep from 500 MHz to 100 GHz for a sinusoidal input of 2 volt amplitude.



(a)



(b)

Figure 4.14: Frequency sweep from 500 MHz to 100 GHz for a sinusoidal input of 2 volt amplitude. (a) 10 GHz, (b) 100 GHz.

4.4 Circuit Simulation

In this section, we investigate oscillator circuits based on memristor. This oscillator is a subset of a family of oscillators named Memristor-Based Reactance-less Oscillators (MRLO) [22, 60]. The two configurations that were investigated are shown in Fig. 4.15. The concept of operation of these oscillators is based on the two distinct states of memristor, namely R_{ON} and R_{OFF}.

To quickly illustrate the circuit operation let us consider the circuit shown in Fig. 4.15a, where V_p and V_n are voltage references that control the operation (as will be shown later). Since the circuit has no input source, upon start up V_o will take a value of V_{oH} or V_{oL}, where V_{oL} here has to be a negative value. Assuming V_{oH} at the beginning, the memristor is forward biased and its internal state variable, w, starts to increase. Effectively, the total device becomes more resistive and the voltage drop across it increases. Thus, V_i drops down till $V_i < V_p$, at this moment $\mathrm{V_o}$ value switches to $\mathrm{V_{oL}}$. Now the memristor is reverse biased and its internal state variable, w, starts to decrease. Effectively, the total device becomes less resistive and the magnitude of the voltage drop across it decreases. Thus, magnitude of V_i keep rising till $|V_i| > |V_n|$, at this moment V_o value switches to V_{oH} and the loop continues. The same procedure can be applied on Fig. 4.15b. The input output relation of the two dashed blocks in Fig. 4.15a and 4.15b are shown in Fig.4.16a and 4.16b, respectively.

The previous work on MRLOs was done using the simple linear ionic drift model, mentioned in chapter 2, which is expressed by eq. (2.2) and (2.3). Condition of oscillation, range of R, frequency and pulse width were determined in terms of R_{ON}, R_{OFF}, V_{oH}, V_{oL}, V_p, and V_n *[60]*. However, in our model, the I-V relation is exponential and there is no hard limit for the resistance as in the linear model. Moreover, V_i wave form, shown in Fig.

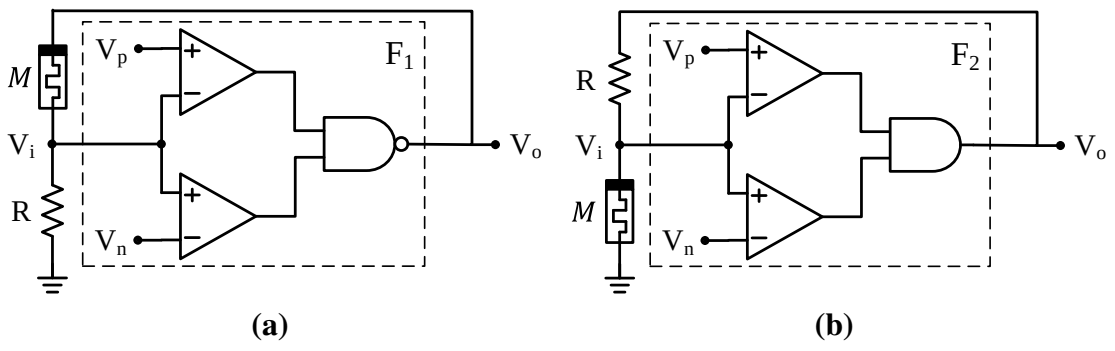


Figure 4.15: Two different configurations of MRLO.

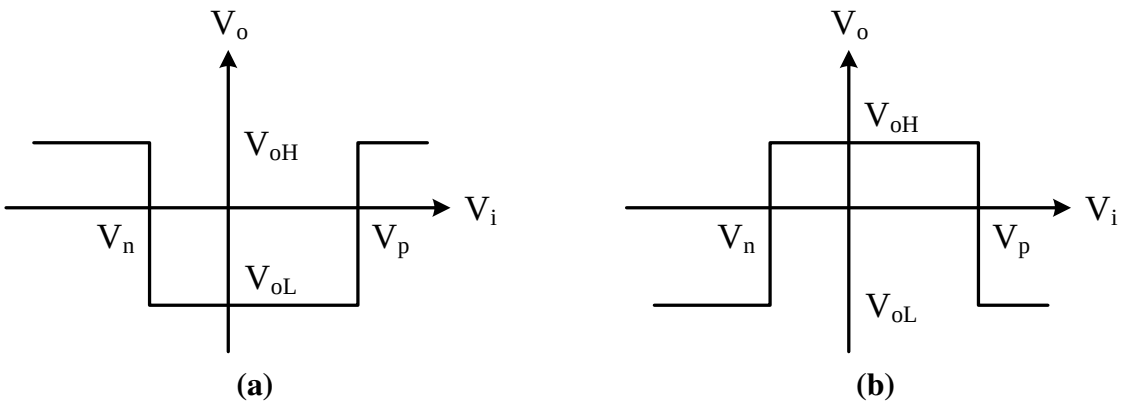


Figure 4.16: Input output relationship of the dashed blocks shown in Fig 4.15.

4.15a and 4.15b, depends strongly on the chosen R. Due to the complexity and coupling between the equations representing our model, discussed in chapter 3, closed expression for oscillation condition and different ranges are difficult to be deduced. However, here we present an alternative procedure to determine the conditions.

4.4.1 Alternative Design Procedure

For the sake of exposition, this procedure will be applied to the circuit shown in Fig. 4.15a. The first step of the design is to determine the desired parameters of the square wave, which are V_{oH}, V_{oL}, the frequency f_o, and the pulse width T_H. Now, for a certain R, the conditions for the oscillations to happen is:

$$V_{min}^{fb} < V_p < V_{max}^{fb} \tag{4.2}$$

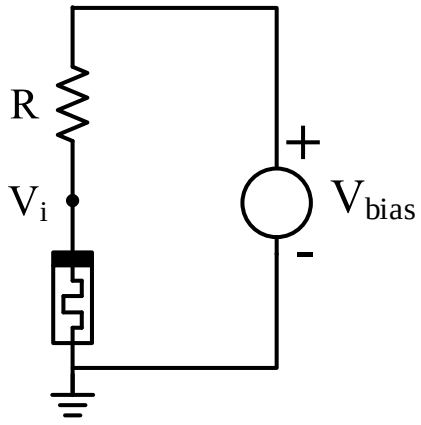
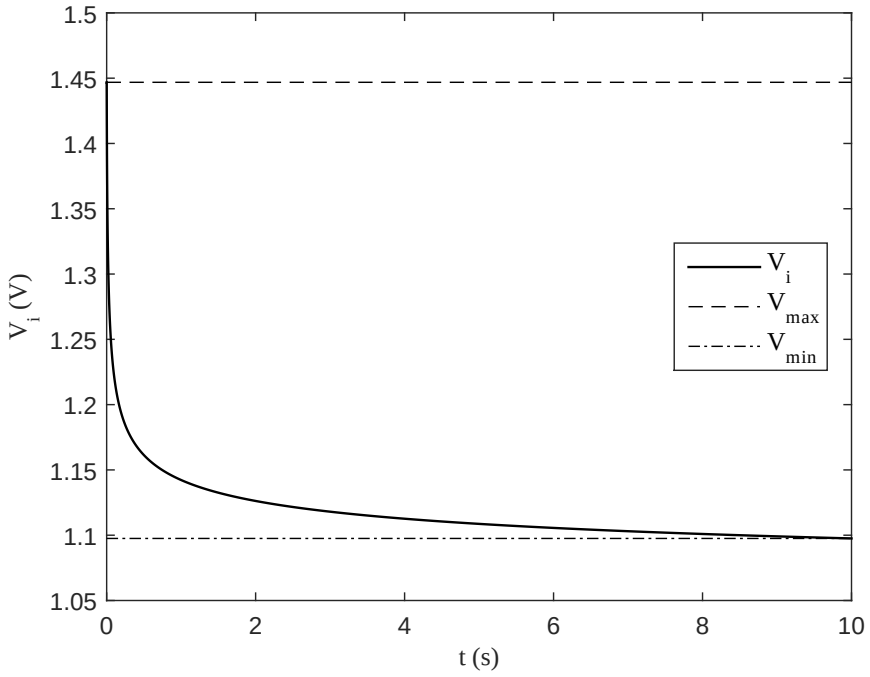
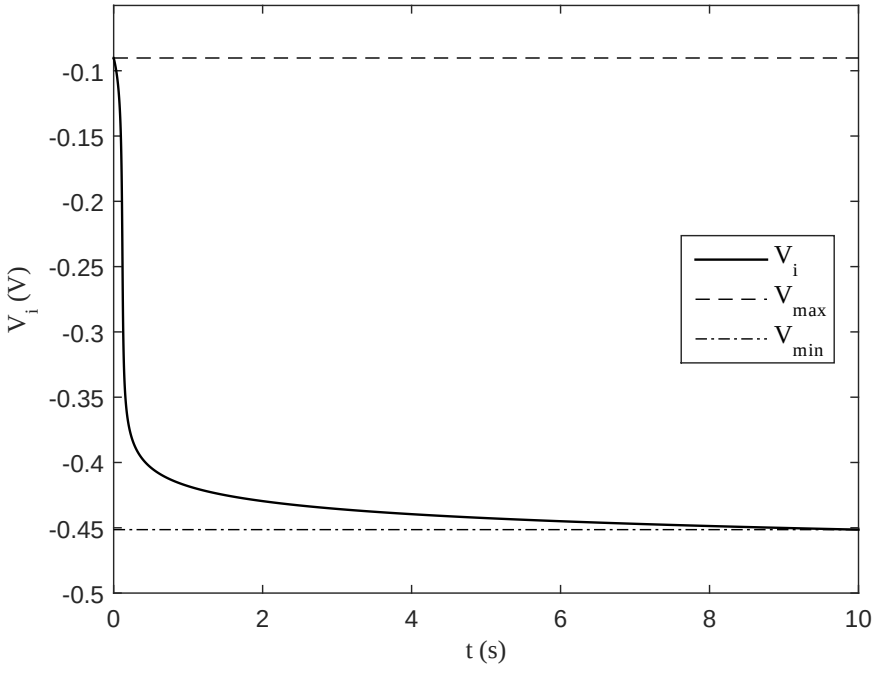


Figure 4.17: Test circuit to determine different design parameters.



(a)



(b)

Figure 4.18: DC bias for the circuit shown in Fig. 4.17 for R = 3 KΩ, and (a) V_{oH} = 2 V, (b) V_{oL}= -1 V.

$$V_{min}^{rb} < V_n < V_{max}^{rb} \tag{4.3}$$

where V_{min}^{fb}, V_{max}^{fb}, V_{min}^{rb}, and V_{max}^{rb} are shown in Fig. 4.18. The next step is to apply a square wave with the parameters chosen before, namely V_{oH}, V_{oL}, f_o, and T_H, and draw V_i versus time, as shown in Fig. 4.19. The values for V_p and V_n that will yield a square wave of the desired parameters are the values of V_i where high-to-low and low-to-high transitions happen respectively. Substituting the values of R, V_p, and V_n in the circuit shown in Fig. 4.15a will yield a square wave with the desired value chosen at the first step.These design steps are summarized in Fig. 4.20.

As an example of the proposed procedure, Fig. 4.21 shows the output voltage of the circuit shown in Fig. 4.15a for R = 3 KΩ, V_p = 1.2 V, V_n = -0.376 V, f_o= 10 Hz, V_{oH} = 2 V, and V_{oL}= -1 V. As can be deduced from the initial internal state variable, w, was 1.2 nm, which is the reason why the first pulse is wider than the others. The internal state variable keeps oscillating between 1.386 nm and 1.404 nm. The reason of choosing V_{oH} greater than V_{oL} is the forward switching dynamics is slower than the reverse switching [47]. Thus, we compensate that by increasing the V_{oH} value. To my best knowledge, no one else has investigated the use of practical models before in any circuit application. We

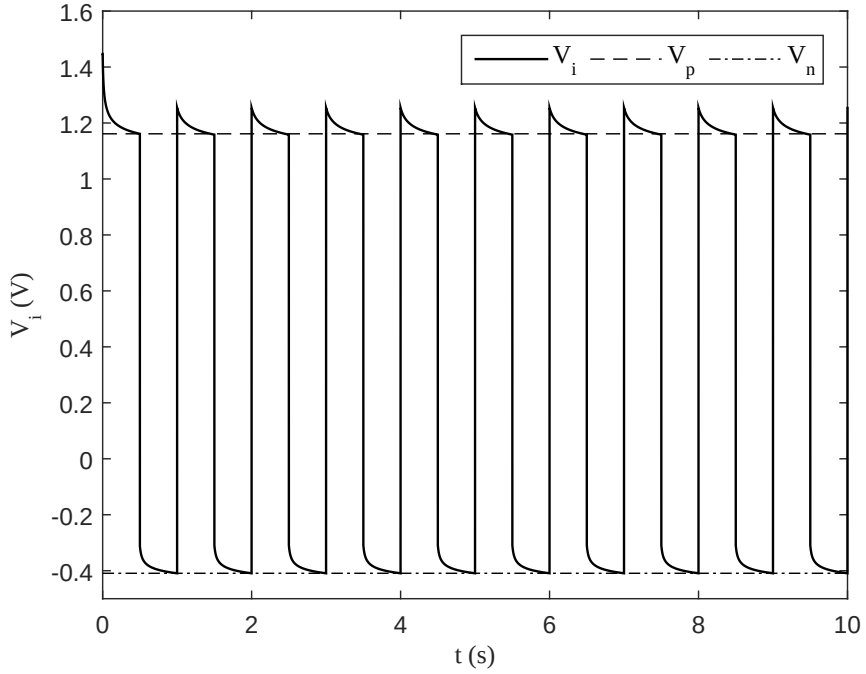


Figure 4.19: Input voltage versus time to determine the value of V_p and V_n.

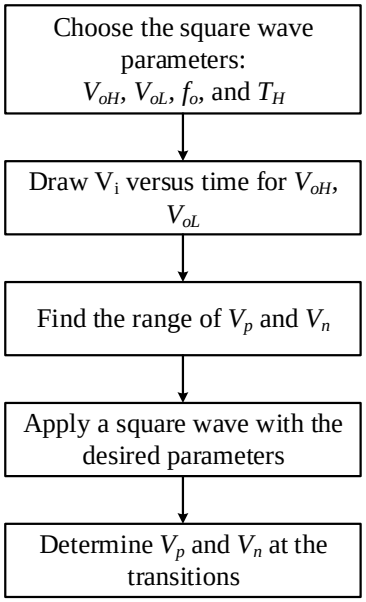


Figure 4.20: Design Procedure.

are the first to do so. I think the reason is that it takes more design steps and many trials before getting the circuit to work as desired.

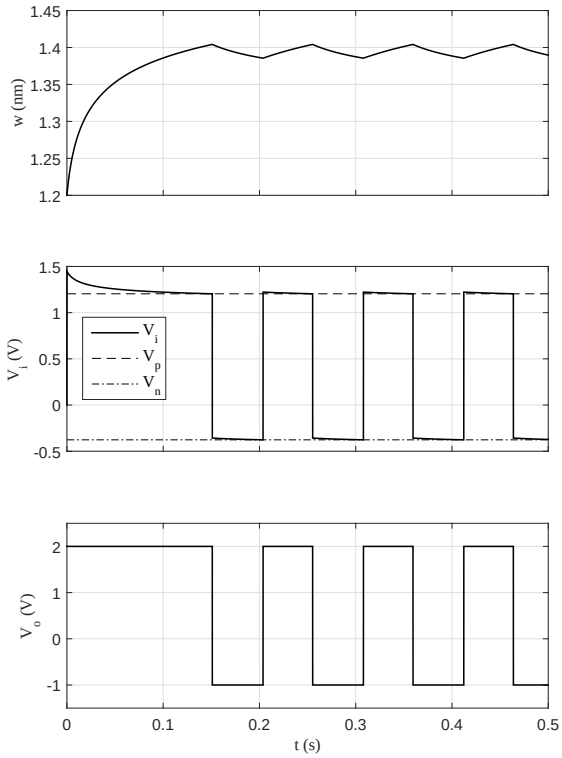


Figure 4.21: Results for applying the design procedure on circuit in Fig. 4.15a.

Fig. 4.22 shows the output voltage of the circuit shown in Fig. 4.15b for R = 3 KΩ, V_p = 0.838 V, V_n = -0.598 V, f_o= 1.31 Hz, V_{oH} = 2 V, and V_{oL}= -1 V. The internal state variable keeps oscillating between 1.363 nm and 1.45 nm. As shown, we have chosen the values of V_p and V_n such that square wave is asymmetric (i.e. $T_H > T_L$).

In order to link between the results obtained from the parametric study and the circuits simulations, we can find that the range of the voltage across the memristor in Fig. 4.22 is about 0.5 ~ 0.7 volts and the frequency is about 1 Hz. This point lies in the hysteresis region in Fig. 4.9, thus, the circuit functions correctly as an oscillator. In order to prove the validity of critical frequency curve, we will try to chose a point in the non-hysteresis region

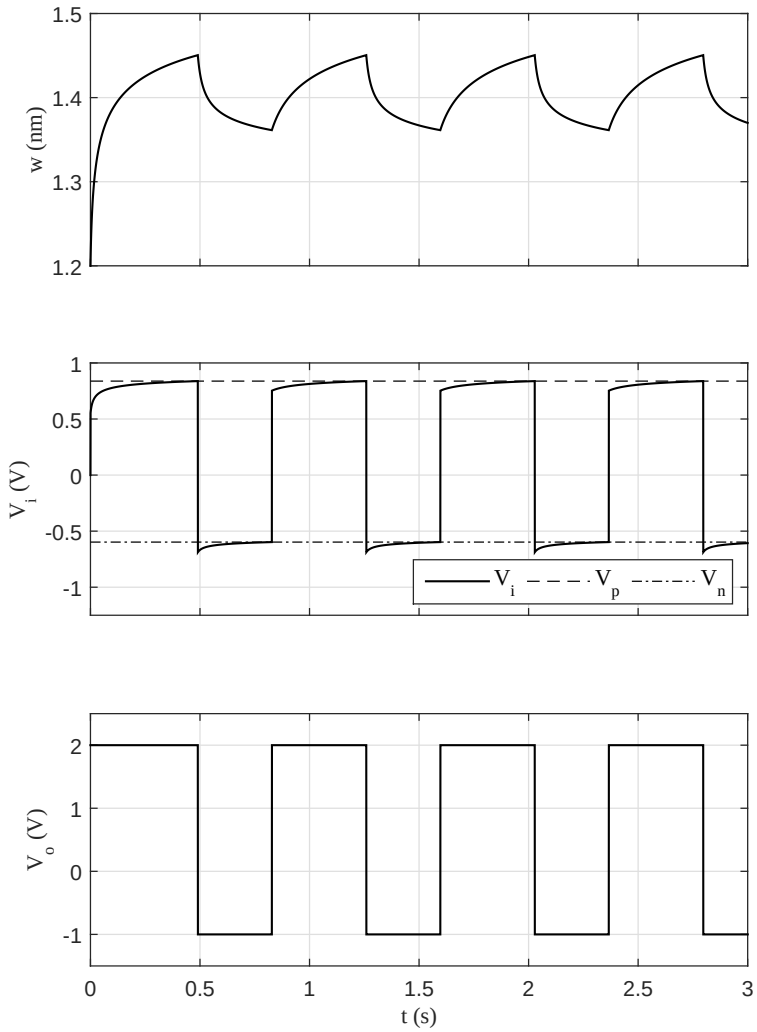


Figure 4.22: Results for applying the design procedure on circuit in Fig. 4.15b.

in the curve and the see the output of the oscillator. It is expected that the memristor will be behaving as a resistor in this region and that no oscillation will result. We will chose a frequency of 10 KHz and the voltage across the memristor will be the same as above (0.5 ~ 0.7 volts).

The results of such simulations is shown in Fig. 4.23 for R = 3 KΩ, f_o= 10 KHz, V_{oH} = 2 V, and V_{oL}= -1 V. As we can see, V_i remains constant as if we are using 2 resistors in series and, as a result, V_o remains constant at V_{oH} without any oscillations. The change in w is only 4 pm which is not negligible and what vary the memristor resistance.

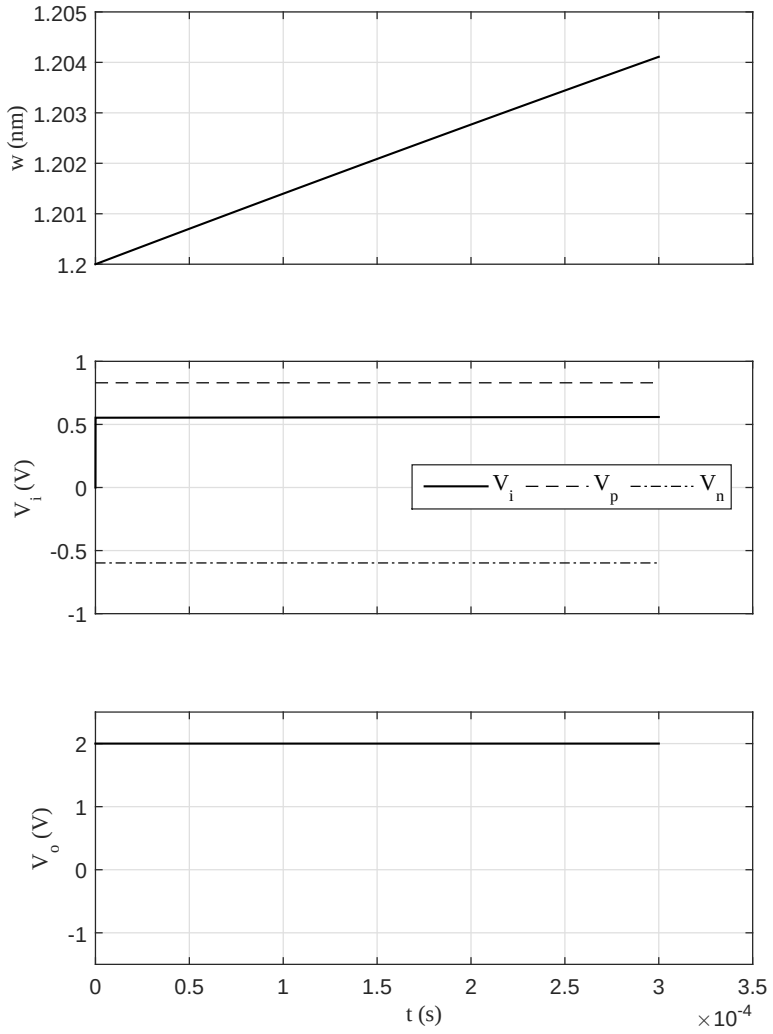


Figure 4.23: Results for applying the design procedure on circuit in Fig. 4.15b for a point in the non-hysteresis region.

Chapter 5

Conclusion and Future Work

5.1 Summary of Research

In this research, we investigate filament-based memristors, as a new emerging device. An overview of what are the memristors, their properties, types, potential applications are discussed in chapter 1. Chapter 2 discusses recent models of memristors and their advantage and disadvantages. In chapter 3, we introduce a new approach for modeling filament-based memristors taking into account trapezoidal electron tunneling barrier. This approach was solved using two different techniques, namely Airy function and Simmons tunneling model for dissimilar electrodes. The results of the tqo techniques were compared against each other and against experimental data showing reasonable agreement, even better than current modeling, as shown in Fig. 4.2 and Fig. 4.3. The accuracy versus previous models was improved by 12.1%.

Moreover, we did a parametric study on different parameters of the model to see their effect on the I-V characteristics. Increasing the barrier height would make the whole memristor device to be more resistive, while increasing the frequency of the applied signal makes the hysteresis loop in the I-V curve vanishes. In addition, we deduced an exponential dependence between the critical frequency, the frequency at which the hysteresis loop vanishes, and the applied voltage amplitude. We also found that this relation is not constant and depends on the shape of the applied voltage (sinusoidal, triangular, ...)

In addition, a SPICE model and Verilog-A code were implemented to be used with any compatible circuit simulator. This is crucial for circuit designers.

5.2 Thesis Contribution

Our contribution is as follows:

1. Two physical models based on different techniques were introduced. The models were verified against each other and against experimental results showing reasonable matching. The accuracy was improved from previous models by about 12.1%.

2. An extensive parametric study was done on different model parameters, such as: the potential barrier height, the shape, frequency, and amplitude of the applied input signal, to find out their effect on the I-V characteristics. Results and conclusion were derived from this study. To the writer best knowledge, no one has carried such an extensive study.

3. SPICE Model and Verilog-A code implementing Simmons tunneling model for dissimilar electrodes were introduced, for both the simple and generalized models. These models aids circuits designers to use memristors in different circuit simulators.

5.3 Future Work

Future work in memristive devices can be divided into three main branches. First, generalizing the state dynamics equations, shown in eq. 3.3 and 3.4. During my work, I was hindered by the state dynamics equation, which we only fitted for the device fabricated in [40]. As an expansion, these equations needs to be investigated more and generalized to account for other fabricated memristors based on different oxides such as Ta_2O_5. Thus, by combining these modified equations with the new model, the introduced model here can accommodate different types of devices.

Second, the memristors abilities to retain its last resistance value and not switching below certain threshold can be of great importance in the field of Digital-to-Analog Converters (DACs). In high speed DACs, a small mismatch between transistors could really degrade the performance of the system. In nowadays technologies, such mismatches always happen due to the small feature size and wafer degradation. As a result, compensation techniques always used to compensate for that mismatch and increase the overall performance of the system. However, these compensation techniques require a

huge chip area and power too. Fortunately, memristors can be very effective in this situation, where we could benefit from the above mentioned properties to compensate for the mismatch in the transistor elements. The reduction in the area and power would be huge as it might take up to only one memristor for each unit cell of DAC that needs compensation. This idea is novel and has not been investigated yet (to my best knowledge).

Third, The effect of the device dimensions on the filament area and the tunneling width. To illustrate more, Fig. 5.1 shows the studied device dimensions, the fabricated device area was $5 \times 5\ \mu m^2$ and the insulator thickness was $50\ nm$. The filament area was $\sim 2 \times 10^4\ nm^2$, while the tunneling width range was $\sim 2\ nm$. This was a micro-scale device fabricated for testing purposes, however, it is very important to study the effect of miniaturizing the device into the nano-scale dimensions. We need to find out what such a shrinkage would do on the filament area, and the tunneling width, and more important what it would do on the tunneling capacitance, especially at high frequencies. In addition, we need to study the effect of using another insulator than TiO_2 on the tunneling capacitance and the formulation of the filament. Whether changing the insulator material would change the filament resistance, or would change the ratio between the tunneling capacitance and the filament resistance, all these factors need to be studied extensively.

Finally, as mentioned before in chapter 1, memristors are part of a big family called memristive devices. This family also includes other elements with memory effect called meminductors and memcapacitors. Although these devices were investigated nowadays, however they lack proper and accurate modeling. So, there is an urgent need for finding a compact and accurate model for these devices that could mimic their behavior and be easily integrated in circuit simulators.

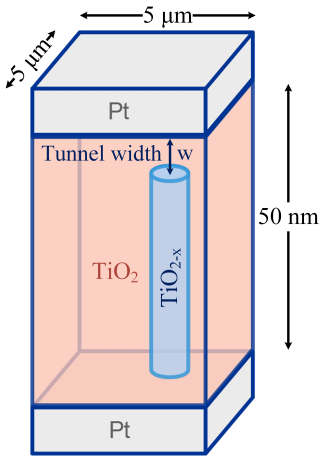


Figure 5.1: The studied device dimensions as published in [40].

References

[1] G. Moore, “Cramming More Components Onto Integrated Circuits,” *Electronics Magazine*, vol. 38, no. 8, 1965.

[2] S. E. Thompson and S. Parthasarathy, “Moore’s Law: The Future of Si Microelectronics,” *Materials Today*, vol. 9, no. 6, pp. 20–25, 2006.

[3] H. Esmaeilzadeh, E. Blem, R. St.Amant, K. Sankaralingam, and D. Burger, “Dark Silicon and The End of Multicore Scaling,” in *38th Annual International Symposium on Computer Architecture (ISCA)*, 2011, pp. 365–376.

[4] W. A. Wulf and S. A. McKee, “Hitting The Memory Wall: Implications of The Obvious,” *SIGARCH Comput. Archit. News*, vol. 23, no. 1, pp. 20–24, 1995.

[5] J. C. Yuan Xie and S. Sapatnekar, Eds., *Three Dimensional Integrated Circuit Design*. Springer US, 2010.

[6] L. Chua, “Memristor-The Missing Circuit Element,” *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507–519, 1971.

[7] L. Chua and S. M. Kang, “Memristive Devices and Systems,” *Proceedings of the IEEE*, vol. 64, no. 2, pp. 209–223, 1976.

[8] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The Missing Memristor Found,” *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[9] M. Di Ventra, Y. Pershin, and L. Chua, “Circuit Elements With Memory: Memristors, Memcapacitors, and Meminductors,” *Proceedings of the IEEE*, vol. 97, no. 10, pp. 1717–1724, 2009.

[10] L. O. Chua, “The Fourth Element,” *Proceedings of the IEEE*, vol. 100, no. 6, pp. 1920–1927, 2012.

[11] S. Kim, S. Choi, and W. Lu, “Comprehensive Physical Model of Dynamic Resistive Switching in an Oxide Memristor,” *ACS Nano*, vol. 8, no. 3, pp. 2369–2376, 2014.

[12] N. Ge, M.-X. Zhang, L. Zhang, J. J. Yang, Z. Li, and R. S. Williams, "Electrode-Material Dependent Switching in TaO_x Memristors," *Semiconductor Science and Technology*, vol. 29, no. 10, p. 104 003, 2014.

[13] Y.-E. Syu, T.-C. Chang, J.-H. Lou, T.-M. Tsai, K.-C. Chang, M.-J. Tsai, Y.-L. Wang, M. Liu, and S. M. Sze, "Atomic-level Quantized Reaction of HfO_x Memristor," *Applied Physics Letters*, vol. 102, no. 17, 172903, 2013.

[14] D.-q. Liu, H.-f. Cheng, G. Wang, X. Zhu, and Z.-z. Shao, "Memristive Properties of Transparent (La, Sr)MnO_3 Thin Films Deposited on ITO Glass at Room Temperature," *IEEE Electron Device Letters*, vol. 34, no. 12, pp. 1506–1508, 2013.

[15] S. Seo, M. J. Lee, D. H. Seo, E. J. Jeoung, D.-S. Suh, Y. S. Joung, I. K. Yoo, I. R. Hwang, S. H. Kim, I. S. Byun, J.-S. Kim, J. S. Choi, and B. H. Park, "Reproducible Resistance Switching in Polycrystalline NiO Films," *Applied Physics Letters*, vol. 85, no. 23, pp. 5655–5657, 2004.

[16] H. Barnaby, A. Edwards, D. Oleksy, and M. Kozicki, "Finite Element Modeling of Ag Transport and Reactions in Chalcogenide Glass Resistive Memory," in *IEEE Aerospace Conference*, 2013, pp. 1–10.

[17] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale Memristor Device as Synapse in Neuromorphic Systems," *Nano Letters*, vol. 10, no. 4, pp. 1297–1301, 2010.

[18] X. Wang, Y. Chen, H. Xi, H. Li, and D. Dimitrov, "Spintronic Memristor Through Spin-Torque-Induced Magnetization Motion," *IEEE Electron Device Letters*, vol. 30, no. 3, pp. 294–297, 2009.

[19] International Technology Roadmap of Semiconductors, 2013 Edition, Emerging Research Devices, [Online]. Available: http : / / www . itrs . net/ (visited on 03/24/2015).

[20] A. Afifi, A. Ayatollahi, and F. Raissi, "Implementation of Biologically Plausible Spiking Neural Network Models on the Memristor Crossbar-based CMOS/Nano Circuits," in *European Conference on Circuit Theory and Design*, 2009, pp. 563–566.

[21] Y. V. Pershin, S. La Fontaine, and M. Di Ventra, "Memristive Model of Amoeba Learning," *Phys. Rev. E*, vol. 80, no. 2, p. 021 926, 2009.

[22] M. A. Zidan, H. Omran, C. Smith, A. Syed, A. G. Radwan, and K. N. Salama, "A Family of Memristor-Based Reactance-Less Oscillators," *International Journal of Circuit Theory and Applications*, vol. 42, no. 11, pp. 1103–1122, 2014.

[23] M. E. Fouda, M. a. Khatib, A. G. Mosad, and A. G. Radwan, "Generalized Analysis of Symmetric and Asymmetric Memristive Two-Gate Relaxation Oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 10, pp. 2701–2708, 2013.

[24] T. Driscoll, J. Quinn, S. Klein, H. T. Kim, B. J. Kim, Y. V. Pershin, M. Di Ventra, and D. N. Basov, "Memristive Adaptive Filters," *Applied Physics Letters*, vol. 97, no. 9, p. 093 502, 2010.

[25] S. Jameel, C. Korasli, and A. Nacaroglu, "Realization of Biquadratic Filter by using Memristor," in *International Conference on Technological Advances in Electrical, Electronics and Computer Engineering (TAEECE)*, 2013, pp. 52–56.

[26] R. Williams, "How We Found The Missing Memristor," *Spectrum, IEEE*, vol. 45, no. 12, pp. 28–35, 2008.

[27] H. Kim, M. Sah, C. Yang, and L. Chua, "Memristor-Based Multilevel Memory," in *12th International Workshop on Cellular Nanoscale Networks and Their Applications (CNNA)*, 2010, pp. 1–6.

[28] K. Tsutsui, "Focus on Strengths and Weaknesses of ReRAM," in *Proceedings of the Flash Memory Summit*, 2013.

[29] M. A. Zidan, H. A. H. Fahmy, M. M. Hussain, and K. N. Salama, "Memristor-Based Memory: The Sneak Paths Problem and Solutions," *Microelectronics Journal*, vol. 44, no. 2, pp. 176–183, 2013.

[30] C.-M. Jung, J.-M. Choi, and K.-S. Min, "Two-Step Write Scheme for Reducing Sneak-Path Leakage in Complementary Memristor Array," *Nanotechnology, IEEE Transactions on*, vol. 11, no. 3, pp. 611–618, 2012.

[31] M. Zidan, A. Eltawil, F. Kurdahi, H. Fahmy, and K. Salama, "Memristor Multiport Readout: A Closed-Form Solution for Sneak Paths," *Nanotechnology, IEEE Transactions on*, vol. 13, no. 2, pp. 274–282, 2014.

[32] B. Abdoli, A. Amirsoleimani, J. Shamsi, Karim, M. Arash, and Ahmadi, "A Novel CMOS-Memristor Based Inverter Circuit Design," in *22nd Iranian Conference on Electrical Engineering (ICEE)*, IEEE, 2014, pp. 371–276.

[33] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov, G. S. Snider, G. Medeiros-Ribeiro, and R. S. Williams, "Memristor-CMOS Hybrid Integrated Circuits for Reconfigurable Logic," *Nano Letters*, vol. 9, no. 10, pp. 3640–3645, 2009.

[34] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "Memristive Switches Enable Stateful Logic Operations via Material Implication," *Nature*, vol. 464, no. 7290, pp. 873–876, 2010.

[35] S. Kvatinsky, G. Satat, N. Wald, E. Friedman, A. Kolodny, and U. Weiser, "Memristor-Based Material Implication (IMPLY) Logic: Design Principles and Methodologies," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 22, no. 10, pp. 2054–2066, 2014.

[36] S. Mohanty, "Memristor: From Basics to Deployment," *Potentials, IEEE*, vol. 32, no. 3, pp. 34–39, 2013.

[37] Y. Chen and X. Wang, "Compact Modeling and Corner Analysis of Spintronic Memristor," *IEEE/ACM International Symposium on Nanoscale Architectures, NANOARCH*, pp. 7–12, 2009.

[38] Y. Chen, G. Liu, C. Wang, W. Zhang, R.-W. Li, and L. Wang, "Polymer Memristor for Information Storage and Neuromorphic Applications," *Mater. Horiz.*, vol. 1, no. 5, pp. 489–506, 2014.

[39] T. Prodromakis, K. Michelakisy, and C. Toumazou, "Fabrication and Electrical Characteristics of Memristors with TiO_2/TiO_{2+x} Active Layers," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, 2010, pp. 1520–1522.

[40] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, and R. S. Williams, "Switching Dynamics in Titanium Dioxide Memristive Devices," *Journal of Applied Physics*, vol. 106, no. 7, 2009.

[41] J. J. Yang, F. Miao, M. D. Pickett, D. A. A. Ohlberg, D. R. Stewart, C. N. Lau, and R. S. Williams, "The mechanism of electroforming of metal oxide memristive switches," *Nanotechnology*, vol. 20, no. 21, p. 215 201, 2009.

[42] Y. N. Joglekar and S. J. Wolf, "The Elusive Memristor: Properties of Basic Electrical Circuits," *European Journal of Physics*, vol. 30, no. 4, p. 661, 2009.

[43] Z. Biolek, D. Biolek, and V. Biolková, "SPICE Model of Memristor with Nonlinear Dopant Drift," *Radioengineering*, vol. 18, no. 2, pp. 210–214, 2009.

[44] J. J. Yang, M. D. Pickett, X. Li, O. A. A., D. R. Stewart, and R. S. Williams, "Memristive Switching Mechanism for Metal/Oxide/Metal Nanodevices," *Nat Nano*, vol. 3, no. 7, pp. 429–433, 2008.

[45] E. Lehtonen and M. Laiho, "CNN using Memristors for Neighborhood Connections," in *12th International Workshop on Cellular Nanoscale Networks and Their Applications (CNNA)*, 2010, pp. 1–4.

[46] J. G. Simmons, "Generalized Formula for the Electric Tunnel Effect between Similar Electrodes Separated by a Thin Insulating Film," *Journal of Applied Physics*, vol. 34, no. 6, pp. 1793–1803, 1963.

[47] H. Abdalla and M. Pickett, "SPICE Modeling of Memristors," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2011, pp. 1832–1835.

[48] D. B. Strukov, J. L. Borghetti, and R. S. Williams, "Coupled Ionic and Electronic Transport Model of Thin-Film Semiconductor Memristive Behavior," *Small*, vol. 5, no. 9, pp. 1058–1063, 2009.

[49] J. P. Strachan, A. C. Torrezan, F. Miao, M. D. Pickett, J. Joshua Yang, W. Yi, G. Medeiros-Ribeiro, and R. Stanley Williams, "State Dynamics and Modeling of Tantalum Oxide Memristors," *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2194–2202, 2013.

[50] C. Yakopcic, T. M. Taha, G. Subramanyam, and R. E. Pino, "Generalized Memristive Device SPICE Model and Its Application in Circuit Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 8, pp. 1201–1214, 2013.

[51] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Team: threshold adaptive memristor model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 1, pp. 211–221, 2013.

[52] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, *et al.*, "A Ferroelectric Memristor," *Nature materials*, vol. 11, no. 10, pp. 860–864, 2012.

[53] S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM – A General Model for Voltage Controlled Memristors," in *CCIT Technical Report no.856*, 2014.

[54] L. Zhang, Z. Chen, J. Joshua Yang, B. Wysocki, N. McDonald, and Y. Chen, "A Compact Modeling of TiO_2-TiO_{2-x} Memristor," *Applied Physics Letters*, vol. 102, no. 13, 2013.

[55] F. Merrikh Bayat, B. Hoskins, and D. B. Strukov, "Phenomenological Modeling of Memristive Devices," *Applied Physics A*, vol. 118, no. 3, pp. 779–786, 2015.

[56] M. Abramowitz and I. A. Stegun, *Handbook of Mathematical Functions*. New York: Dover Publications, 1965.

[57] J. G. Simmons, "Electric Tunnel Effect between Dissimilar Electrodes Separated by a Thin Insulating Film," *Journal of Applied Physics*, vol. 34, no. 9, pp. 2581–2590, 1963.

[58] J. G. Simmons, "Potential Barriers and Emission-Limited Current Flow Between Closely Spaced Parallel Metal Electrodes," *Journal of Applied Physics*, vol. 35, no. 8, pp. 2472–2481, 1964.

[59] J. Shin, I. Kim, K. P. Biju, M. Jo, J. Park, J. Lee, S. Jung, W. Lee, S. Kim, S. Park, and H. Hwang, "TiO_2-Based Metal-Insulator-Metal Selection Device for Bipolar Resistive Random Access Memory Cross-Point Application," *Journal of Applied Physics*, vol. 109, no. 3, p. 033 712, 2011.

[60] M. E. Fouda and A. Radwan, "Memristor-Based Voltage-Controlled Relaxation Oscillators," *International Journal of Circuit Theory and Applications*, vol. 42, no. 10, pp. 1092–1102, 2014.

Appendix A

SPICE and Verilog-A Models

A.1 Simple Model

A.1.1 SPICE Model

```
.SUBCKT TB_Model p n $PARAMS:
************** Parameters **************
+phy1=0.6 phy2=1.4 Lm=0.0998 ffb=3.5e-6
+ifb=115e-6 afb=1.2 frb=40e-6 irb=8.9e-6
+arb=1.8 b=590e-6 wc=102e-3 w_init=1.2
*****************************************
Gfb p internal value='stp(V(x))*(1/V(dw))^2*0.1234*(V(phi2)*exp(-V(B)*
    V(fbsr))-(V(phi2)+abs(V(x)))*exp(-V(B)*V(fbsr2)))'
Grb internal p value='stp(-V(x))*(1/V(dw))^2*0.1234*(V(phi1)*exp(-V(B)
    *V(rbsr))-(V(phi1)+abs(V(x)))*exp(-V(B)*V(rbsr2)))'
Rf internal n 250
Eg x 0 value='V(p)-V(internal)'
Elamda Lmda 0 value='Lm/V(w)'
EB B 0 value='10.24634*V(dw)'
ER R 0 value='(V(w2)/V(w1))*(V(w)-V(w1))/(V(w)-V(w2))'
Efbsr fbsr 0 value='sqrt(V(phi2))'
Efbsr2 fbsr2 0 value='sqrt(V(phi2)+abs(V(x)))'
Erbsr rbsr 0 value='sqrt(V(phi1))'
Erbsr2 rbsr2 0 value='sqrt(V(phi1)+abs(V(x)))'
Efbw1 fbw1 0 value='1.2*V(Lmda)*V(w)/phy2'
Erbw1 rbw1 0 value='((9.2*V(Lmda)*V(w))/(3*phy1+4*V(Lmda)-2*(abs(V(x))
    -V(dphi))))-((1.2*V(Lmda)*V(w))/(phy2-abs(V(x))))'
Efbw2 fbw2 0 value='V(w1)+V(w)-((9.2*V(Lmda)*V(w))/(3*phy2+4*V(Lmda)
    -2*(abs(V(x))+V(dphi))))'
Erbw2 rbw2 0 value='V(w)-((1.2*V(Lmda)*V(w))/(phy2-abs(V(x))))'
Ew1 w1 0 value='stp(V(x))*V(fbw1) + stp(-V(x))*V(rbw1)'
```

```
Ew2 w2 0 value='stp(V(x))*V(fbw2) + stp(-V(x))*V(rbw2)'
EDw dw 0 value='V(w2)-V(w1)'
EDphi dphi 0 value='phy2-phy1'
Ephi1 phi1 0 value='phy1-(abs(V(x))-V(dphi))*((V(w1)+V(w2))/(2*V(w)))
    -1.15*V(Lmda)*V(w)*log(V(R))/V(dw)'
Ephi2 phi2 0 value='phy2-(abs(V(x))+V(dphi))*((V(w1)+V(w2))/(2*V(w)))
    -1.15*V(Lmda)*V(w)*log(V(R))/V(dw)'
C1 w 0 1e-9 IC='w_init'
R w 0 1e15
Ec c 0 value='abs(V(internal)-V(n))/250'
Emon1 mon1 0 value='((V(w)-afb)/wc)-(V(c)/b)'
Emon2 mon2 0 value='(arb-V(w))/wc-(V(c)/b)'
Gfbw 0 w value='ffb*sinh(stp(V(x))*V(c)/ifb)*exp(-exp(V(mon1))-V(w)/wc
    )'
Grbw w 0 value='frb*sinh(stp(-V(x))*V(c)/irb)*exp(-exp(V(mon2))-V(w)/
    wc)'
.ENDS TB_Model
```

A.1.2 Verilog-A Model

```
`include "constants.vams"
`include "disciplines.vams"
module My_Model_VerilogA(p, n);
    inout p, n;
    electrical p, n, intr;
    parameter real dt=200e-6;
    parameter real w_initial=1.2;
    parameter real f_off = 3.5e+3;
    parameter real i_off = 115e-6;
    parameter real a_off = 1.2;
    parameter real b = 590e-6;
    parameter real w_c = 102e-3;
    parameter real f_on = 40e+3;
    parameter real i_on = 8.9e-6;
    parameter real a_on = 1.8;
    parameter real R_internal = 250;
    parameter phi_2 = 1.4;
    parameter phi_1 = 0.6;
    real first_iteration, lamda, B, delta_phi;
    real w, w1, w2, vg, delta_w, phi_I, curr, dwdt;
analog function integer sign;
    real arg; input arg;
    sign = (arg >= 0 ? 1 : -1 );
```

```
endfunction
analog function integer stp;
    real arg; input arg;
    stp = (arg >= 0 ? 1 : 0 );
endfunction
analog begin
    if (first_iteration == 0) begin
        w = w_initial;
        dwdt_last = 0;
        end
    lamda = 0.0998/w;
    delta_phi = phi_2 - phi_1;
    vg = abs(V(p,intr));
    if (sign(V(p,n)) == 1) begin
        w1 = 1.2*0.0998/phi_2;
        delta_w = w - (9.2*0.0998/(3*phi_2 + 4*lamda - 2*(vg +
            delta_phi)));
        w2 = w1 + delta_w;
        B = 10.24634*delta_w;
        phi_I = phi_2 - (vg + delta_phi)*((w1+w2)/2/w) - (0.1148/
            delta_w*ln((w2*(w-w1))/(w1*(w-w2))));
    end
    else begin
        w1 = (0.91816/(3*phi_1 + 4*lamda - 2*(vg - delta_phi))) -
            (0.11976/(phi_2 - vg));
        w2 = w - (0.11976/(phi_2 - vg));
        delta_w = w2 - w1;
        B = 10.24634*delta_w;
        phi_I = phi_1 - (vg - delta_phi)*((w1+w2)/2/w) - (0.1148/
            delta_w*ln((w2*(w-w1))/(w1*(w-w2))));
    end
    curr = (0.1233/(pow(delta_w,2))*(phi_I*exp(-B*sqrt(phi_I)) - (
        phi_I + vg)*exp(-B*sqrt(phi_I + vg))));
    if (sign(V(p,n))==1)
        dwdt = f_off*sinh(abs(curr)/i_off)*exp(-exp(((w-a_off)/w_c)-(
            abs(curr)/b))-(w/w_c));
    else
        dwdt = -f_on*sinh(abs(curr)/i_on)*exp(-exp(((a_on-w)/w_c)-(abs
            (curr)/b))-(w/w_c));
    w = w + (dwdt + dwdt_last)*dt/2;
    dwdt_last = dwdt;
    I(p,n) <+ sign(V(p,intr))*curr;
    V(intr,n) <+ sign(V(p,intr))*curr*R_internal;
```

```
    first_iteration=1;
end
endmodule
```

A.2 Generalized Model

A.2.1 SPICE Model

```
.SUBCKT TB_Model p n $PARAMS:
************** Parameters **************
+phy1=0.6 phy2=1.4 Lm=0.0998 ffb=3.5e-6
+ifb=115e-6 afb=1.2 frb=40e-6 irb=8.9e-6
+arb=1.8 b=590e-6 wc=102e-3 w_init=1.2
*****************************************
Gfb p internal value='stp(V(x))*(1/V(dw))^2*0.1234*(V(phi2)*exp(-V(B)*
    V(fbsr))-(V(phi2)+abs(V(x)))*exp(-V(B)*V(fbsr2)))'
Grb internal p value='stp(-V(x))*(1/V(dw))^2*0.1234*(V(phi1)*exp(-V(B)
    *V(rbsr))-(V(phi1)+abs(V(x)))*exp(-V(B)*V(rbsr2)))'
Ctun p internal Value='8.854e-12*5*2e-5/V(w)' IC=0
Rf internal n 250
Eg x 0 value='V(p)-V(internal)'
Elamda Lmda 0 value='Lm/V(w)'
EB B 0 value='10.24634*V(dw)'
ER R 0 value='(V(w2)/V(w1))*(V(w)-V(w1))/(V(w)-V(w2))'
Efbsr fbsr 0 value='sqrt(V(phi2))'
Efbsr2 fbsr2 0 value='sqrt(V(phi2)+abs(V(x)))'
Erbsr rbsr 0 value='sqrt(V(phi1))'
Erbsr2 rbsr2 0 value='sqrt(V(phi1)+abs(V(x)))'
Efbw1 fbw1 0 value='1.2*V(Lmda)*V(w)/phy2'
Erbw1 rbw1 0 value='((9.2*V(Lmda)*V(w))/(3*phy1+4*V(Lmda)-2*(abs(V(x))
    -V(dphi))))-((1.2*V(Lmda)*V(w))/(phy2-abs(V(x))))'
Efbw2 fbw2 0 value='V(w1)+V(w)-((9.2*V(Lmda)*V(w))/(3*phy2+4*V(Lmda)
    -2*(abs(V(x))+V(dphi))))'
Erbw2 rbw2 0 value='V(w)-((1.2*V(Lmda)*V(w))/(phy2-abs(V(x))))'
Ew1 w1 0 value='stp(V(x))*V(fbw1) + stp(-V(x))*V(rbw1)'
Ew2 w2 0 value='stp(V(x))*V(fbw2) + stp(-V(x))*V(rbw2)'
EDw dw 0 value='V(w2)-V(w1)'
EDphi dphi 0 value='phy2-phy1'
Ephi1 phi1 0 value='phy1-(abs(V(x))-V(dphi))*((V(w1)+V(w2))/(2*V(w)))
    -1.15*V(Lmda)*V(w)*log(V(R))/V(dw)'
Ephi2 phi2 0 value='phy2-(abs(V(x))+V(dphi))*((V(w1)+V(w2))/(2*V(w)))
    -1.15*V(Lmda)*V(w)*log(V(R))/V(dw)'
```

```
C1 w 0 1e-9 IC='w_init'
R w 0 1e15
Ec c 0 value='abs(V(internal)-V(n))/250'
Emon1 mon1 0 value='((V(w)-afb)/wc)-(V(c)/b)'
Emon2 mon2 0 value='(arb-V(w))/wc-(V(c)/b)'
Gfbw 0 w value='ffb*sinh(stp(V(x))*V(c)/ifb)*exp(-exp(V(mon1))-V(w)/wc
    )'
Grbw w 0 value='frb*sinh(stp(-V(x))*V(c)/irb)*exp(-exp(V(mon2))-V(w)/
    wc)'
.ENDS TB_Model
```

A.2.2 Verilog-A Model

```
`include "constants.vams"
`include "disciplines.vams"
module My_Model_VerilogA(p, n);
    inout p, n;
    electrical p, n, intr, c;
    parameter real dt=200e-6;
    parameter real w_initial=1.2;
    parameter real f_off = 3.5e+3;
    parameter real i_off = 115e-6;
    parameter real a_off = 1.2;
    parameter real b = 590e-6;
    parameter real w_c = 102e-3;
    parameter real f_on = 40e+3;
    parameter real i_on = 8.9e-6;
    parameter real a_on = 1.8;
    parameter real R_internal = 250;
    parameter phi_2 = 1.4;
    parameter phi_1 = 0.6;
    real first_iteration, lamda, B, delta_phi, cap, dwdt_last;
    real w, w1, w2, vg, delta_w, phi_I, curr, curr_total, dwdt;
analog function integer sign;
    real arg; input arg;
    sign = (arg >= 0 ? 1 : -1 );
endfunction
analog function integer stp;
    real arg; input arg;
    stp = (arg >= 0 ? 1 : 0 );
endfunction
analog begin
    if (first_iteration == 0) begin
```

```
        w = w_initial;
        dwdt_last = 0;
    end
    lamda = 0.0998/w;
    delta_phi = phi_2 - phi_1;
    vg = abs(V(p,intr));
    if (sign(V(p,n)) == 1) begin
        w1 = 1.2*0.0998/phi_2;
        delta_w = w - (9.2*0.0998/(3*phi_2 + 4*lamda - 2*(vg +
            delta_phi)));
        w2 = w1 + delta_w;
        B = 10.24634*delta_w;
        phi_I = phi_2 - (vg + delta_phi)*((w1+w2)/2/w) - (0.1148/
            delta_w*ln((w2*(w-w1))/(w1*(w-w2))));
    end
    else begin
        w1 = (0.91816/(3*phi_1 + 4*lamda - 2*(vg - delta_phi))) -
            (0.11976/(phi_2 - vg));
        w2 = w - (0.11976/(phi_2 - vg));
        delta_w = w2 - w1;
        B = 10.24634*delta_w;
        phi_I = phi_1 - (vg - delta_phi)*((w1+w2)/2/w) - (0.1148/
            delta_w*ln((w2*(w-w1))/(w1*(w-w2))));
    end
    curr = (0.1233/(pow(delta_w,2))*(phi_I*exp(-B*sqrt(phi_I)) - (
        phi_I + vg)*exp(-B*sqrt(phi_I + vg))));
    cap = 8.854e-12*5*2e-5/w;
    V(c) <+ ddt(cap*V(p,intr));
    curr_total = sign(V(p,intr))*curr + V(c);
    if (sign(V(p,n))==1)
    dwdt = f_off*sinh(abs(curr_total)/i_off)*exp(-exp(((w-a_off)/w_c)
        -(abs(curr_total)/b))-(w/w_c));
    else
    dwdt = -f_on*sinh(abs(curr_total)/i_on)*exp(-exp(((a_on-w)/w_c)-(
        abs(curr_total)/b))-(w/w_c));
    w = w + (dwdt + dwdt_last)*dt/2;
    dwdt_last = dwdt;
    I(p,n) <+ curr_total;
    V(intr,n) <+ curr_total*R_internal;
    first_iteration=1;
end
endmodule
```

ملخص الرسالة

مع اقتراب نهاية تطبيق قانون مور، يبحث العلماء الأن عن نبائط جديدة لنتمكن من تحقيق ما بعد مور. أحد هذه النبائط الواعده هو الميمريستور. تعتبر الميمريستورات (اختصار للمقاومة المتذكرة) المكون الكهربي الرابع الغير فعال، بجانب المقاوم الكهربي، المكثف، و ملف الحث. اول من فرض نظرية الميمريستور هو العالم ليون تشوا عام ١٩٧١، و اول من قام بتصنيعه هي معامل HP عام ٢٠٠٨. تتمتع الميمريستورات بخصائص مميزة و واعدة، مثل: منحنيات جهد و تيار ذات شكل هيستيري، احجام صغيرة تصل الي بضع نانومترات، و القدرة علي الاحتفاظ بالقيمة الأخيرة للمقاومة حتي بعد انقطاع المصدر الكهربي.

في هذا البحث، يتم تناول الميمريستورات ذات الشعيرة الموصلة و دراسة النماذج الحالية لها بهدف تحسينها. نقدم طريقة جديدة لنمذجة الميمريستورات بالأخذ في الأعتبار حاجز للجهد علي شكل شبه منحرف. البحث مقسم الي جزئين: جزء للنبائط و جزء للدوائر الكهربية.

في جزء النبائط، يتم تطبيق و حل الطريقة المقترحة باستخدام وسيلتين مختلفتين. أول وسيلة هي استخدام دوال آيري، و ثاني وسيلة هي استخدام نموذج سيمونز لعبور حاجز للجهد علي شكل شبه منحرف. ثم يتم مقارنة النموذجين مع النتائج المعملية للتأكد من صحتهما و رفع كفاءة النمذجة بصورة ملحوظة. بالاضافة الي هذا، قمنا بدراسة تاثير البارامترات المختلفة للنموذج علي منحني الجهد و التيار للميمريستور. بعض هذه البارامترات هي: ارتفاع حاجز الجهد، شكل و تردد و قيمة الجهد المطبق علي الميمريستور. تم استنتاج علاقة من كل من هذه الدراسات و التي ستفيد مصممو الدوائر الكهربية كثيرا.

في جزء الدوائر الكهربية، قمنا بعمل نمط SPICE و نمط Verilog-A مبنيان علي نموذج سيمونز لعبور حاجز للجهد علي شكل شبه منحرف، و قمنا باستخدام هذه الأنمطة في محاكاة بعض تطبيقات الميمريستور في الدوائر الكهربية و مناقشة هذه النتائج.

مهندس: عمرو محمود حسن محمود
تاريخ الميلاد: ١٩٨٩/٠٣/٠٢
الجنسية: مصري
تاريخ التسجيل: ٢٠١٢/٠٣/١٣
تاريخ المنح: ..../..../....
الدرجة: ماجستير العلوم
القسم: الرياضيات و الفيزيقا الهندسية

المشرفون:

أ.د. نادية حسين رأفت
أ.د. حسام علي فهمي

الممتحنون:

أ.د. نادية حسين رأفت (المشرف الرئيسي)
أ.د. حسام علي حسن فهمي (مشرف)
أ.د. علاء قرني عبد المجيد (الممتحن الداخلي)
أ.د. خالد علي شحاته (الممتحن الخارجي)
(كلية الهندسة – الاكاديمية العربية للعلوم و التكنولوجيا)

عنوان الرسالة:

نموذج محسن للميمريستور ذو الشعيرة الموصلة و تطبيقه علي بعض الدوائر الكهربية

الكلمات الدالة:
الميمريستور، الميمريستور ذو الشعيرة الموصلة، دوال آيري، حاجز للجهد علي شكل شبه منحرف

ملخص الرسالة:
تعتبر الميمريستورات المكون الكهربي الرابع الغير فعال و تتميز بخصائص فريدة و واعدة. هذه الرسالة تهدف الي تقديم طريقة جديدة لتحسين النمذجة الحالية للميمريستورات بالأخذ في الاعتبار حاجز للجهد علي شكل شبه منحرف. البحث مقسم الي جزئين: جزء للنبائط و جزء للدوائر الكهربية. في جزء النبائط، يتم تطبيق و حل الطريقة المقترحة باستخدام وسيلتين مختلفتين، ثم يتم مقارنة النموذجين مع النتائج المعملية و رفع كفاءة النمذجة بصورة ملحوظة. في جزء الدوائر الكهربية، يتم استخدام النموذج المقترح في محاكاة بعض تطبيقات الميمريستور في الدوائر الكهربية.

نموذج محسن للميمريستور ذو الشعيرة الموصلة و تطبيقه علي بعض الدوائر الكهربية

إعداد

عمرو محمود حسن محمود

رسالة مقدمة إلي
كلية الهندسة – جامعة القاهرة
كجزء من متطلبات الحصول علي درجة
ماجستير العلوم
في
الفيزيقا الهندسية

يعتمد من لجنة الممتحنين:

أ.د. نادية حسين رأفت – المشرف الرئيسي

أ.د. حسام علي حسن فهمي – مشرف

أ.د. علاء قرني عبد المجيد – الممتحن الداخلي

أ.د. خالد علي شحاته – الممتحن الخارجي
(كلية الهندسة – الاكاديمية العربية للعلوم و التكنولوجيا)

كلية الهندسة – جامعة القاهرة
الجيزة – جمهورية مصر العربية
٢٠١٥

نموذج محسن للميمريستور ذو الشعيرة الموصلة و تطبيقه علي بعض الدوائر الكهربية

إعداد

عمرو محمود حسن محمود

رسالة مقدمة إلي
كلية الهندسة – جامعة القاهرة
كجزء من متطلبات الحصول علي درجة
ماجستير العلوم
في
الفيزيقا الهندسية

تحت إشراف

أ.د. نادية حسين رأفت
أستاذ
قسم الرياضيات و الفيزيقا الهندسية
كلية الهندسة – جامعة القاهرة

أ.د. حسام علي فهمي
أستاذ
قسم الاتصالات و الالكترونيات الكهربية
كلية الهندسة – جامعة القاهرة

كلية الهندسة – جامعة القاهرة
الجيزة – جمهورية مصر العربية
٢٠١٥

نموذج محسن للميمريستور ذو الشعيرة الموصلة و تطبيقه علي بعض الدوائر الكهربية

إعداد

عمرو محمود حسن محمود

رسالة مقدمة إلي
كلية الهندسة – جامعة القاهرة
كجزء من متطلبات الحصول علي درجة
ماجستير العلوم
في
الفيزيقا الهندسية

كلية الهندسة – جامعة القاهرة
الجيزة – جمهورية مصر العربية
٢٠١٥