A PROGRAMMABLE BASEBAND CHAIN FOR A GSM/DECT FULLY INTEGRATED CMOS RF RECEIVER

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Abstract *- A programmable/reconfigurable baseband chain with filter and amplifier sections that can be shared by two different wireless standards, GSM and DECT, is presented in this paper. This results in a simplified, low power and cost-effective design solution. Filters and amplifiers of the baseband chain were implemented using a fully balanced differential difference amplifier (FBDDA). A new approach is used to implement an analog to digital converter using the FBDDA in order to enhance the design regularity. The noise and linearity performance of individual stages was investigated, and simulations of the overall system showed that it complies with both standards under consideration. Using a suitable algorithm implemented by the digital signal processor (DSP) of the receiver, the chain could be configured to operate efficiently in different environments.*

I. INTRODUCTION

Global roaming is a fundamental goal of the evolution of the third generation (3G) wireless telecommunication systems. This requires the 3G mobile terminals to achieve a wide compatibility between various co-existing standards as well as backward compatibility. In this paper the design of a digitally programmable baseband chain suitable for monolithic integration is presented. The design supports two of the most common wireless standards: the Global System for Mobile telecommunications (GSM) and the Digitally Enhanced Cordless Telecommunication (DECT) standard.

While digital technologies can easily realize reconfigurable low cost single chip solutions, the analog front end continues to be the bottleneck of a fully integrated solution [1]. The processing of the received signal by the analog front end of a receiver is achieved as follows: First, the RF spectrum is translated to the baseband, and then the weak received signal is amplified while the strong surrounding interferers are attenuated by filtering. Finally, the resulting signal is then digitized for further demodulation and/or other signal processing. The digital signal processor (DSP) of the receiver will be responsible of configuring the receiver blocks to exhibit the required bandwidth, gain and amount of filtering to accommodate the operating standard.

The organization of this paper is as follows: in section II the building blocks of the baseband chain are implemented using fully balanced differential deference amplifier (FBDDA). Then the overall system performance is studied in section III. Section IV summarizes the main findings of the paper and concludes it.

II. BASEBAND CHAIN BLOCKS

The first step in the design of the baseband chain is the implementation of the main building block: the differential difference amplifier (DDA) [2]. It is used later in the implementation of the successive stages. Since most of the modern high performance analog integrated circuits incorporate fully differential signal paths, a fully balanced differential difference amplifier (FBDDA)[3] was used. The complete circuit of FBDDA and its symbolic representation are shown in Fig. 1-a and Fig. 1-b, respectively.

The circuit was simulated using TopSpice V5.7 and a 0.5 μm model available through MOSIS. The open loop gain of the FBDDA was found to be around 6170 associated with an offset voltage of -1.4 μV and a power consumption of 4.62 mW at the quiescent point. The unity gain bandwidth of the open loop FBDDA was 40.12 MHz associated with a load of 1.5 pF. Noise analysis clarified that the above FBDDA has a flicker and thermal noises, measured at 1 KHz, of 17.24 nV/√Hz and 6.52 nV/√Hz, respectively.

A. Filters

There are different filter classes that can be incorporated in the design of the baseband chain. Active-RC, MOS-C, Gm-C, and switched capacitor filters are some examples. Active RC and MOS-C classes are attractive since linearity requirements can be easily maintained by employing linear poly resistors and poly-to-poly capacitances. Also the active RC class has the highest signal to noise ratio among all classes [4]. Three different kinds of filters are incorporated in the design of the whole chain. All of them share one essential property, which is "programmability". Programmability means that the DSP can change the filter bandwidth to accommodate the appropriate signal received either for GSM or DECT.

To begin with, a 2nd order prefilter is be used to attenuate the out-of-band blockers to prevent aliasing and keep the ADC dynamic range in an applicable range. On the other hand, hard restrictions are imposed on the prefilter due to its position as the first stage in the chain. Thus, the prefilter is required to have low input referred noise and high linearity. In order to attenuate adjacent channels to levels below the noise level, at least a 5th order filter is required. So, a 3rd order filter had to be implemented in addition to the previously implemented 2nd order filter. Two different versions were introduced: nontunable and tunable filters. A

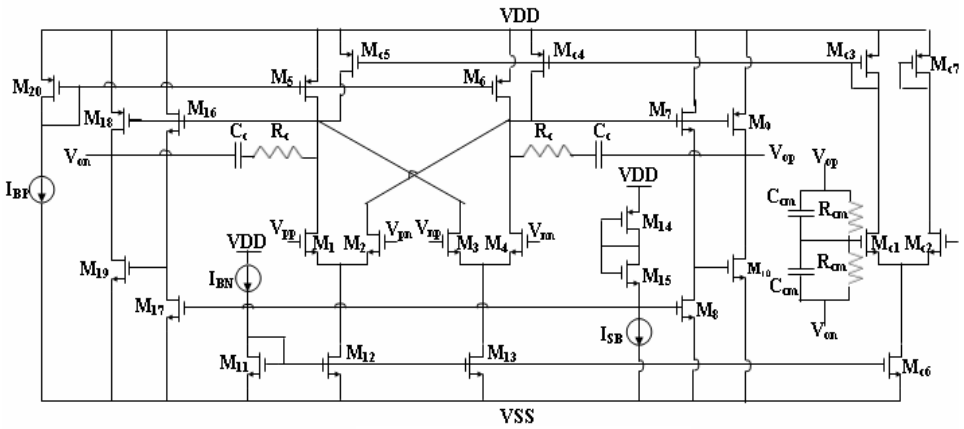

Figure 1. a)
FBDDA Circuit Diagram.

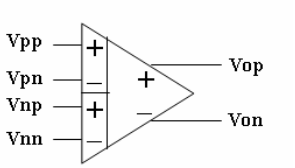

Figure 1.b)
FBDDA Symbol.

nontunable 3rd order filter can be simply constructed by cascading a first order RC passive filter to the prefilter previously described. This configuration is desirable since it involves one active element per 3rd order filter, which will improve the overall linearity, noise and power consumption. Programmability is achieved by altering the resistor values through employing an N-MOS transistor as a switch. On the other hand, the tunable filter incorporates the concept of MOS-C filter. Its design is similar to the nontunable one except that an N-MOS transistor operating in the triode region is connected in parallel with the resistors. Fig. 2 shows the circuit connection. It is clear that by varying the gate voltages of MOS transistors we can finely tune the combined resistor values to get the desired precise bandwidth. The filter response to different DC input voltage values is illustrated in Fig. 3 for GSM operation.

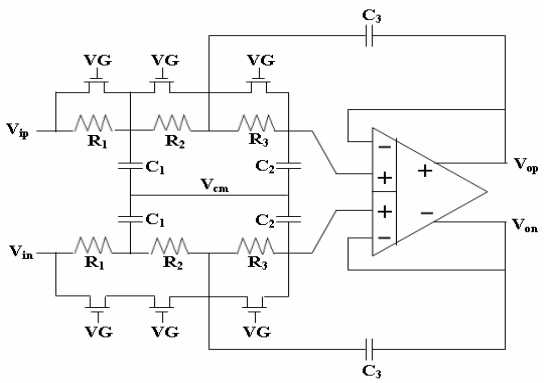

Figure 2
3rd Order Fully Differential Sallen-key Filter.

B. Variable Gain Amplifiers

Variable gain amplifiers (VGAs) are employed in many applications in order to maximize the dynamic range of the overall system. The VGA is typically employed in a feedback loop to realize an automatic gain control (AGC) loop. Another important consideration of feedback loops is the DC offset cancellation as a small DC offset can be amplified by the VGA to a level that saturates the following stages or may cause the output signal to be clipped.

In order to be employed in the programmable baseband chain, a VGA should have digitally controlled gain and offset trimming capabilities, with gain steps independent of the differential VGA based on different techniques were investigated. The second generation current conveyor (CCII) based VGA [5], decibel linear VGA [6,7] and a modified current division network (CDN) based one were simulated. Simulation results showed that even though the above realizations exhibit almost constant bandwidth at different gain settings and dissipates the same power, the CCII based VGA has the best noise performance. Thus, the VGA to be employed in the baseband chain is the CCII based one that is based on the concept of current sensing, as originally introduced by Sedra and Smith in 1970 [8]. The currents of both output terminals of a differential buffer are sensed and conveyed to additional current ports I_{zn} and I_{zp} using current

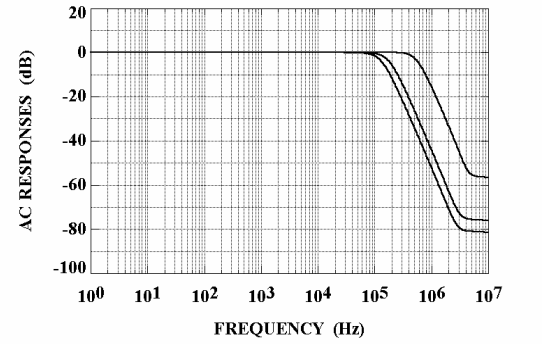

Figure 3
Tunable Filter AC Response for GSM Operation.

mirrors as shown in Fig. 4. A Resistor array is used to digitally program the gain. Depending on the level of the received signal, the DSP applies a control word to the gates of the programming transistors in order to get the required gain from the VGA. Resistor values are chosen to give almost fixed gain steps. The offset voltage V_{off} is determined by the DSP then fed back to the VGA through digital to analog converter DAC to carry out DC offset cancellation process. Fig. 5. shows the AC response on the proposed VGA.

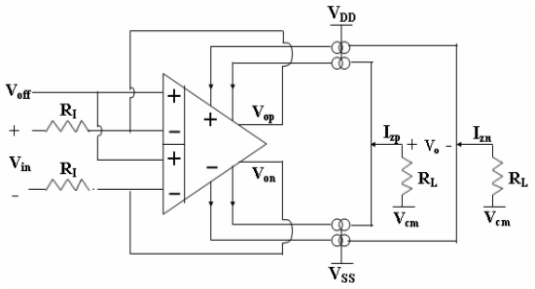

Figure 4
Digitally Programmable VGA

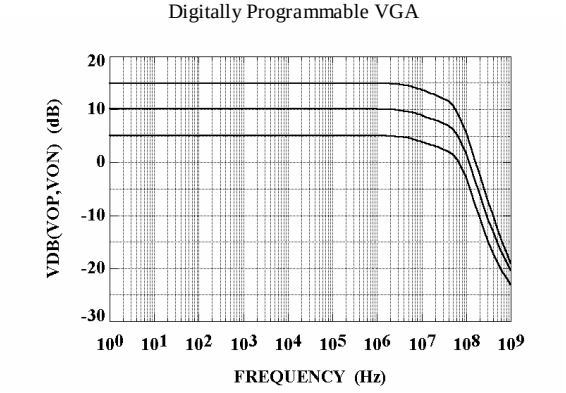

Figure 5
AC Response Of The CCII-Based VGA.

C. Analog to Digital Converter

The ADC provides the link between the analog world (the baseband chain) and the digital world (DSP) in the receiver. An algorithmic-pipelined [9] ADC was implemented using the FBDDA to enhances the design regularity. This realization of the ADC consists of a sample and hold circuit, a comparator, and adder/subtractor and multiplier circuit.

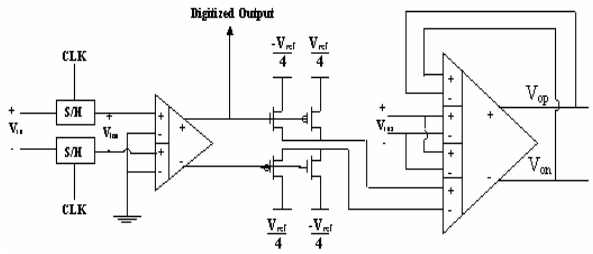

Figure 6
Complete Circuit Of One Stage Of The A/D Converter.

The operation of algorithmic ADC, $V_{out} = 2V_{in} \pm V_{ref} / 2$, (addition/subtraction and multiplication) can be achieved by employing one active element and resistors. The use of resistors doesn't give accurate doubling due to process mismatches. A new approach is taken here using special characteristics of the FBDDA to perform this operation. By adding two differential pairs identical to the two input pairs the FBDDA is modified into an 8-input version. When the two outputs V_{op} and V_{on} are fed back to one differential pair (*VP1* and *VN1*), the input V_{in} is fed differentially into the second and third differential pairs (*VP2*, *VN2* and *VP3*, *VN3*) and the input $V_{ref} / 2$ is fed differentially into the last pair (*VP4* and *VN4*) then the differential output of the FBDDA would be $V_{op} - V_{on} = 2V_{in} - V_{ref} / 2$. In this way doubling and subtraction are carried out accurately using a single active element. The complete circuit of one stage of the proposed fully differential ADC converter is shown in Fig. 6. Fig. 7 shows the doubling and subtraction of the input by the FBDDA.

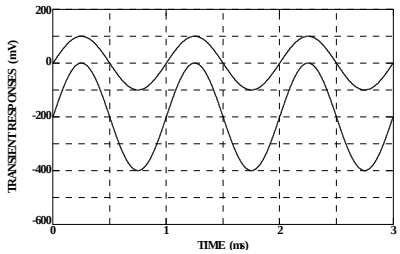

Figure 7
Multiplication by 2 and Subtraction

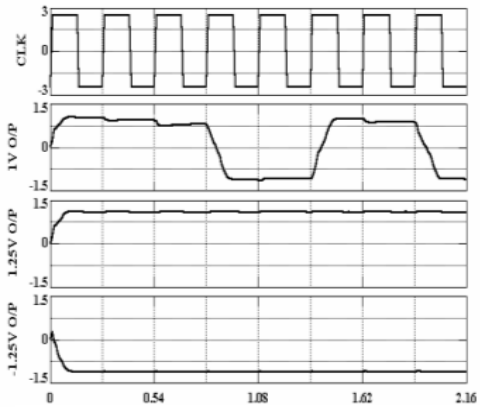

Figure 8
ADC Output For Different Dc Inputs

The ADC was simulated when working as one cell by feeding the output to the input. Thus the ADC produces N bits every *N* clock cycles. This is because the pipelined configuration could not be simulated. The reference voltage (V_{ref}) of the ADC was chosen to be double the largest possible signal at the input of the A/D converter, which is at 12 dBm. Thus V_{ref} should be set to be 2.5 V. The algorithmic A/D converter operates from $- V_{ref} / 2$ to $V_{ref} / 2$. Fig. 8 shows the ADC outputs when different dc values are applied to its input. Simulations were carried out using the open loop S&H circuit with Miller capacitance. The ADC resolution was found to be 8 bits. Since the S&H circuits are the main source of error [10] that limits the resolution of the ADC, the resolution will double if we use a pipelined architecture, as each stage will contain only one S&H circuit instead of two for the cyclic configuration used in the simulation.

III. Simulation Results

For the receiver to be compliant with the GSM standard , and considering the gain of the RF section to be 30dB, the input IP3 of the baseband chain is required to be 12 dBm or better, while, the IIP3 required for the DECT receiver is 8 dBm [11]. Also, the baseband chain is allowed to provide a maximum input referred noise of 50 nV/√Hz for the GSM standard and 90 nV/√Hz for DECT [12].

Table I
Baseband Chain Configurations Following The Prefilter For GSM (A, B, C, D) AND DECT (E, F, G, H, I, J)

	1st Stage	2nd Stage	3rd Stage	4th Stage	IIP3 (dBm)	Noise nV/√Hz
a	8 dB	Tunable			17.48	46.47
b	18 dB	Nontunable			13.31	37.37
c	8 dB	Nontunable	18 dB		13.09	46.16
d	8 dB	Nontunable	28 dB		13.89	44.69
e	8 dB	Nontunable			11.86	26.99
f	18 dB	Nontunable			12.97	24.9
g	8 dB	Nontunable	18 dB		12.3	27.87
h	8 dB	Nontunable	28 dB		12.95	27.49
i	Nontunable	Tunable	8 dB	28 dB	11.4	47.25
j	Nontunable	Tunable	8 dB	18 dB	10.93	47.47

A reconfigurable chain is proposed, where the order and number of the baseband blocks can be varied. This can enhance the noise performance versus linearity or vice versa within the same standard or to change from one standard to another. The first block in the baseband chain should be the prefilter for the reasons mentioned before. Table I lists different configurations that satisfy the noise and linearity requirements if operated in GSM (a, b, c, d) and DECT (e, f, g, h, i, j) modes. It is worth mentioning that a gain stage directly after the prefilter will relax the noise requirement but reduce the overall IIP3 of the baseband chain. Obviously, this gain stage should be followed by a filter stage to attenuate the blockers and hence keep the IIP3 within the accepted limits. The relaxed noise specification of the DECT standard removes the necessity of a gain stage right after the prefilter (configurations i and j). Signal level and blockers values through the overall chain with a total gain of 36dB for DECT receiver is shown in Fig. 9.

Simulations of the ADC converter showed that a 13 bits resolution is reasonable for different gain setting. The sampling frequency of the ADC should be larger than or equal to 5MHz for GSM signals and 20MHZ for DECT signals. Thus even though configurations (b), (c) and (d) for GSM standard satisfies the both GSM and the DECT specifications, it requires a sampling frequency of 20 MHZ or greater for DECT while GSM needs only 5 MHz which means more power consumption, concluding that one configuration cannot be optimum for both standards. Reconfigurabilty gives us the option to have an efficient solution concerning power, noise or linearity. A suitable algorithm can be implemented in the DSP to carryout the reconfigurabilty role. Control signals from the DSP can be used to connect the needed blocks via a system interconnect unit. This baseband chain described in this paper can be extended to operate on future generation of wireless communication systems[1].

IV. Conclusions

In this paper, a fully differential baseband chain has been implemented that can be programmed via the DSP part of the receiver to operate in either GSM or DECT environments. A new approach that exploits the differential characteristics of the FBDDA was presented to implement an algorithmic ADC. Finally the performance of the overall system was evaluated and was found to comply with the standards underhand. As an extension, 3G wireless systems receivers with multistandard support features can be implemented using the same concept.

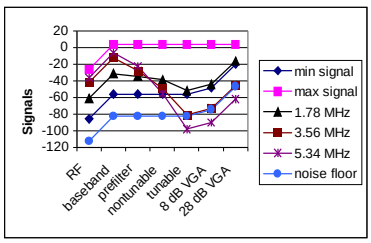

Figure 9
Signals throughout the DECT Receiver.

V. References

[1] H. Elwan "CMOS digitally Programmable Analog Front Ends for Third Generation Wireless Applications" Ph.D. Thesis, Ohio State University, 2001.

[2] E. Sackinger and W. Guggenbuhl, "A Versatile building block: The CMOS differential difference amplifier," IEEE J. Solid –State Circuits, vol. 22, pp. 287-294, Apr. 1987.

[3] H. Alzahar and M. Ismail, " A CMOS fully balanced differential difference amplifier and its applications," IEEE Trans. Circuits Syst. II, vol. 48, no.6, June 2001.

[4] T. Au, "Programmable, Low-noise, High-linearity Baseband Filter for a Fully integrated Multi-Standard CMOS RF Receiver" Master Thesis, University of California, Berkeley, 2000.

[5] H. Elwan and A. Soliman, "A novel CMOS current Conveyor realization with an current- mode filter suitable for VLSI, " IEEE Trans. Circuits Syst. II, vol. 43, no.9, pp. 663-670, Sept. 1996.

[6] H. Elwan, A. Soliman, and M. Ismail, "A CMOS Norton amplifier-based digitally controlled VGA for low-power wireless applications," IEEE Trans. Circuits Syst. II, vol. 48, no.3, pp. 245-254, March 2000.

[7] H. Elwan and M. Ismail, "Low voltage digitally controlled dB-linear CMOS VGA circuit for wireless communication"

[8] H. Alzaher, H. Elwan and M. Ismail "CMOS fully differential second-generation current conveyor", Electronics Letter, vol.36, pp. 1095-1096, June 2000.

[9] D. Johns and K. Martin, Analog Integrated Circuit Design, New York: John Wiley & Sons, first ed., 1997.

[10] B. Razavi, Principles of Data Conversion system Design, New Jersey: Prentice-Hall, first ed., 1995.

[11] B. Razavi, RF Microelectronics, Los Angeles: Prentice-Hall, first ed., 1998.

[12] J. Rudell, J. Weldon, J. Ou, L. Lin, and P. Gray, An Integrated GSM/DECT Receiver: Design Specifications, UCB Electronics Laboratory Memorandum.