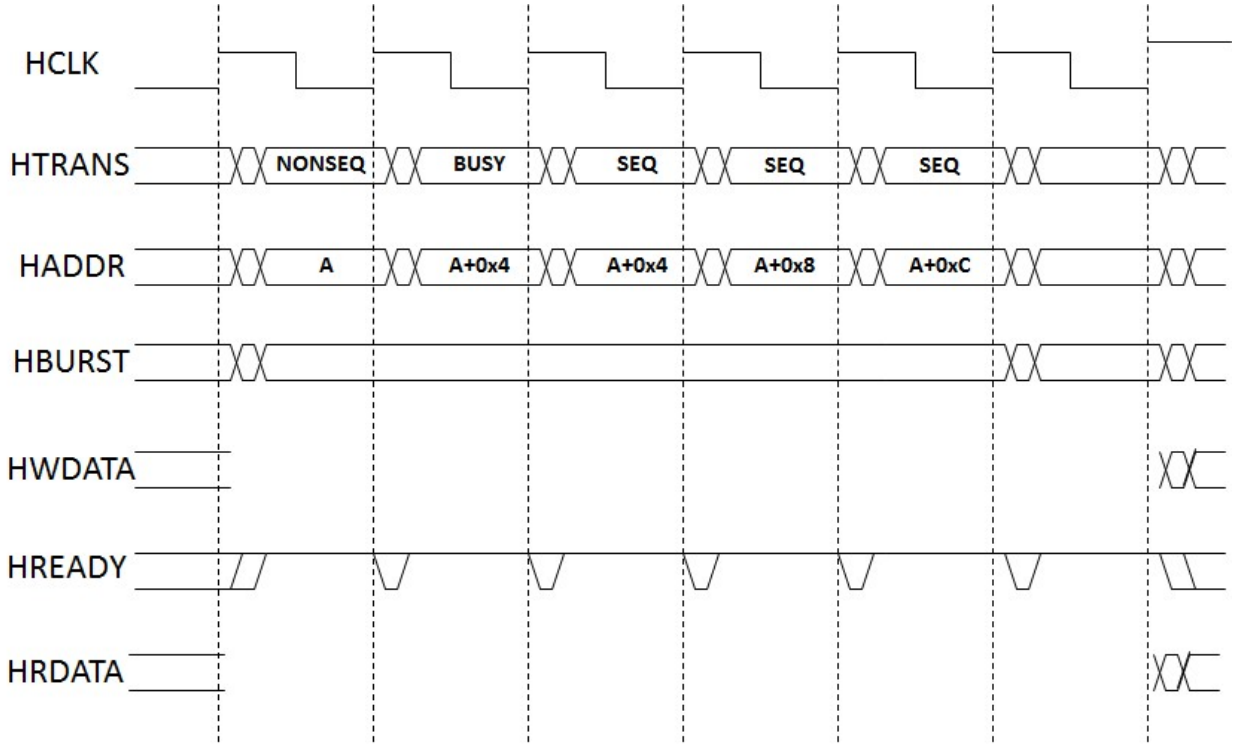
Electronics and Electrical Communications Engineering Department
Cairo University
ELC 3030 Advanced Microprocessor Architecture

Interconnections Homework

Problem 1:

Draw the potential activities of the data buses for the following burst transaction of an AHB bus



Problem 2:

Assuming we are transmitting letter "Z", binary 01011010, with even parity bit and 1 stop bit, show the sequence of bits transferred. Find the percentage overhead due to framing.

Problem 3:

Calculate the total number of bits transferred if 5 pages of ASCII data (each with 80x25 characters) are sent using asynchronous serial data transfer. Assume a data size of 8 bits, 1 stop bit, no parity. Calculate the time needed to transfer the entire 5 pages with (a) 2400 bps, (b) 9600 bps.

Problem 4:

A given bus is serving the following 2 transactions: Transaction A that reads data from a slow peripheral device and Transaction B that writes a burst of data to memory. Transaction A needs 1 clock cycle for addressing, 2 clock cycles for data read, and 13 clock cycles of wait due to the slow nature of the peripheral device. Meanwhile, transaction B consists of 1 clock cycle for addressing, 32 clock cycles for data write to memory.

a. How many clock cycles are needed to complete both transactions if no split transactions are used.
b. How many clock cycles are needed to complete both transactions if split transactions are used
c. Plot the time line of activities of both transactions in both cases indicating which transaction is using the bus and for which function.
d. What is the percentage time saving due to split transactions.

(Hint: Assume arbitration and transaction switching for split transactions do not consume any clock cycles.)

Problem 5:

Draw the signals transmitted over the USB differential pair for the following payload packet 0101111111100011.