

- Please state clearly any assumptions you make in solving the following problems.
  - Please read the solution of homework 3 before proceeding.
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## 1 Patent search

We will attempt in this problem to train you to find, understand and implement previous research work. Our focus is on multipliers.

1. Please visit the US Patent and Trademark office and search for a patent from 1976 to the present using the two terms *redundant* and *multiplier* in the title field. You should get a citation where the first author is named Nishiyama. Read this patent. (You can download the full images with complete drawings as well if you want.)

This should teach you how to search for a patent and to understand their wording which is quite different from published articles in technical journals.

2. Next, go to the papers published in the proceedings of the IEEE Symposium on Computer Arithmetic Search for a paper by the same author (Nishiyama). You should find a paper titled “Design of High Speed MOS Multiplier and Divider Using Redundant Binary Representation.” Download that paper and read it.

Please write *one page* comparing the patent and the published paper. Both documents are quite old, nevertheless they are still useful. If you are interested, you can see the recent advances in arithmetic by browsing the latest sessions of the symposium.

3. Code the three types of adder cells presented in the paper in Verilog and test them exhaustively.
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## 2 Simple calculations

Problem 5.3 of chapter 5 in the book.

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## 3 Interval arithmetic

Problem 5.13 of chapter 5 in the book