Dr. Hossam A. H. Fahmy

Professor, EECE, Cairo University, Egypt
Principal Engineer, Analog Devices Inc., Cairo, Egypt

Citizenship: Canada, Egypt
Fluent in: Arabic, English, French
Senior Member of IEEE

Education and Academic Records

1997-2003	**PhD: Stanford University, California, USA** Electrical Engineering Department, **Cumulative GPA: 4.0/4.0** Thesis: *A Redundant Digit Floating Point System*
1995-1997	**MSc: Cairo University, Cairo, Egypt** Electronics and Electrical Communications Engineering Thesis: *Novel Digital Structures Utilizing Single Electron Devices*
1990-1995	**BSc: Cairo University, Cairo, Egypt** Electronics and Electrical Communications Engineering, **Rank: 1st/216** Graduation project: *Design and implementation of a 24 bit RISC processor on a VLSI chip using the sea-of-gates technology*

Academic Positions

June 2015 to Present	**Professor**, Electronics and Electrical Communications Engineering Department, Cairo University, Egypt.
July 2017 to June 2018	**Professor and Program Director**, Communications and Information Engineering, Zewail City of Science and Technology, Egypt.
Spring of 2016 and 2017	**Visiting Faculty**, Electrical and Computer Engineering Department, Sultan Qaboos University, Oman.
June 2010 to June 2015	**Associate Professor**, Electronics and Electrical Communications Engineering Department, Cairo University, Egypt.
July 2006 to June 2010	**Assistant Professor**, Electronics and Electrical Communications Engineering Department, Cairo University, Egypt.
June 2005 to June 2006	**Assistant Professor**, Divison of Computing Systems, School of Computer Engineering, Nanyang Technological University, Singapore.
Nov. 2003 to June 2005	**Assistant Professor**, Electronics and Electrical Communications Engineering Department, Cairo University, Egypt.

Teaching Experience

Cairo University, Egypt	*Computer Arithmetic* (graduate class)	Autumn 2003, 2004, 2006 to 2014, 2016
	Technical English (graduate class)	Autumn 2003, 2004, 2006 to 2008, Winter 2010 to 2015
	Computer Architecture (undergraduate class)	Autumn 2003, 2004, 2006 to 2016
	Computer Architecture (graduate class)	Winter 2007 to 2015
	Electronics and Instrumentations Labs	Winter 2004, 2005, 2009
	Operating Systems (TA)	Autumn 1995, 1996
Zewail UST, Egypt	*Digital Design and Computer Architecture*	Autumn 2017, Spring 2018
	Operating Systems	Autumn 2017, Spring 2018
SQU, Oman	*Embedded Systems*	Winter 2016, 2017
	Introduction to Networking	Winter 2016
	Advanced Embedded Systems	Winter 2017
	Signals and Systems	Winter 2017
KAUST, Saudi Arabia	*Computer Architecture* (graduate class)	Winter 2012, 2013
German University in Cairo, Egypt	*Computer Architecture*	Winter 2007, 2008
	Processor Design	Autumn 2006, 2007
	Advanced Computer Lab	Autumn 2006, 2007
	Embedded Systems	Autumn 2007
Nanyang Technological University, Singapore	*Advanced Computer Arithmetic* (graduate class)	Winter 2006
	Advanced Computer Architecture (graduate class)	Autumn 2005
	Digital Circuits and Systems (Tutorials)	Autumn 2005
American University in Cairo, Egypt	*Digital Logic Design Lab*	Winter 2005
Stanford University, USA	*Advanced Computer Arithmetic* (graduate class, TA)	Winter 2003

University Service

- Member of the committee for the formulation of the graduate studies curriculum of the Electronics and Communications Department, 2006–2008.
- Member of the committee for the formulation of the undergraduate studies curriculum of the Electronics and Communications Department, 2007–2009.
- Member of the committee for the recording of the grades and results of the Civil Engineering Department, 2006–2017.

Industrial Experience

June 18–present **Principal Engineer** at Analog Devices Inc., Cairo, Egypt
Design and verification of digital blocks for 5G mm-waves chips

Sep 14–Dec 16 **Senior Consultant** at Wasiela, Maadi, Egypt
Application Specific Instruction set Processor design for communications systems

Sep 07–Jan 14 **Co-founder and CTO** at SilMinds, Maadi, Egypt
Managing research team, securing several rounds of funding, patenting
Datapath design, decimal floating point blocks compliant to the IEEE Std 754-2008

Nov 08–Dec 09 **Consultant** at Varkon Semiconductors, Maadi, Egypt
Digital receiver system for the DVB-C standard

Jan 04–May 05 **Consultant** at International Electrical Products, 6th of October City, Egypt
System on a chip for a digital satellite receiver

Oct 03–Aug 04 **Consultant** at National Authority for Remote Sensing and Space Sciences, Egypt
Preliminary design of the on-board computer controlling the operation of EgyptSat2

Jun 99–Sep 99 **Design Engineer** at Advanced Micro Devices, Sunnyvale, California, USA
Optimizations of the simulation code for a graphics hardware acceleration unit

Jul 96–Sep 96 **Visiting Researcher** at IBM T. J. Watson research center, New York, USA
Design of digital cells using Single Electron Transistors

Aug 94–Sep 94 **Visiting Researcher** at Imec, Leuven, Belgium
HF extraction of model parameters for High Electron Mobility Transistor devices

Research Work

1. Interests: My focus is on the datapath of digital designs from the devices that might be needed to the systems that perform the users' requirements. A good optimization of the arithmetic blocks results in an improved datapath which directly leads to a better overall design. A system level research (embedded systems and computer architecture) and device level research (current CMOS and future nanoelectronics) guide my work at the arithmetic units level. Digital typography is the second direction of my research and it is due to my deep interest in how the scholarly written information is presented.

   Supervised and Co-supervised 68 graduate students theses. (65 MSc, 3 PhD)

2. Awards

   - Elevated to Senior Member of IEEE in April 2009.
   - Stanford Graduate Fellowship 1998-2002.
   - 1995 IEEE Computer Society Upsilon Pi Epsilon award for academic excellence.

3. Research Services
   - Member of the working group and the ballot group on the IEEE Standard for Floating-Point Arithmetic (754–2008 published August 2008 and 754–2019 published July 2019).
   - Member of the ballot group on the IEEE Standard for Metric Practice (PSI-10).
   - Member of the ballot group on the IEEE Guide for Smart Gird (P2030).
   - Member of the working group and the ballot group on the IEEE Standard for Interval Arithmetic (1788–2015 published June 2015).
   - Reviewer for the IEEE Transactions on Computers, IEEE Transactions on VLSI, IEEE Transactions on Parallel and Distributed Systems, International Journal of Circuit Theory and Application, IEEE Transactions on Circuits and Systems-I, VLSI Design, IEEE Symposium on Computer Arithmetic, IEEE International Symposium on Circuits and Systems, and a number of other conferences.
4. Funding and Projects
   - Co-PI in the STDF grant "Micro-Coded Programmable Solution for a Class of OFDMA Wireless Applications", May 2009–May 2011.
   - Co-PI in the RDI grant "Promoting Egypt as the first Decimal Arithmetic Intellectual Property Cores Provider for financial applications in the world", August 2009–January 2011.
   - PI in the ITAC grant "Commercialization of Decimal HW Acceleration Technology for Greener Financial Computation", June 2011–March 2013.
   - Implementation Consultant in the NTRA grant "Design and Implementation of DVB-T/T2 Solution", July 2011–June 2013.

Granted Patents

1. R. Samy, H. A. H. Fahmy, T. Eldeeb, R. Raafat, Y. Farouk, M. Elkhouly, and A. Mohamed, "Decimal floating-point fused multiply-add unit," Apr. 2014. US Patent number 8,694,572
2. A. Mohamed, H. A. H. Fahmy, R. Raafat, Y. Farouk, M. Elkhouly, R. Samy, and T. Eldeeb, "Rounding unit for decimal floating-point division," June 2014. US Patent number 8,751,555
3. T. ElDeeb, H. A. H. Fahmy, and M. Y. Hassan, "Decimal elementary functions computation," July 2014. US Patent number 8,788,560
4. A. Mohamed, R. Raafat, H. A. H. Fahmy, T. Eldeeb, Y. Farouk, R. Samy, and M. Elkhouly, "Parallel redundant decimal fused-multiply-add circuit," Aug. 2014. US Patent number 8,805,917
5. R. Raafat, A. Mohamed, H. A. H. Fahmy, Y. Farouk, M. Elkhouly, T. Eldeeb, and R. Samy, "Decimal floating-point square-root unit using Newton-Raphson iterations," Aug. 2014. US Patent number 8,812,575
6. A. A. Ayoub and H. A. H. Fahmy, "BID to BCD/DPD converters," Sept. 2015. US Patent number 9,134,958
7. A. A. Ayoub, H. A. H. Fahmy, and T. Eldeeb, "DPD/BCD to BID converters," Sept. 2015. US Patent number 9,143,159
8. T. Eldeeb, H. A. H. Fahmy, A. Elhosiny, M. Y. Hassan, Y. Aly, and R. Raafat, "Decimal floating-point processor," Apr. 2016. US Patent number 9,323,521
9. M. S. BenSaleh, A. M. Obeid, Y. A. Alzahrani, A. F. Shalash, H. A. H. Fahmy, H. A. Sayed, and M. A. Aly, "Application specific instruction-set processor (ASIP) architecture having separated input and output data ports," Dec. 2019. US Patent number 10,496,596
10. M. S. BenSaleh, A. M. Obeid, Y. A. Alzahrani, A. F. Shalash, H. A. H. Fahmy, H. A. Sayed, and M. A. Aly, "Application specific instruction-set processor (ASIP) for simultaneously executing a plurality of operations using a long instruction word," June 2020. US Patent number 10,671,395

Publications

Books and Book Chapters:

1. H. A. H. Fahmy, *Redundant digit floating point system: Providing speed and flexibility.* VDM Verlag, Aug. 2009
2. M. A. ElSawaf, A.-L. ElShafei, and H. A. H. Fahmy, "Multi-core CPU air cooling," in *Heat Transfer — Engineering Applications* (V. Vikhrenko, ed.), ch. 16, pp. 377–400, InTech, Dec. 2011
3. W. A. A. Ibrahim, H. A. H. Fahmy, and A. H. Khalil, *Implementation of a Binary Floating Point Fused Multiply-Add Unit.* LAP LAMBERT Academic Publishing, Dec. 2012
4. H. A. H. Fahmy, "Decimal floating point number system," in *Embedded Systems Design with Special Arithmetic and Number Systems* (A. S. Molahosseini, L. S. de Sousa, and C.-H. Chang, eds.), ch. 5, pp. 89–111, Springer International Publishing, Mar. 2017. DOI: 10.1007/978-3-319-49742-6_5
5. W. S. Sayed, A. G. Radwan, and H. A. H. Fahmy, "Chaos and bifurcation in controllable jerk-based self-excited attractors," in *Nonlinear Dynamical Systems with Self-Excited and Hidden Attractors* (V.-T. Pham, S. Vaidyanathan, C. Volos, and T. Kapitaniak, eds.), ch. 2, pp. 45–70, Springer International Publishing, 2018. DOI: 10.1007/978-3-319-71243-7_2

Papers:

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1. H. A. H. Fahmy, "Design and implementation of AHD-2494, a 24-bit RISC processor on a VLSI chip," *'looking.forward' the IEEE Computer Society's Student Newsletter*, 1995. (fall issue)

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2. H. A. H. Fahmy and K. Ismail, "Analysis of a single-electron decimal adder," *Applied Physics Letters*, vol. 70, pp. 2613–2615, May 1997

(1999)

3. H. A. H. Fahmy, M. Morf, and R. Kiehl, "Potential functionality of multi-valued tunneling phase logic devices," in *European Conference on Circuit Theory and Design, Stresa, Italy, Session S10-II*, Aug. 1999
4. P. Hung, H. A. H. Fahmy, O. Mencer, and M. J. Flynn, "Fast division algorithm with a small lookup table," in *Thirty-Third Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, vol. 2, pp. 1465–1468, Oct. 1999
5. H. A. H. Fahmy and R. Kiehl, "Complete logic family using tunneling-phase-logic devices," in *The 11th International Conference on Microelectronics, ICM 99, Kuwait*, Nov. 1999

(2001)

6. H. A. H. Fahmy, A. A. Liddicoat, and M. J. Flynn, "Improving the effectiveness of floating point arithmetic," in *Thirty-Fifth Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, vol. 1, pp. 875–879, Nov. 2001

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7. H. A. H. Fahmy, A. A. Liddicoat, and M. J. Flynn, "Parametric time delay modeling for floating point units," in *The International Symposium on Optical Science and Technology, SPIE's 47th annual meeting (Arithmetic session), Seattle, Washington, USA*, July 2002

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8. H. A. H. Fahmy and M. J. Flynn, "The case for a redundant format in floating point arithmetic," in *Proceedings of the 16th IEEE Symposium on Computer Arithmetic, Santiago de Compostela, Spain*, June 2003
9. H. A. H. Fahmy and M. J. Flynn, "Rounding in redundant digit floating point systems," in *The International Symposium on Optical Science and Technology, SPIE's 48th annual meeting (Arithmetic session), San Diego, California, USA*, Aug. 2003

(2004)

10. H. A. H. Fahmy and M. J. Flynn, "An adder for a redundant digit arithmetic unit," in *COOL Chips VII, Yokohama, Japan*, Apr. 2004

(2005)

11. Y. He, C.-H. Chang, J. Gu, and H. A. H. Fahmy, "A novel covalent redundant binary booth encoder," in *The IEEE International Symposium on Circuits and Systems, (ISCAS), Kobe, Japan*, pp. 69–72, May 2005
12. S. Tawfik and H. A. H. Fahmy, "Error analysis of a powering method and a novel square root algorithm," in *The 17th IMACS World Congress Scientific Computation, Applied Mathematics and Simulation, Paris, France*, July 2005

(2006)

13. S. A. Tawfik and H. A. H. Fahmy, "Algorithmic truncation of minimax polynomial coefficients," in *The IEEE International Symposium on Circuits and Systems, (ISCAS), Kos, Greece*, pp. 2421–2424, May 2006
14. H. A. H. Fahmy, "Typesetting the Qur'an and its specific challenges to the TEX family," in *EuroTEX 2006: Proceedings of the* 16th *Annual Meeting of the European TEX Users, Debrecen, Hungary*, July 2006
15. H. A. H. Fahmy, "AlQalam for typesetting traditional Arabic texts," in *TUG 2006: The Annual Meeting of the International TEX Users Group, Marrakesh, Morocco*, Nov. 2006
16. S. K. Gopi, H. A. H. Fahmy, and V. A. Prasad, "Redundant adders consume less energy," in *The IEEE Asia-Pacific Conference on Circuits and Systems, (APCCAS), Singapore*, pp. 422–425, Dec. 2006

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17. H. A. H. Fahmy, "AlQalam for typesetting traditional Arabic texts," *TUGboat*, vol. 27, pp. 159–166, Jan. 2007. This paper groups the work already presented in EuroTEX 2006 and TUG 2006
18. A. A. Essawi, H. A. H. Fahmy, and N. H. Raafat, "Characterization of a coaxial mid-gap SB CNTFET inverter," in *IMNC, 20th International Microprocesses and Nanotechnology Conference, Kyoto, Japan*, Nov. 2007
19. A. M. Sherif and H. A. H. Fahmy, "Parameterized Arabic font development for AlQalam," *TUGboat*, vol. 29, pp. 79–88, Jan. 2008. Appeared originally in EuroBachoTEX 2007: the 17th Annual Meeting of the European TEX Users, Bachotek, Poland

(2008)

20. H. A. H. Fahmy and A. Elezabi, "Bipolar sequences correlator and squarer for multiple-access systems," in *Forty-Second Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, pp. 1837–1839, Oct. 2008
21. R. Raafat, A. Mohamed, R. Samy, T. ElDeeb, Y. Farouk, M. Elkhouly, and H. A. H. Fahmy, "A decimal fully parallel and pipelined floating point multiplier," in *Forty-Second Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, Oct. 2008
22. M. E. A. Ibrahim, M. Rupp, and H. A. H. Fahmy, "Power estimation methodology for VLIW digital signal processor," in *Forty-Second Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, Oct. 2008
23. A. M. Sherif and H. A. H. Fahmy, "Meta-designing parameterized Arabic fonts for AlQalam," *TUGboat*, vol. 29, pp. 435–443, Nov. 2008. Appeared originally in TUG 2008: The Annual Meeting of the International TEX Users Group, Cork, Ireland
24. A. M. A. Hussein, H. A. H. Fahmy, and M. M. Khairy, "Efficient hardware implementation for 802.16e double binary Turbo decoder," in *The International Conference on Microelectronics, ICM 2008, United Arab Emirates*, Dec. 2008
25. A. M. S. Tosson, H. A. H. Fahmy, and M. F. A. El-Yazeed, "DRUS: A new proposed interoperable DRM hardware-software solution," in *The 4th International Computer Engineering Conference, Giza, Egypt*, Dec. 2008

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26. M. M. Harb and H. A. H. Fahmy, "Deploying electronic vehicle identification (EVI) system in developing countries," in *The 6th International Workshop on Intelligent Transportation, Hamburg, Germany*, pp. 181–184, Mar. 2009
27. M. A. ElSawaf, H. A. H. Fahmy, and A.-L. ElShafei, "CPU dynamic thermal management via thermal spare cores," in *The 25th IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose, CA, USA*, pp. 139–145, Mar. 2009. DOI: 10.1109/STHERM.2009.4810755

28. A. Ahmedin, , S. Rashad, M. Fayez, M. A. Raouf, M. Sayed, H. A. H. Fahmy, A. K. Sultan, and M. Hamed, "A simplification in integral frequency offset estimation based on joint detection algorithm for WiMAX 802.16e," in *National Radio Science Conference, Cairo, Egypt*, Mar. 2009
29. H. A. H. Fahmy, R. Raafat, A. M. Abdel-Majeed, R. Samy, T. ElDeeb, and Y. Farouk, "Energy and delay improvement via decimal floating point units," in *Proceedings of the 19th IEEE Symposium on Computer Arithmetic, Portland, Oregon, USA*, pp. 221–224, June 2009
30. A. A. Al-Sallab, H. A. H. Fahmy, and M. Rashwan, "Hardware implementation of distributed speech recognition system front end," in *EUSIPCO, 17th European Signal Processing Conference, Glasgow, Scotland*, pp. 953–957, Aug. 2009
31. A. A. Al-Sallab, H. A. H. Fahmy, and M. Rashwan, "Optimized hardware implementation of FFT processor," in *The 4th International Design and Test Workshop (IDT), Riyadh, Saudi Arabia*, Nov. 2009. DOI: 10.1109/IDT.2009.5404139
32. K. ElWazeer, M. M. Khairy, H. A. H. Fahmy, and S. E.-D.Habib, "FPGA implementation of an improved channel estimation algorithm for mobile WiMAX," in *The International Conference on Microelectronics, ICM 2009, Morocco*, Dec. 2009
33. M. E. A. Ibrahim, M. Rupp, and H. A. H. Fahmy, "Code transformations and SIMD impact on embedded software energy/power consumption," in *ICCES09, International Conference on Computer Engineering and Systems, Cairo, Egypt*, Dec. 2009

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34. R. Samy, H. A. H. Fahmy, R. Raafat, A. Mohamed, T. ElDeeb, and Y. Farouk, "A decimal floating-point fused-multiply-add unit," in *Fifty-Third MidWest Symposium on Circuits and Systems, (MWSCAS), Seattle, Washington, USA*, Aug. 2010
35. H. Salah, H. Ahmed, T. ElShabrawy, and H. A. H. Fahmy, "Low-energy configurable syndrome/chien search multi-channel Reed Solomon decoder," in *The 23rd IEEE International System On Chip Conference, Las Vegas, Nevada, USA*, Sept. 2010
36. H. A. Ahmed, H. Salah, T. ElShabrawy, and H. A. H. Fahmy, "A low energy high speed Reed-Solomon decoder using decomposed inversionless Berlekamp-Massey algorithm," in *Forty-Fourth Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, Nov. 2010
37. A. Sayed-Ahmed, H. A. H. Fahmy, and M. Hassan, "Three engines to solve verification constraints of decimal floating-point operations," in *Forty-Fourth Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, Nov. 2010
38. K. Yehia, H. A. H. Fahmy, and M. Hassan, "A redundant decimal floating-point adder," in *Forty-Fourth Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, Nov. 2010
39. M. Hassan, T. ElDeeb, and H. A. H. Fahmy, "Algorithm and architecture for on-line decimal powering computation," in *Forty-Fourth Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, Nov. 2010
40. H. A. H. Fahmy, T. ElDeeb, M. Hassan, Y. Farouk, and R. Eissa, "Decimal floating point for future processors," in *The 22nd International Conference on Microelectronics, ICM 2010, Egypt*, Dec. 2010

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41. M. E. A. Ibrahim, M. Rupp, and H. A. H. Fahmy, "A Precise High-Level Power Consumption Model for Embedded Systems Software," *EURASIP Journal on Embedded Systems*, vol. 2011, 2011. Article ID 480805, doi:10.1155/2011/480805
42. M. Abdelall, A. F. Shalash, and H. A. H. Fahmy, "A reconfigurable baseband processor for wireless OFDM synchronization sub-system," in *The IEEE International Symposium on Circuits and Systems, (ISCAS), Rio de Janeiro, Brazil*, pp. 2385–2388, May 2011. DOI: 10.1109/ISCAS.2011.5938083
43. E. M. Abdel-Hamid, H. A. H. Fahmy, M. M. Khairy, and A. F. Shalash, "Memory conflict analysis for a multi-standard, reconfigurable turbo decoder," in *The IEEE International Symposium on Circuits and Systems, (ISCAS), Rio de Janeiro, Brazil*, pp. 2701–2704, May 2011. DOI: 10.1109/ISCAS.2011.5938162

44. M. Mahmoud and H. A. H. Fahmy, "A parallel combined binary/decimal fixed-point multiplier with binary partial products reduction tree," in *The 21st International Conference on Computer Theory and Applications (ICCTA), Alexandria, Egypt*, Oct. 2011
45. M. H. Amin, A. M. ElTantawy, H. A. H. Fahmy, and A. Khedr, "Efficient decimal leading zero anticipator designs," in *Forty-Fifth Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, Nov. 2011
46. A. Sayed-Ahmed, H. A. H. Fahmy, and R. Samy, "Verification of decimal floating-point fused-multiply-add operation," in *The Ninth ACS/IEEE International Conference on Computer Systems and Applications, (AICCSA), Sharm El-Sheikh, Egypt*, Dec. 2011

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47. A. H. M. Zaytoun, H. A. H. Fahmy, and K. M. F. Elsayed, "Implementation and evaluation of large interconnection routers for future many-core networks on chip," in *The 14th IEEE International Conference on High Performance Computing and Communications, Liverpool, UK*, June 2012
48. W. El-Reedy, A. A. El-Moursy, and H. A. H. Fahmy, "High performance memory requests scheduling technique for multicore processors," in *The 14th IEEE International Conference on High Performance Computing and Communications, Liverpool, UK*, June 2012
49. S. Y. Elsayed, H. A. H. Fahmy, and M. S. Khairy, "Residue codes for error correction in a combined decimal/binary redundant floating point adder," in *Forty-Sixth Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA*, Nov. 2012
50. A. Hazem and H. A. H. Fahmy, "LCAP - A Lightweight CAN Authentication Protocol for securing in-vehicle networks," in *10th escar Embedded Security in Cars Conference, Berlin, Germany*, Nov. 2012
51. H. A. Ahmed, H. Salah, T. Elshabrawy, and H. A. H. Fahmy, "Low energy high speed Reed-Solomon decoder using two parallel modified evaluator inversionless Berlekamp-Massey," in *19th IEEE International Conference on Electronics, Circuits, and Systems, Seville, Spain*, Dec. 2012
52. S. S. Mansour and H. A. H. Fahmy, "Experiences with Arabic font development," *TUGboat*, vol. 33, pp. 295–299, Dec. 2012

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53. M. A. Zidan, H. A. H. Fahmy, M. M. Hussain, and K. N. Salama, "Memristor-based memory: The sneak paths problem and solutions," *Microelectronics Journal*, vol. 44, pp. 176–183, Feb. 2013. DOI: 10.1016/j.mejo.2012.10.001
54. M. T. A. Osman, H. A. H. Fahmy, Y. A. H. Fahmy, and M. A. Elsabrouty, "Two programmable BCH soft decoders for high rate codes with large word length," in *The IEEE International Symposium on Circuits and Systems, (ISCAS), Beijing, China*, May 2013
55. M. N. H. Shaker, H. M. Hamed, A. F. Shalash, and H. A. H. Fahmy, "Efficient implementation of time de-interleaver for DVB-T2," in *International Conference on Communication, Control and Computer Engineering, (ICCCCE), Istanbul, Turkey*, Dec. 2013

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56. M. A. Zidan, A. M. Eltawil, F. Kurdahi, H. A. H. Fahmy, and K. N. Salama, "Memristor multi-port readout: A closed-form solution for sneak-paths," *IEEE Transactions on Nanotechnology (TNANO)*, vol. 13, pp. 274–282, Mar. 2014. DOI: 10.1109/TNANO.2014.2299558
57. M. T. A. Osman, H. A. H. Fahmy, Y. A. H. Fahmy, M. M. Elsabrouty, and A. Shalash, "Two extended programmable BCH soft decoders using least reliable bits reprocessing," *Circuits, Systems and Signal Processing by Springer*, vol. 33, pp. 1369–1391, May 2014. DOI: 10.1007/s00034-013-9709-x
58. M. M. Mahmoud, N. Soin, and H. A. H. Fahmy, "Design framework to overcome aging degradation of the 16 nm VLSI technology circuits," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol. 33, pp. 691–703, May 2014. DOI: 10.1109/TCAD.2014.2299713
59. A. S. Ahmed, H. A. H. Fahmy, and U. Kuehne, "Verification of the decimal floating-point square root operation," in *19th IEEE European Test Symposium (ETS), Paderborn, Germany*, May 2014
60. A. A. El-Moursy, W. El-Reedy, and H. A. H. Fahmy, "Fair memory access scheduling algorithms for multicore processors," *International Journal of Parallel, Emergent and Distributed Systems*, 2014. DOI: 10.1080/17445760.2014.922560

61. M. A. Zidan, A. S. Salem, H. A. H. Fahmy, and K. N. Salama, "Leakage analysis of crossbar memristor arrays," in *14th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA), Notre Dame, Indiana, USA*, July 2014. DOI:10.1109/CNNA.2014.6888635
62. A. A. Emara, M. Aboudina, and H. A. H. Fahmy, "Corrected and accurate verilog-A for linear dopant drift model of memristor," in *Fifty-Seventh MidWest Symposium on Circuits And Systems, (MWSCAS), College Station, Texas, USA*, Aug. 2014
63. A. Elhelw, A. A. El-Moursy, and H. A. H. Fahmy, "Time-based least memory intensive scheduling," in *The 8th IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-14), Aizu-Wakamatsu, Japan*, Sept. 2014
64. A. Maher and H. A. H. Fahmy, "Using range arithmetic in evaluation of compact models," in *16th GAMM-IMACS International Symposium on Scientific Computing, Computer Arithmetic and Validated Numerics (SCAN2014), Würzburg, Germany*, Sept. 2014
65. A. Hany, M. A. El-Moursy, and H. A. H. Fahmy, "Network of cores for large systems," in *9th IEEE International Conference on Computer Engineering and Systems (ICCES), Cairo, Egypt*, Dec. 2014
66. M. R. Soliman, H. A. H. Fahmy, and S. E.-D. Habib, "NoC-based many-core processor using CUSPARC architecture," in *26th IEEE International Conference on Microelecronics (ICM), Doha, Qatar*, Dec. 2014

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67. M. A. Zidan, A. S. Salem, H. Omran, H. A. H. Fahmy, and K. N. Salama, "Compensated readout for high density MOS-gated memristor crossbar array," *IEEE Transactions on Nanotechnology (TNANO)*, vol. 14, pp. 3–6, Jan. 2015. DOI: 10.1109/TNANO.2014.2363352
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