Lecture 6: Introduction to memories

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Overview

Inside large digital integrated circuits

Memories

- for temporary storage of results (registers),
- for the reduction of the information retrieval time (caches),
- or as the main store of information (main memory, virtual memory).

Control logic blocks handle the flow of information and assure that the circuit performs what is desired by the user.

Datapath blocks

- the real engine that performs the work.
- Mainly perform either some arithmetic or logic operations on the data.

Communications between all the elements is via wires usually arranged in the form of buses.

Classification: write, read, and erase

- Some technologies allow only a single writing and many reads, others allow re-writing.
- In some technologies a new writing overrides the older information, other technologies need an erase cycle.

How do you classify: clay, pottery, paper (pencils and pens), and classboards?

Classification: sequential versus random access

Random access means that we access any location (that you choose randomly) in the same amount of time.

- *Does the tape provide random access?*
- *Is the ROM a random access memory?*

Think of turning your eyes in a large room versus moving with your legs.

Classification: volatility

Do we loose the information when we turn the power off?

Non-volatile: such as ROM, Flash, CD, ...

Volatile: such as RAMs.

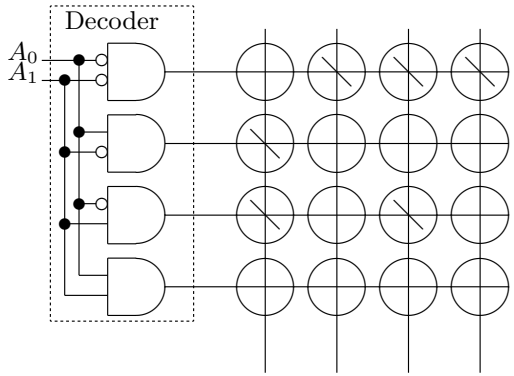
Contrast pottery to a statement written in the sand on the beach.

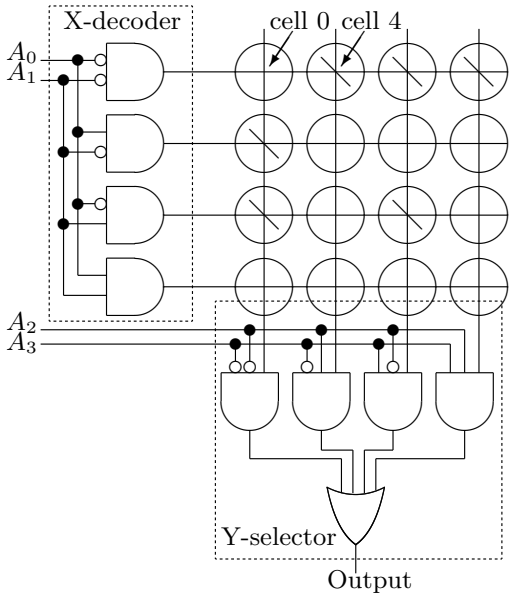
Access time and capacity

- Let us order the memories within a computer according to the time taken to retrieve the information.
- Now, let us do it according to the capacity.

Memory chip organization

The size of the memory grows exponentially with the number of bits in the address. Capacity $= \underbrace{2^{\text{address lines}} \times \text{data lines}}_{\text{Organization}}$.





What is the effect of the number of address lines and data lines on the speed? Why?

Inside the cell

The design of the cells leads to different memory technologies.

Wire	ROM
Fuse	PROM
Floating gate	EPROM, EEPROM, Flash
Latch	Static RAM
1T+1C	Dynamic RAM

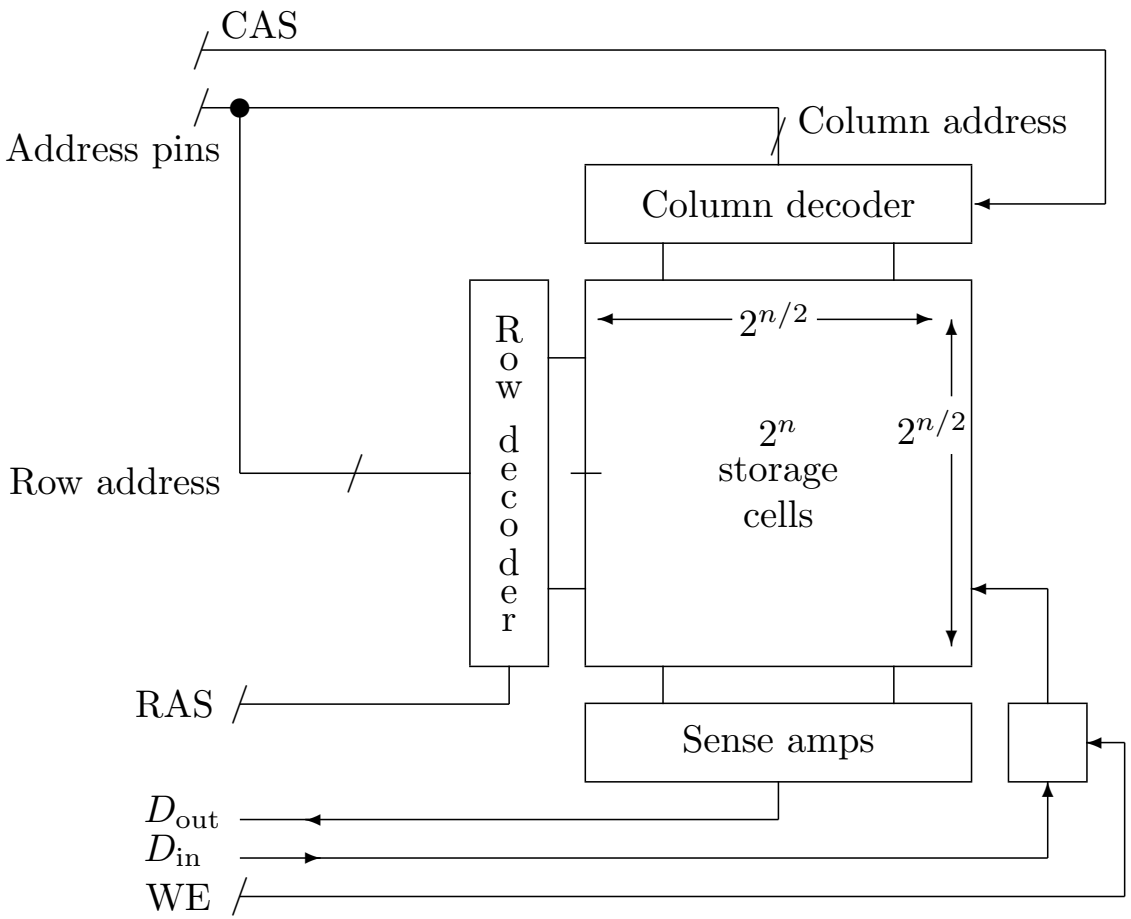
SRAM and DRAM

	Static RAM	Dynamic RAM
Cell composition	many transistors	1 T + 1 C
Cell size	bigger	smaller
Density	lower	higher
Capacity	smaller	larger
Speed	faster	slower
Power consumption	more	less
Retention	as long as power is on	needs refreshing

Which one do we use in caches? And in the main memory?

Back to DRAM chips

DRAM addressing is divided to rows and columns.



DRAM enhancements

The DRAM controller multiplexes the address and provides the RAS and CAS to the chip. To get a faster access, we use

- a fast page mode,
- SDRAM (S for synchronous) or DDR SDRAMs, or
- RDRAMs (R for Rambus).

Memory summary

A memory is an entity that holds the information for a later use.

- A memory with a small capacity fetches the information faster than another with a larger capacity. *Why?*
- A memory with a small capacity may use larger cells with more power to provide an even faster operation. *Why does a bigger cell and more power translate to speed?*
- Decoding is in levels. Remember your own algorithm to reach the room 8208.