Resolution Enhancements Techniques for the 45nm node and Beyond

by

Eng. Ahmed ElSayed Salem Farag Omran
Electronics and Communications Department
Faculty of Engineering, Cairo University

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the Requirement for the Degree of
MASTER OF SCIENCE
in
ELECTRONICS AND COMMUNICATIONS ENGINEERING

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Under the supervision of

Dr. Ahmed Hussien Khalil
Associate Professor
Elec. and Com. Dept.

Dr. Hossam A. H. Fahmy
Associate Professor
Elec. and Com. Dept.

Dr. Jochen Schacht
Senior AE Manager
Mentor Graphics Corp.

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Approved by the Examining Committee

Prof. Diaa AbdelMeged Khalil, Ain Shams University, Member

Prof. Dr. Serag El-Din ElSayed Habib, Cairo University, Member

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Associate Prof. Ahmed Hussien Khalil , Cairo University , Thesis Advisor

---

Associate Prof. Hossam A. H. Fahmy, Cairo University , Thesis Advisor

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Dr. Jochen Schacht , Mentor Graphics , Thesis Advisor

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ABSTRACT

Semiconductor manufacturing is continuously ramping up the yield of technology processes with transistor dimensions well below the exposure wave length. Pushing the limits of the exposure wave length to resolve patterns of smaller dimension introduces light diffraction effects in the lithography stage. Light diffraction prevents printing wafer patterns identical to the shapes drawn on the exposure mask. Resolution Enhancements Techniques (RET) are enabling these technologies to manufacture. In this thesis a complete survey about different Advanced Resolution Enhancements techniques (RET) in the 45nm node and beyond are discussed in details, talking particulary about Optical Proximity Correction (OPC) and Sub-resolution assist features (SRAF).

Optical Proximity Correction (OPC) is one of the main RET techniques that plays a major role enabling the advanced technologies to be realized. By changing the mask shapes to account for light diffraction, the final pattern on the wafer matches the desired target pattern. OPC achieves this by breaking the layout edges into smaller fragments and using models that simulate the exposure process to calculate the differences between printed shapes and desired shapes. These differences are referred to as Edge Placement Errors (EPE). OPC minimizes the EPE for all fragments in an iterative process. Traditional OPC uses a constant feedback factor. In this work, a dynamic feedback controller is introduced which uses a customized feedback factor for each fragment. This new algorithm shows improved performance in terms of OPC accuracy and run time. For the layout under test, the dynamic feedback algorithm achieves an improved OPC accuracy characterized by an EPE range of 1.5nm compared to a constant feedback controller characterized by an EPE range of 2.75nm (around $\sim$2X improvement in the OPC accuracy). Moreover, an up to 50% run time reduction is realized since the dynamic feedback controller is using only half of the iterations used by the constant feedback scheme. Additionally, the time for developing an OPC recipe using the dynamic feedback controller is shorter compared to the development time of constant feedback controller.

Sub-resolution assist features (SRAF), or scatter bars (SB), are very small non printable features which are added to a layout to provide critical process window enhancements in the lithography process. Traditionally, SRAF generation is based on geometric rules, which are extracted from a large amount of simulations and empirical wafer data from printing test masks. In this work, a new two step SRAF insertion flow (rule based SRAF seed placement followed by model based growth of the SRAF seeds concurrent to OPC) is compared to a traditional rule based SRAF insertion flow. Consistent SRAF seed placement is achieved by rules generated from inverse Lithography (Pixbar) results in test pattern. For a given annular illuminator a set of basic SRAF insertion rules is derived from process window analysis in test pattern. A medium size random logic interconnect layout (square and rectangular contact shapes) is used for SRAF recipe testing and process window analysis. The new SRAF insertion flow increases the common process window characterized by Depth of Focus (DOF) by 75% and reduces the maximum Mask Error Enhancement Factor (MEEF) from 8 to 5 when comparing to the traditional SRAF insertion flow. The rule based SRAF seed generation ends in ∼3.5% of the model based OPC (nmOPC) runtime over a full chip layout in a distributed cpu cluster. An analysis of DOF and MEEF is presented to compare process window for both SRAF insertion flows. The new SRAF insertion flow requires setting up a more complex nmSRAF insertion recipe which also requires more time for testing and debugging before tape out. During the early stage of process development, frequent changes of the illuminator would require changes to the SRAF recipe which may not be practical, however, in the stage of a more mature process closer to production, the new flow provides significant improvements in terms of performance and consistency of the resulting mask.

Keywords: Resolution Enhancement Techniques (RET), Optical Proximity Correction (OPC), Feedback Controller, OPC Convergence, Mask Error Enhancement Factor (MEEF), Sub-Resolution Assist Feature (SRAF) , Model-Based SRAF (MBSRAF), Scattering Bar (SBAR), Assist Features, Depth of Focus (DOF), Process Window

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I would like to thank Mentor Graphics Egypt for supporting the 2 conference papers out of the thesis and for providing me the necessary software and hardware to complete this work [1] [2].

Many thanks to my parents, my sister and my brother for their continuous support and encouragement during all working days.

Many thanks to my wife, for her cooperation, support and patience while I was working on my thesis.

Above all, I must thank God who gave me the strength and determination to complete the thesis.

DEDICATION

To my parents, my sister, my brother and my lovely wife.

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Chapter 1

Introduction

1.1 Motivation

The recent expansion in the semiconductor market has generated many new and challenging problems. Lithography has been one of the key drivers for the semiconductor industry. Moore's law [9] states that the number of devices on a chip doubles every 18 months as shown in Figure 1.1. The paper noted that the number of components in integrated circuits had doubled every year from the invention of the integrated circuit in 1958 until 1965 and predicted that the trend would continue "for at least ten years".

In the fabrication process of the cutting-edge technology nodes, it was proven that sub-wavelength microlithography can not survive without applying the approaches of Resolution Enhancements Techniques (RET) at different steps of the process [10] [11]. Sub-wavelength microlithography is depending on extending the utilization of the older lithography system with the newer technology nodes, even with the light source wavelength that is larger than the dimensions on the physical layout and mask reticle. This new situation impacted a lot the pattern quality printed on wafer, due to the optical diffraction of light beside some other factors. RET approaches were adopted to overcome these disturbances.

With emerging new technology nodes up to 28nm, and in the near future 20nm, 14nm and 10nm. All this has resulted in a strong need for a solid understanding of the different aspects of Lithography as well as Resolution Enhancement Techniques that may provide higher level of confidence in achieving the required technical goals in a given market-sensitive time window pushed by Moore's law.

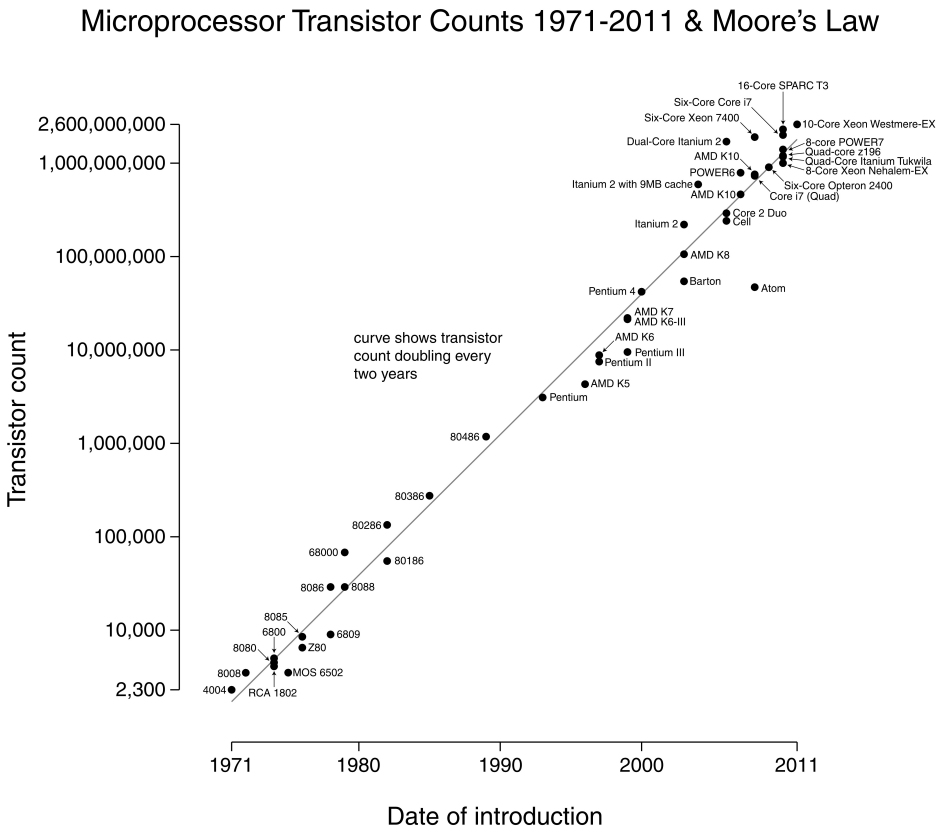


Figure 1.1: Moore's Law, Plot of CPU transistor counts against dates of introduction. Note the logarithmic vertical scale; the line corresponds to exponential growth with transistor count doubling every two years.
Source: *Moore's Law, Wikipedia [3]*

This thesis studies the different aspects of the Resolution Enhancement Techniques used currently in the industry for the 45nm technology node and beyond. Focusing on both, Optical Proximity Correction (OPC) and Sub-Resolutions Assist Features (SRAF), as key techniques to enable the advanced technologies to be realized. An innovative algorithm of OPC dynamic feedback controller is introduced

in this work which shows improved performance in terms of OPC accuracy and run time. A new two step SRAF insertion flow (rule based SRAF seed placement followed by model based growth of the SRAF seeds concurrent to OPC) is also implemented and compared to a traditional rule based SRAF insertion flow. The new flow provides significant improvements in terms of performance and consistency of the resulting mask.

1.2 Thesis Structure

Chapter 2 of the thesis starts by a comprehensive introduction about lithography steps. The Fourier Optics and how it affects the minimum dimension on wafer is then briefly discussed. Lithography metrics and how we measure its quality is reviewed in brief. The chapter ends with a description of the different types of RET known in the industry focusing on OPC and SRAF.

Chapter 3 focuses on the Optical Proximity Correction (OPC). The chapter starts with a quick overview of different OPC types (rule based OPC and model based OPC) followed by an explanation of the concept of constant feedback OPC algorithm. Introducing the new dynamic feedback OPC algorithm and its implementation, as well as testing results for a random logic layout. The new dynamic feedback OPC algorithm and traditional constant feedback OPC algorithm are compared and discussed with respect to OPC convergence and performance.

Chapter 4 describes the Sub-Resolution Assist features (SRAF), starting by the concept of SRAF insertion and how it works. An implementation of a new two step SRAF insertion flow (rule based SRAF seed placement followed by model based growth of the SRAF seeds concurrent to OPC)s is discussed in the following sections. The chapter ends by an analysis comparing the conventional rule based SRAF insertion flow and the new two step SRAF insertion flow in terms of accuracy and consistency.

The final chapter concludes the work of the thesis and highlights the results

and open issues witnessed in the study of advanced Resolution Enhancement Techniques. Several suggestions for future work are also listed.

Chapter 2

Advanced RET Techniques

2.1 Introduction

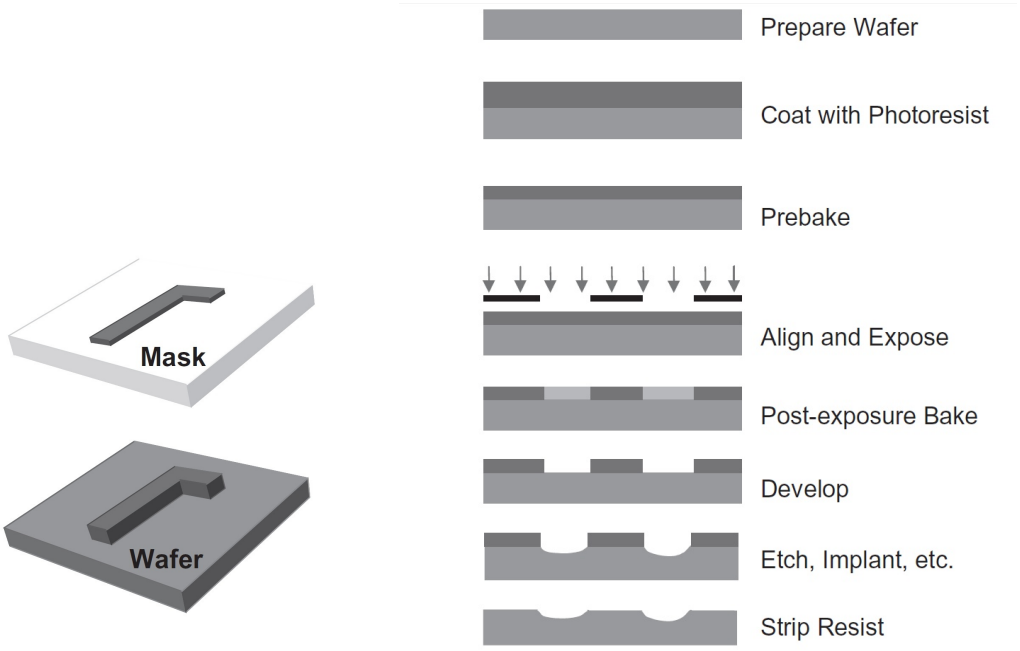
In this chapter a quick introduction about lithography steps will be illustrated. The Fourier Optics and how it affects the minimum dimension on wafer is discussed comprehensively. Lithography metrics and how we measure its quality is then briefly reviewed. The chapter ends with a description of the different types of Resolution Enhancements Techniques (RET) known in the industry.

2.2 Microlithography Technology

The fabrication of an integrated circuit (IC) consists of several physical and chemical processes performed on a silicon substrate. In general, the various processes used to make an IC fall into four categories: film deposition, patterning, semiconductor doping and film removal or etchings [8]. Films of both conductors (such as polysilicon, aluminum, tungsten and copper) and insulators (various forms of silicon dioxide, silicon nitride and others) are used to connect and isolate transistors and their components. Selective doping of various regions of silicon allows the conductivity of the silicon to be changed with the application of voltage. By creating structures of these various components, millions (or even billions) of transistors

can be built and wired together to form the complex circuitry of a modern microelectronic device. Fundamental to all of these processes is lithography, i.e. the formation of three-dimensional (3D) relief images on the substrate for subsequent transfer of the pattern into the substrate.

The word lithography comes from the Greek lithos, meaning stones, and graphia, meaning to write [12]. It means quite literally writing on stones. In the case of semiconductor lithography, our stones are silicon wafers and our patterns are written with a light sensitive polymer called a photoresist as shown on figure 2.1a. The general sequence of processing steps for a typical optical lithography process is: substrate preparation, photoresist spin coat, post-apply bake, exposure, post-exposure bake, development and postbake. Metrology and inspection followed by resist strip are the final operations in the lithographic process, after the resist pattern has been transferred into the underlying layer via etching or ion implantation. The typical sequence of lithographic processing step is shown in Figure 2.1b.



(a) Lithography is print on stone (b) Lithography Steps

Figure 2.1: Typical sequence of lithographic processing step
Source: *Fundamental Principle of Optical Lithography, By Chris Mack [7]*

Substrate preparation is intended to improve the adhesion of the photoresist material to the substrate. This is accomplished by one or more of the following processes: substrate cleaning to remove contamination, dehydration bake to remove water, and addition of an adhesion promoter. **Photoresist coating** is done by dispensing a small volume of the liquid resist onto a wafer. The wafer is then spun about its axis at a high rate of spin, flinging off the excess resist and leaving behind, as the solvent evaporates, a thin film of solid resist. After coating, the resulting resist film will contain between 20% and 40% by weight solvent. The **post-apply bake** , also called a softbake or a prebake, involves drying the photoresist after spin coat by removing this excess solvent. The main reason for reducing the solvent content is to stabilize the resist film.

Integrated circuits are fabricated by a series of patterning steps. Each new pattern must be placed on top of preceding layers, and proper overlay of the new layer to the circuit pattern already on the wafer is achieved during the **alignment** step by using specialized equipment. Photoresists are materials that undergo photochemical reactions when **exposed** to light. By exposing the resist selectively in some areas and not others, the pattern of the circuit can be created in the resist film. This selective exposure is accomplished in optical lithography by the imaging of a mask. Photomasks are sheets of glass, partially covered by an opaque material, usually chromium, that has been removed according to the pattern of the circuit. By shining light onto the mask, and then projecting the transmitted image onto the resist film, the pattern of one layer of the circuit is transferred to the resist film on the wafer.

Post-exposure bake is an optional baking step used to drive additional chemical reactions or the diffusion of components within the resist film. The main purpose of the post-exposure bake is reducing the standing wave effect [13]. **Development** is the step by which a resist is removed. The **postbake** (not to be confused with the post-exposure bake) is used to harden the final resist image so that it will withstand the harsh environments of implantation or etching.

After the small patterns have been lithographically printed in photoresist, these patterns must be transferred into the substrate. There are two main basic **pattern transfer** approaches: subtractive transfer (etching), and impurity doping (ion implantation). **Etching** is performed either using wet chemicals such as acids, or more commonly in a dry plasma environment. When the etching is complete, the resist is stripped leaving the desired pattern etched into the deposited layer. **Ion implantation** uses a beam of dopant ions accelerated at the photoresist-patterned substrate. The resist blocks the ions, but the areas uncovered by resists are embedded with ions, creating the selectively doped regions that make up the electrical heart of the transistors. After the imaged wafer has been processed (e.g., etched, ion implanted, etc.) the remaining photoresist must be finally removed by the **strip** operation. There are two classes of resist stripping techniques: wet stripping using organic or inorganic solutions, and dry (plasma) stripping.

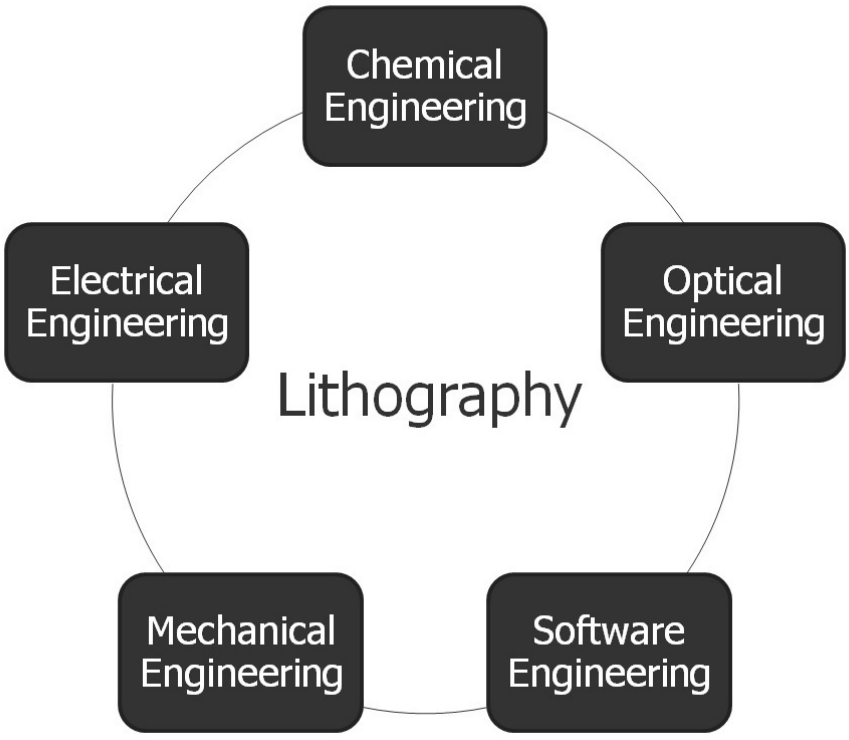


Figure 2.2: The science of lithography is related to many branches of engineering

The science of lithography is related to several parts of engineering. Several engineers from different backgrounds need to work together to develop a workable lithography process suitable for production. Optical background is needed to improve the image formation on wafer. Chemistry and material background is required to chose the photo resist kind needed for different process steps. Choosing the resist thickness and layer stake thickness (dielectrics and metallizations) needs a great knowledge of mechanics and materials to establish a good chemical mechanical polishing (CMP). Good experience of electrical engineering is also desired to improve the electrical characteristics of different devices supported by the lithography process (such as transistors, diodes, capacitors, etc..). Talented software engineers need to work to simulate different lithography and process related topics such as optics simulator, device simulators and electrical simulators to help reducing the development time of each part. A complete summary for different branches of engineering related to lithography are shown in Figure 2.2.

2.3 Fourier Optics

To understand the limitation of Microlithography in the advanced node and the need for the Resolution Enhancement Techniques the basic of imaging theory need to be explained including the behavior of an optical imaging system. Consider the generic projection system shown in Figure 2.3. It consists of a light source, a condenser lens, the mask, the objective lens and the resist coated wafer. The combination of the light source and the condenser lens is called the illumination system. In optical design terms, a lens is a system of (possibly many) lens elements. Each lens element is an individual piece of glass (refractive element) or a mirror (reflective element) or other optical element. The purpose of the illumination system is to deliver light to the mask (and eventually into the objective lens) with sufficient intensity, the proper directionality and spectral characteristics, and adequate uniformity across the field (i.e. across the mask). The mask consists of a transparent substrate on which a pattern has been formed. This pattern changes

the transmittance of the light and in its simplest form is just an opaque film. The light then passes through the clear areas of the mask and diffracts on its way to the objective lens. The purpose of the objective lens is to pick up a portion of the diffraction pattern and project an image onto the wafer which, one hopes, will resemble the mask pattern (or, more correctly, the desired pattern as expressed in the original design data).

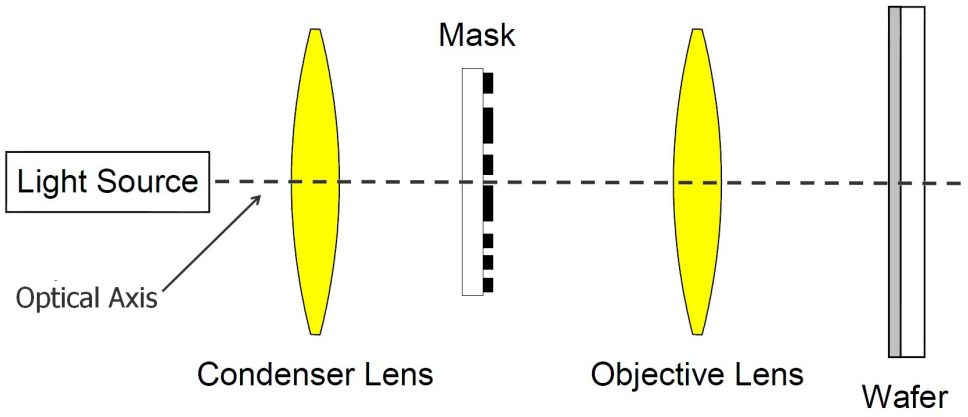


Figure 2.3: Block diagram of a generic projection imaging system

2.3.1 Diffraction

The first and most basic phenomenon occurring in projection imaging is the diffraction of light. Diffraction is usually thought of as the bending of light as it passes through an aperture, which is certainly an appropriate description for diffraction by a lithographic mask. Maxwells equations describe how electromagnetic waves propagate, but result in partial differential equations of vector quantities which, for general boundary conditions, are extremely difficult to solve without the aid of a powerful computer and sophisticated numerical algorithms. In order to establish a mathematical description of diffraction by a mask, we must first describe the electric field transmittance of a mask pattern $tm(x, y)$, where the mask is in the xy plane and $tm(x, y)$ has in general a magnitude and phase.

For a thin chrome-glass mask, the mask transmittance is binary: $t_m(x, y)$ is 1 in transparent region and 0 under the chrome. Let the xy plane be the diffraction

plane, that is, the entrance to the objective lens, and let z be the distance from the mask to this diffraction plane. We will also assume monochromatic light of wavelength λ and that the entire system is in a medium of refractive index n (i.e n=1 in air). Defining the spatial frequencies of the diffraction pattern (which are simply scaled coordinates in the $x' - y'$ plane) as $f_x = nx'/(z\lambda)$ and $fy = ny'/(z\lambda)$, the electric field of our diffraction pattern, $Tm(fx, fy)$, given by the Fraunhofer diffraction integral showing in Equation 2.1 (named after Joseph von Fraunhofer, who used a lens to create the far field diffraction pattern [14] [15]). The Fraunhofer diffraction integral describes the diffraction effect coming from the mask.

$$T_m(f_x, f_y) = \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} E_i(x, y) t_m(x, y) e^{-2\pi i(f_x x + f_y y)} dxdy \tag{2.1}$$

where E_i is the electric field incident on the mask (and is just 1 for our unit amplitude, normally incident plane wave). This equation is recognized as a Fourier transform. The diffraction pattern (i.e. the electric field distribution as it enters the objective lens) is the Fourier transform of the mask pattern transmittance (the electric field directly under the mask). This is the principle of Fourier optics [16].

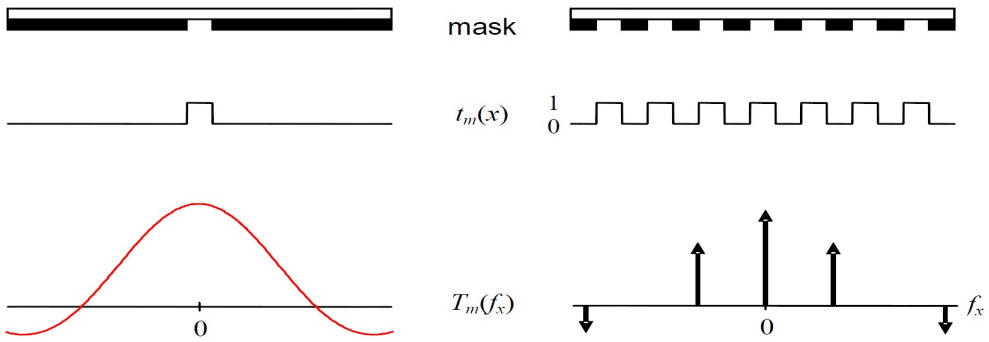


Figure 2.4: Two typical mask patterns, an isolated space and an array of equal lines and spaces, and the resulting Fraunhofer diffraction patterns assuming normally incident plane wave illumination.

Figure 2.4 shows two mask patterns, one an isolated space, the other a series of equal lines and spaces both infinitely long in the y-direction. The resulting one-dimensional mask field transmittance functions, $t_m(x)$, looks like a square pulse.

The Fourier transforms for normally incident plane wave illumination ($E_i = 1$) are computed directly from Equation 2.1 or found in tables or textbooks and are also shown in Figure 2.4. The isolated space gives rise to a *sinc* function ($sin(x)/x$) diffraction pattern as in Equation 2.2, and the equal lines and spaces yield discrete diffraction orders as in Equation 2.3. where δ is the Dirac delta function, w is the spacewidth and p is the pitch (the linewidth plus the spacewidth). The delta function is the mathematical representation of a point of light, for more information about delta function please refer to Appendix C of (Mack, 2008)[7] .

$$\text{Isolated space: } Tm(fx) = \frac{\sin(\pi w f_x)}{\pi f_x} \tag{2.2}$$

$$\text{Dense space: } Tm(fx) = \frac{1}{p} \sum_{j=-\infty}^{+\infty} \frac{\sin(\pi w f_x)}{\pi f_x} \delta(f_x - \frac{j}{p}) \tag{2.3}$$

2.3.2 Imaging Lens

In general, the diffraction pattern extends throughout the xy plane. However, the objective lens, being only of finite size, cannot collect all of the light in the diffraction pattern. Only those portions of the mask diffraction pattern that fall inside the aperture of the objective lens contribute to form the image. We can describe the size of the lens aperture by its radius, but a more common definition uses the maximum angle of diffracted light that can enter the lens. Consider the geometry shown in Figure 2.5. Light passing through the mask is diffracted at various angles. Given a lens of a certain size placed at a certain distance from the mask, there is some maximum angle of diffraction, θ_{max}, for which the diffracted light propagates into the lens. Light emerging from the mask at larger angles misses the lens and is not used in forming the image. The lens aperture is characterised by its numerical aperture, defined as the sine of the maximum half-angle of diffracted light that can enter the lens times the index of refraction of the surrounding medium, n as shown in Equation 2.4.

$$NA = n \sin \theta_{max} \tag{2.4}$$

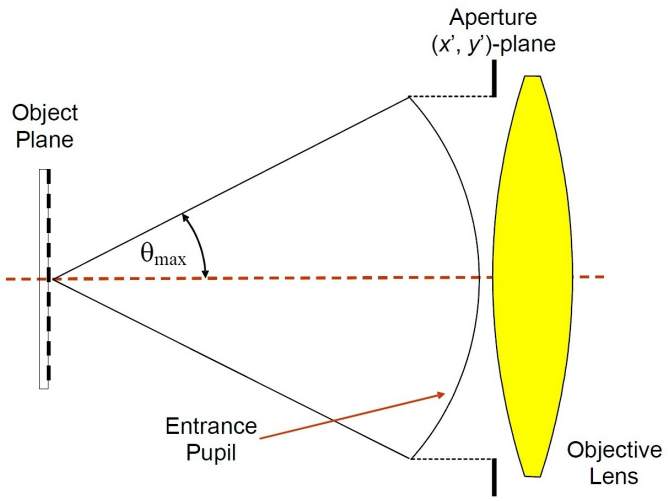


Figure 2.5: The numerical aperture is defined as $NA = nsin\theta_{max}$ where θ_{max} is the maximum half-angle of the diffracted light that can enter the objective lens, and n is the refractive index.

A large numerical aperture means that a larger portion of the diffraction pattern is captured by the objective lens. For a small numerical aperture, much more of the diffracted light is lost. We can prove that the maximum spatial frequency that can enter the objective lens is given by NA/λ [7]. The system resolution power is a function of NA/λ. Consider the case of a mask pattern of equal lines and spaces. The resulting diffraction pattern is a series of discrete diffraction orders. In order to produce the image of the original mask pattern, it is necessary to capture the zero diffraction order and at least one higher order. If the light illuminating the mask is a normally incident plane wave, the diffraction pattern will be centered with respect to the objective lens. Since the positions of the $\pm 1^{st}$ diffraction orders in frequency space are given by 1/p, the requirement that a lens must capture these diffraction orders to form an image puts a lower limit on the pitch that can be imaged. Thus, the smallest pitch (pmin) that still produces an image will put the first diffraction order at the outer edge of the objective lens as in Equation 2.5.

$$\frac{1}{p_{min}} = \frac{\lambda}{NA} \tag{2.5}$$

If we let R represent the linewidth or the spacewidth of the equal line/space pattern, the resolution limit will be given by Equation 2.6.

$$R = 0.5\frac{\lambda}{NA} \tag{2.6}$$

This equation is often called the theoretical resolution limit of an imaging system. Note that several assumptions were made in deriving this resolution equation: a mask pattern of equal lines and spaces was used, and the illumination was a monochromatic wavelength normally incident plane wave (coherent illumination). This equation defines the pitch, the smallest pitch that can be imaged. As a result, this approximate resolution expression is often generalized as in Equation 2.7. Such resolution equation are best interpreted as scaling equations, with K_1 as the scaled resolution. More discussion about K_1 follows in the upcoming sections.

$$R = K_1\frac{\lambda}{NA} \tag{2.7}$$

2.4 Lithography Metrics

In order to understand the lithography in depth we need to develop methods to quantify image quality. In addition, lithographers very often have to determine the optimal printing techniques among many approaches. These options may include various resolution enhancement techniques, photo resist tones, and exposure system parameters such as wavelength, NA, and illumination settings. Thus, there is also a need to quantify robustness of image so that they can be compared. Suitable metrics are discussed below. These include critical dimension, contrast, normalized image log slope, exposure latitude, depth of focus, mask error enhancement factor and process variation band.

2.4.1 Critical Dimension (CD)

In placing patterns onto silicon via lithography, critical dimension accuracy (CD) is the fundamental concern. Achieving accurate CD means that the sizes of the final silicon patterns match the desired sizes. A 10% error tolerance in CD is normally cited as acceptable. Different types of accuracy measures are often used such as : CD uniformity, CD linearity, line-end shortening and corner rounding [17].

The CD uniformity is a one-dimensional criteria that applies to line widths of long lines. The term refers to variations in printed line width observed for a given target line width as the spacing to adjacent lines is varied. The iso/dense bias is an example of a CD uniformity issue. CD linearity refers to the accuracy at which line widths are printed for a range of different target values. Line-end shortening is a large pullback is often seen at line-ends at the smallest dimension. This can be a significant problem when overlap between layers is required. The effect of the bandlimited optics system on corners is that corners become rounded on the wafer. Again, overlay concerns warrant that corner rounding should be minimized [4].

2.4.2 Contrast

Aerial Image Contrast is a classic image metric useful for small equal line/space patterns and simple patterns, the image contrast is defined as the difference between the maximum and minimum intensities of an image divided by their sum [7] as defined in Equation 2.8 and shown in Figure 2.6. Higher contrast value reflects better image fidelity. Contrast is a simple metric that works well with periodic pattern (dense structure). For Isolated structure $I_{min} = 0$ and $I_{max} \geq 0$, image contrast is not a suitable metric anymore because the contrast is always equal to 1 regardless of the opening width of mask [7].

$$Contrast = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \tag{2.8}$$

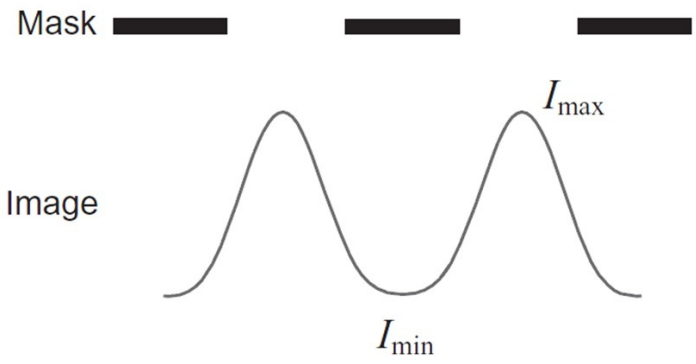


Figure 2.6: Aerial Image Contrast

2.4.3 Normalized Image Log Slope (NILS)

Image Log Slope (ILS) is the slope of the logarithm of the aerial image, usually defined at the nominal edge of the designed pattern [7]. Normalized Image Log Slope (NILS) is the slope of the logarithm of an aerial image, measured at the desired photoresist edge position, normalized by multiplying by the nominal resist feature width (w) [7]. Generally, the sign of the slope is adjusted to be positive.

$$ILS = \frac{1}{I}\left|\frac{dI}{dx}\right| = \left|\frac{d\ln(I)}{dx}\right| \tag{2.9}$$

$$NILS = w\frac{\mathrm{d}\ ln(I)}{dx} \tag{2.10}$$

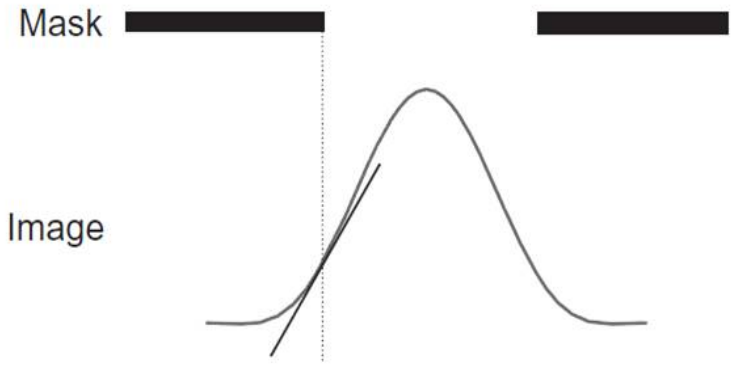


Figure 2.7: Normalized Image Log-Slope (NILS)

2.4.4 Exposure Latitude (EL)

Exposure Latitude(EL) is the range of exposure energies that can be tolerated to keep the linewidth within specified limits [6] (EL usually expressed as a percent variation from the nominal energy dose). Consider imaging of a nominally 150nm line with a threshold resist and a ±10% dimension tolerance (A ±10% tolerance is typical for photolithography), as shown in Figure 2.8. Suppose the dose to print the feature within specification ranges from $2.7E_o$ to $3.2E_o$, and $3E_o$ is the dose to print the line on size, the dose is allowed to deviate from

$$\frac{2.7-3}{3} \times 100\% = -10\% \tag{2.11}$$

to

$$\frac{3.2-3}{3} \times 100\% = 6.7\% \tag{2.12}$$

about the nominal. The exposure latitude is 16.7% in this case.

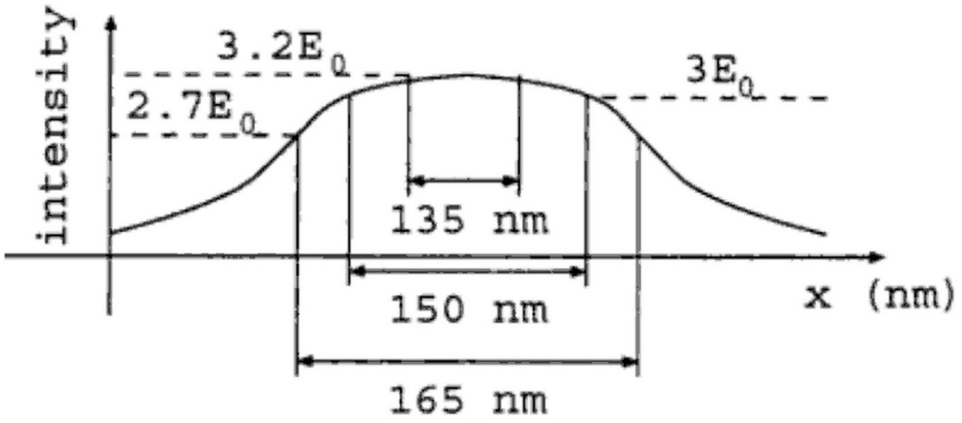


Figure 2.8: Exposure latitude is the maximum amount of dose variation which can be tolerated before the printed pattern dimension falls outside the specification.
Source: *Resolution Enhancement Techniques in Optical Lithography, By A. Wong* [4]

2.4.5 Depth of Focus (DOF)

Depth of Focus (DOF) is the total the range of focus that keeps the resulting printed feature within a specified limits. In other hand, DOF represents the range of defocus (in nm) around nominal focus in which the printed contour on wafer would print within acceptable percentage of the target layer as desired by the designer (10% usually used in photolithography as an acceptable variation in line width). Consider imaging of a nominally 150nm line with a threshold resist and a ±10% dimension tolerance as shown in Figure 2.9. Suppose the dose is set such that the nominal dimension results at a focus of 50nm, and the feature size is 165nm at the focus levels of −300nm and 350nm, the focus can deviate from

$$-300 - 50nm = -350nm \tag{2.13}$$

to

$$350 - 50nm = 300nm \tag{2.14}$$

about the nominal focus. The depth of focus is 650nm.

Depth of Focus is well known in photography (also known as depth of field). The area within the depth of field appears sharp, while the areas in front of and beyond the depth of field appear blurry as shown in Figure 2.10.

2.4.6 Mask Error Enhancement Factor (MEEF)

Mask Error Enhancement Factor (MEEF) , first discussed by Wilhelm Maurer [18], is defined as the incremental change in the final resist feature size per unit change in the corresponding mask feature size as described in Equation 3.1. A value of 1 implies a linear imaging of mask features to the wafer. A MEEF of 2 example is shown in Figure 2.11. A 1nm CD error on the mask (assuming CD on the mask are

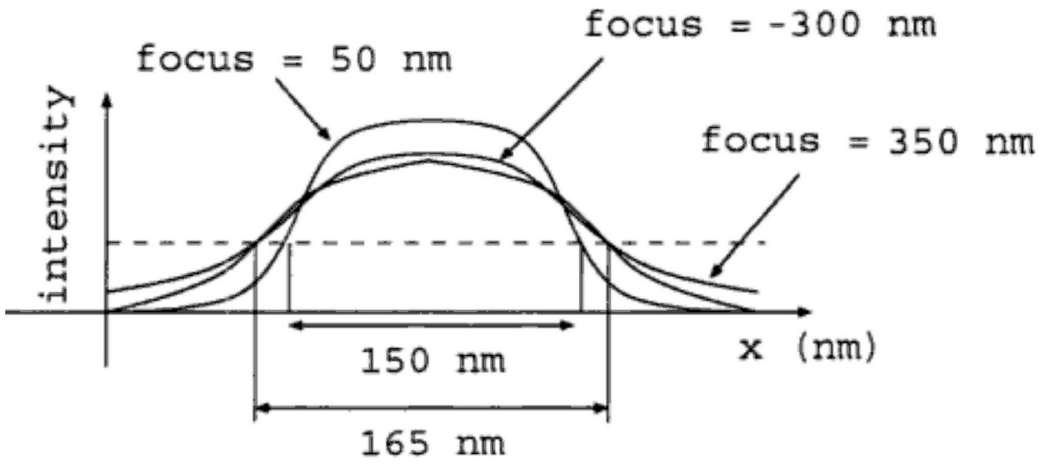


Figure 2.9: The depth of focus is the maximum amount of focus change that can be tolerated before the printed pattern size falls outside the specification.
Source: *Resolution Enhancement Techniques in Optical Lithography, By A. Wong* [4]

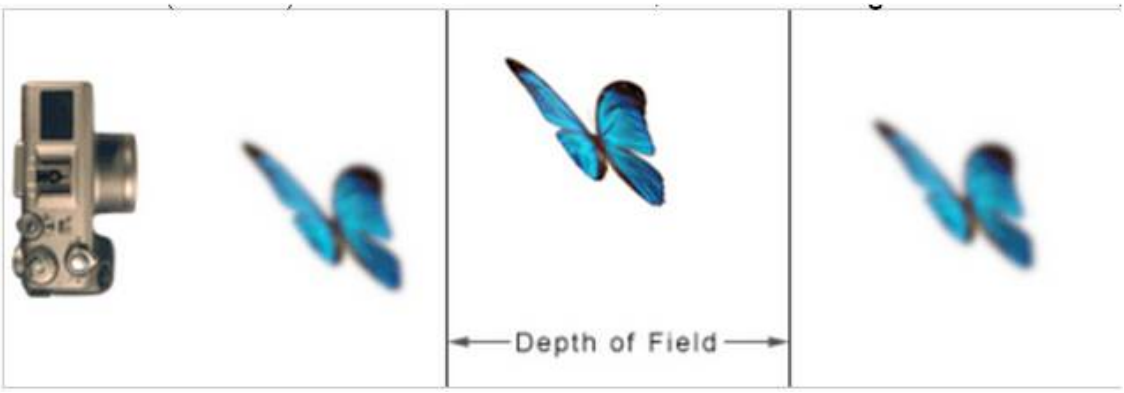


Figure 2.10: DOF in Photography:- the area within the depth of field appears sharp, while the areas in front of and beyond the depth of field appear blurry.
Source: *Resolution Enhancement Techniques in Optical Lithography, By A. Wong* [5]

expressed here in wafer dimensions) would result in a 2nm CD error on the final resist feature.

$$MEEF = \frac{\Delta CD_{wafer}}{\Delta CD_{mask}} \tag{2.15}$$

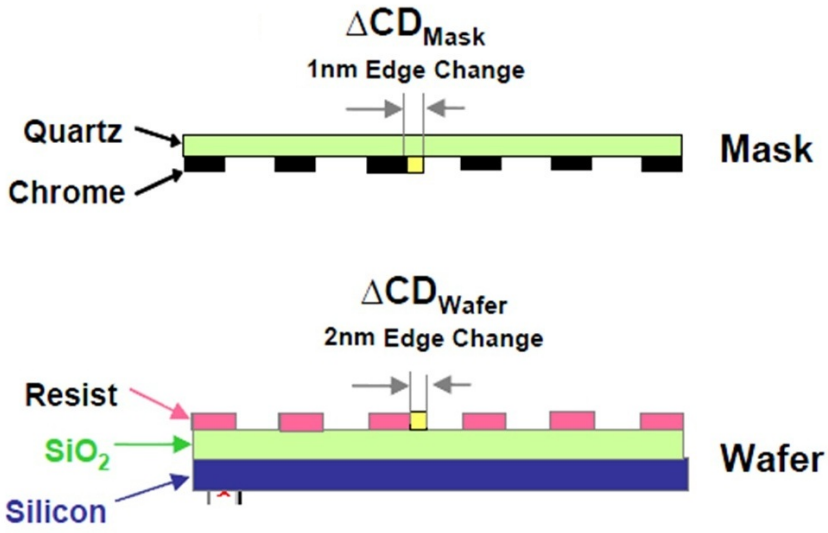


Figure 2.11: MEEF = 2 Example

2.4.7 Process Variability Band (Pvband)

A Process Variability Band (PVband) is defined as the physical representation of the layout sensitivity to process variations. One way to calculate a PVband is to calculate the pattern transfer image at multiple process conditions followed by a series of Boolean operations to extract the maximum edge placement and the minimum edge placement as indicated in Figure 2.12. The region inside the PV-band corresponds to the constantly printing region while the band itself (grey), corresponds to the variability region that indicates probable locations of the printing/non-printing boundary.

As Figure 2.13 explains, the PVband is an uncertainty region between areas that will always print and areas that will never print, thus providing a mechanism to

assess the likelihood of a particular topology transfer. In other words, the smaller the PVband is, the higher the probability of correct pattern transfers, independent of the process under study. PVband width shows how printing responds to process variations by representing the simulated contour extremes as a function of process variation (such as focus and exposure). Since the width of the PVband represents how much the image changes through focus and dose, it is inversely proportional to the process window. Thus, a decreasing PVband width correlates to increasing image quality, so a minimal PVband width (w) is desired [19] [20].

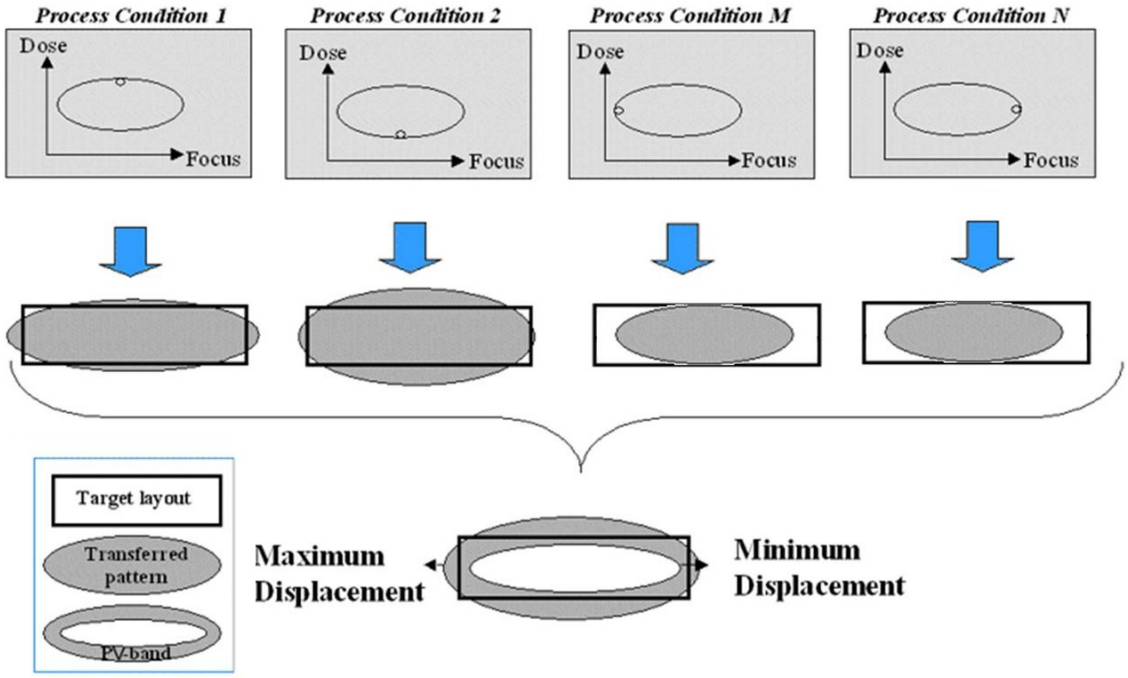


Figure 2.12: Generation of PVband from images at multiple process conditions.

2.5 Resolution Enhancement Techniques

Lithography is limited by both the minimum feature size and the cost of the used equipment. We illustrated that further reducing in Critical Dimension (CD) need to introduce an illumination system with lower wavelength (λ) and projection lens with higher Numerical Aperture (NA). It was proven that decreasing the value of

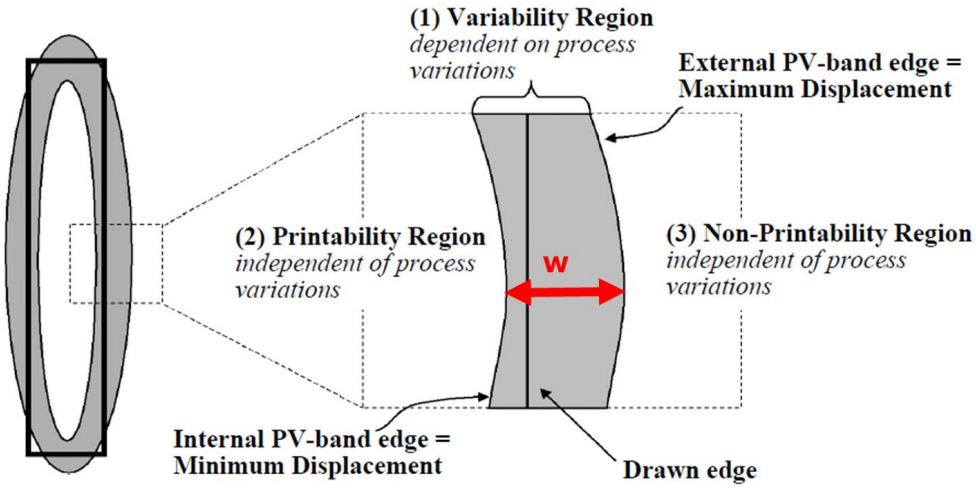


Figure 2.13: Process Variability Pvband (Pvband), the target is to minimize width (w) of Pvband for all design features.

the wavelength λ and increasing the value of Numerical Aperture (NA) will highly affect the Depth of Focus (DOF) [4] . Although we can't decrease the value of the wavelength λ to less than 157nm as it would need different lens and photoresist material which may increase the cost of exposure tool. Increasing NA needs a larger size of projecting lens which will increase the complexity of the lens design, cost and weight. Thus, the Resolution Enhancement Techniques (RET) are introduced to decrease the value of K_1 described in Equation 2.6. By decreasing the value of K_1, the value of minimum Critical Dimension (CD) will decrease. This will not affect the value of the DOF illustrated in Equation **??**.

To see how resolution enhancement techniques can reduce K_1, consider the basic properties of any electromagnetic wave: amplitude, phase and propagation direction. These parameters are three handles to manipulate and improve the imaging process. Each of the main RET approaches controls and manipulates one of the light handles at the mask in a process known as wavefront engineering. Optical Proximity Correction (OPC) is targeted at wavefront amplitude, Phase-Shift Masks (PSM) at wavefront phase, and Off-Axis Illumination (OAI) at wavefront direction. The best method to optimize electromagnetic wavefront in a lithography system is during the mask manufacturing side, because it is changing with different layers,

while the rest of the lithographic system is kept constant (i.e. NA, λ, Source parameters, etc.) [8].

2.5.1 Optical Proximity Correction (OPC)

Optical proximity correction (OPC) is a photolithography enhancement technique commonly used to compensate for image errors due to diffraction or process effects. Images on wafer appear with irregularities such as line widths that are narrower or wider than designed, 2D optical defects such as corner rounding and line-end shortening. There are local CD changes, which when reaching the extreme, become missing patterns or pattern touching as shown in Figure 2.14. OPC compensate these image defects by adjusting the pattern on the mask used [4]. OPC can maintain the edge placement integrity of the original design, after processing, into the etched image on the silicon wafer. Figure 2.15 shows how the mask pattern edge is modified to bring the edge of the wafer image as close to the desired position as possible. The line ends are enlarged with the so-called hammerhead to maintain the line width and length. The inside corner is carved in while the outside corner is beefed up. The line edge facing a line end is moved slightly away from the line end. The two islands are enlarged to compensate for the reduced image size [6] .

The basis of edge correction lies in relocating the edge of the mask pattern so that the image edge falls on the desired position. Figure 2.16 shows the direction in which to move the pattern edge. The exact amount to move is related but not equal to the amount of edge error. There are two main ways to assign the changes at the mask pattern edge: rule-based and model-based.

a) Rule-based OPC

Rule-based OPC is done via experimentally determined OPC rules. Such rules include the bias table for 1D patterns and serif or hammerhead rules for 2D patterns. With the help of design rule checking on CAD tools, OPC can be performed automatically. For correction efficiency, OPC rules are established by only considering the pattern itself or its nearest-neighboring patterns, thus it is only applicable for

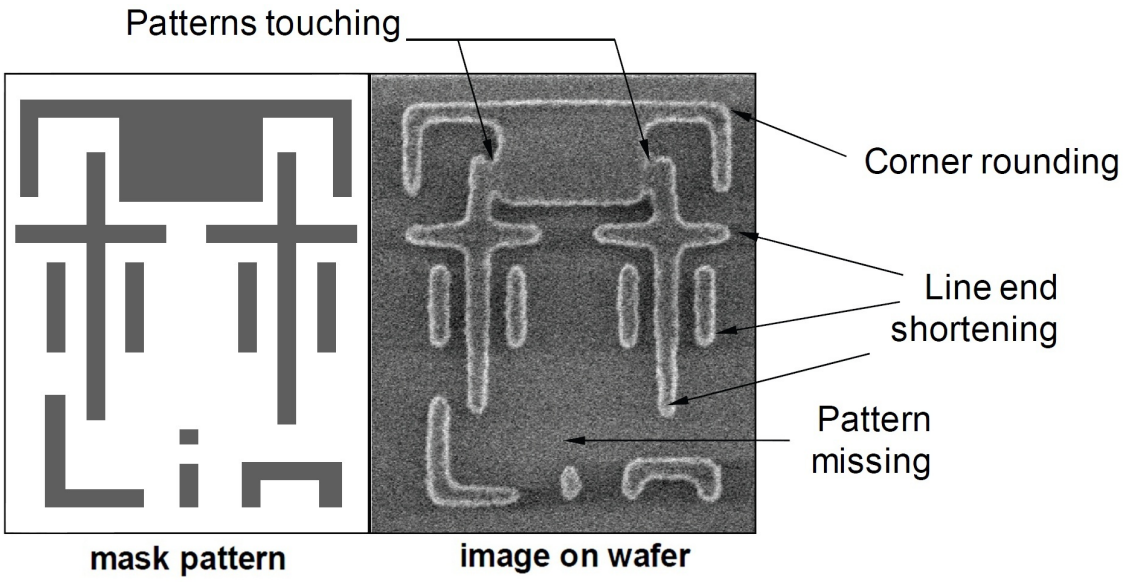


Figure 2.14: 2D and other proximity deffects due to diffraction and process effects. ***Source:*** *Optical Lithography, Here is Why, By Burn J. Lin* [6]

correcting loosely distributed ASIC or patterns with a fixed environment, such as memory cells. Figure 2.17 shows a bias table to dictate the change of features according to their width and space and the distance from a neighboring feature. The lighter shades indicate addition to the feature; the darker shades indicate subtraction. Rule-based OPC is applicable for a wide variety of technology nodes (0.18 m, 0.13 m, etc.) and exposure systems (i-line, KrF, ArF, etc.) [21].

b) Model-based OPC

The model-based OPC techniques are different from rule-based OPC in that simulation models are used to compute the wafer results and modify edges on the mask to improve the simulated wafer results. Model-based OPC is capable of more general corrections, but can require longer OPC time, because simulation is time-intensive [17]. By dividing the original design into edge segments (called Fragments), each of the fragments can be individually moved during the Model-based OPC process. For each fragment, we insert an imaginary line perpendicular to it named site, at which a property named Edge Placement Error (EPE) is calculated. EPE is defined as the distance between desired target edge on wafer and the actual printing contour on wafer as shown in Figure 2.18.

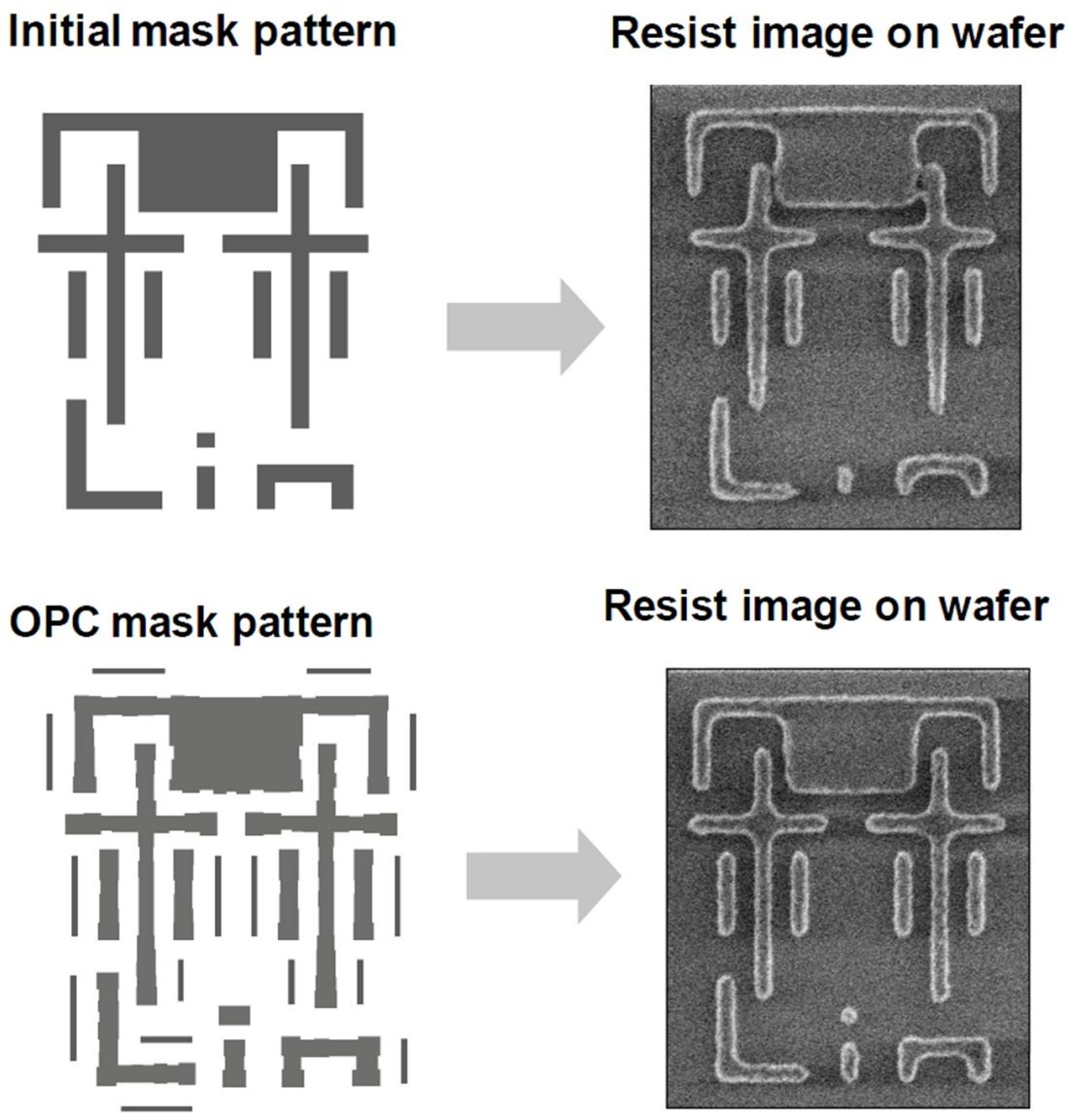


Figure 2.15: Optical Proximity Correction (OPC) by edge bias.
Source: *Optical Lithography, Here is Why, By Burn J. Lin* [6]

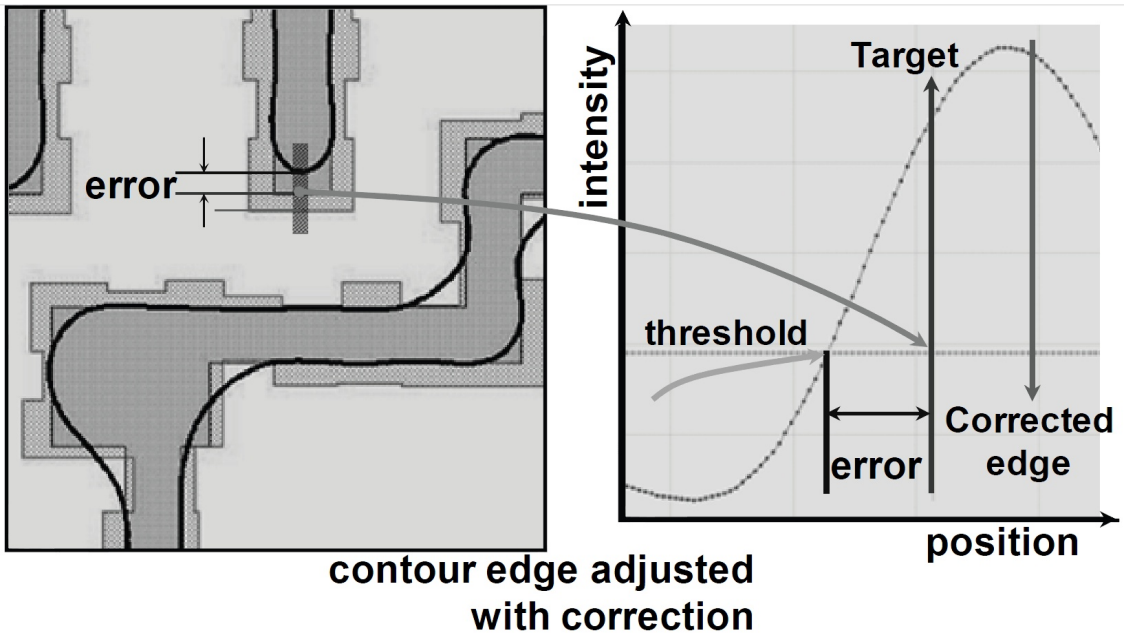


Figure 2.16: Correction by moving the edge to meet the threshold.
Source: *Optical Lithography, Here is Why, By Burn J. Lin* [6]

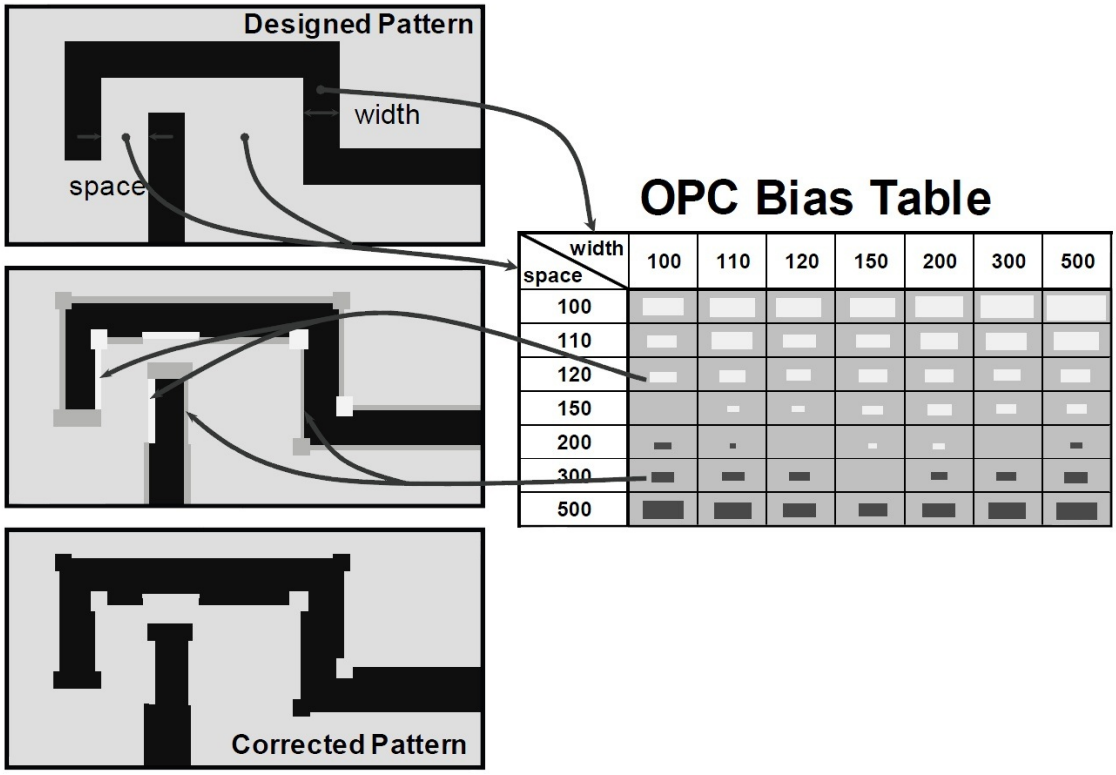


Figure 2.17: Rule-based OPC from a lookup table.
Source: *Optical Lithography, Here is Why, By Burn J. Lin* [6]

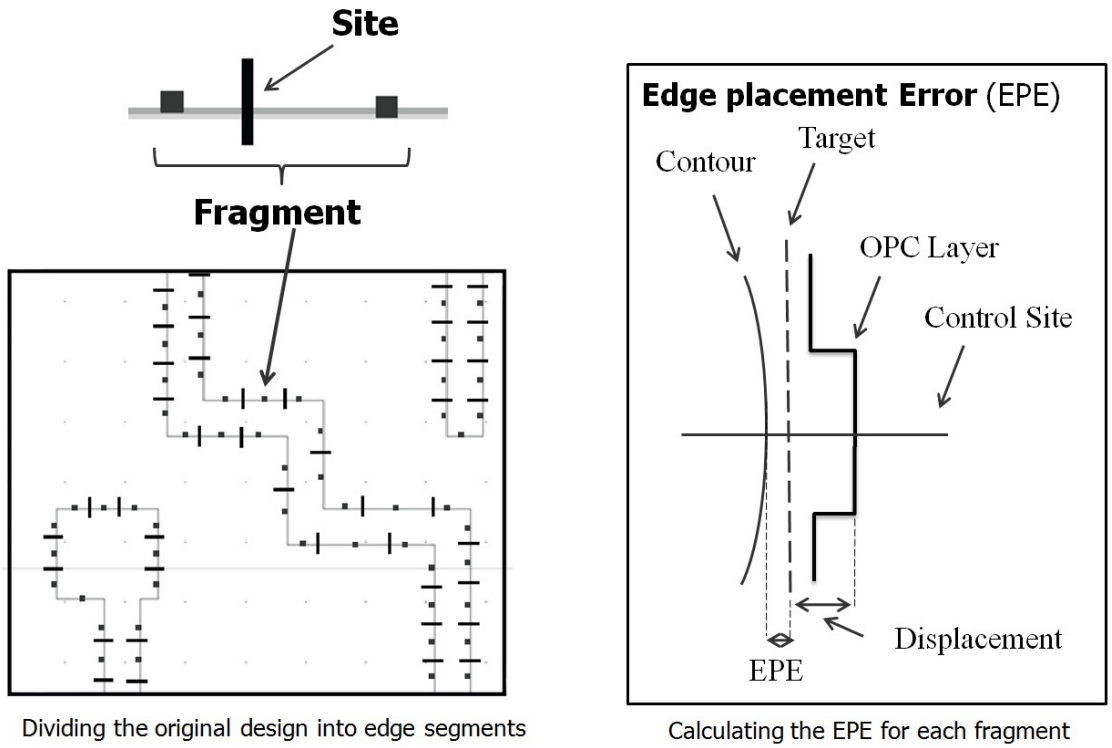


Figure 2.18: OPC system components.

The goal of OPC is to achieve an EPE equals zero for all fragments. The EPE is used as a cost function to determine the best placement on mask for each fragment. As the OPC progresses, small perturbation polygons are added and subtracted from the mask to result in a mask which improves edge placements on the wafer. The OPC system works as a control system in which the line width on mask is changed iteratively to achieve the desired line width on wafer (i.e the desired target) as shown in Figure 2.19. The fragment movement at each OPC iteration is determined usually by multiplying the EPE value by a constant feedback factor (usually a constant value of feedback factor equals -0.4 is used). More discussion about feedback factor is in chapter 3. The overall OPC system and the components required to implement OPC is described in detail in (Cobb, 1998)[17].

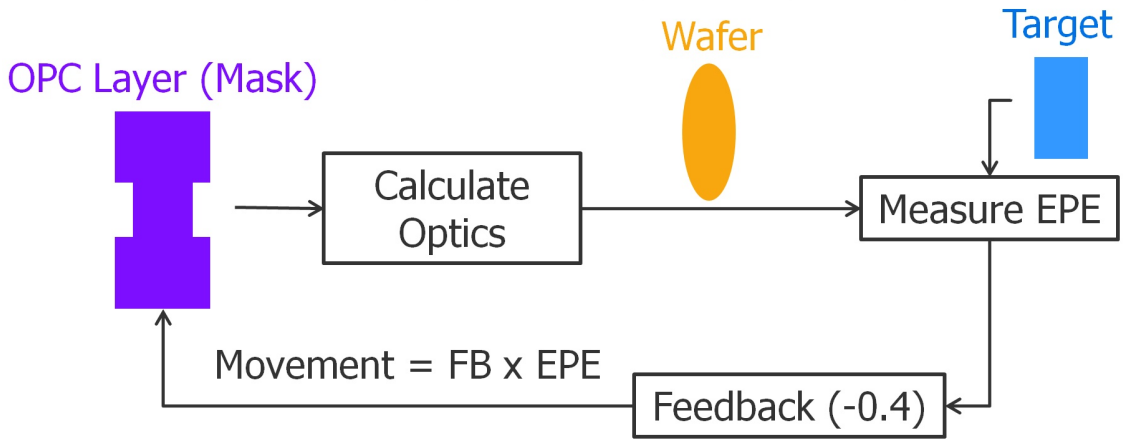
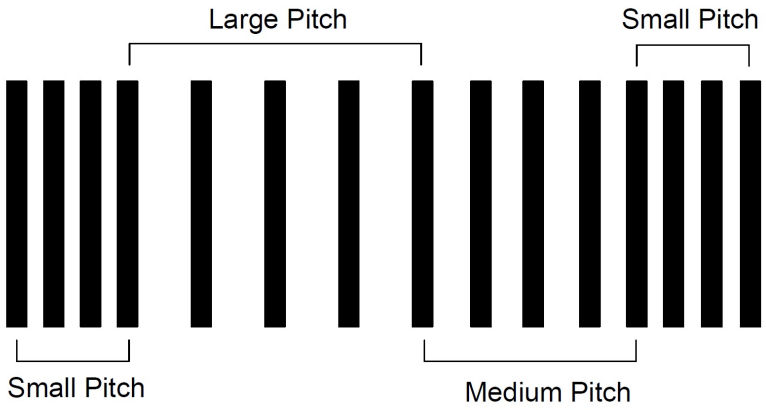


Figure 2.19: The OPC system works as a control system in which the line width on mask is changed iteratively to achieve the desired line width on wafer.

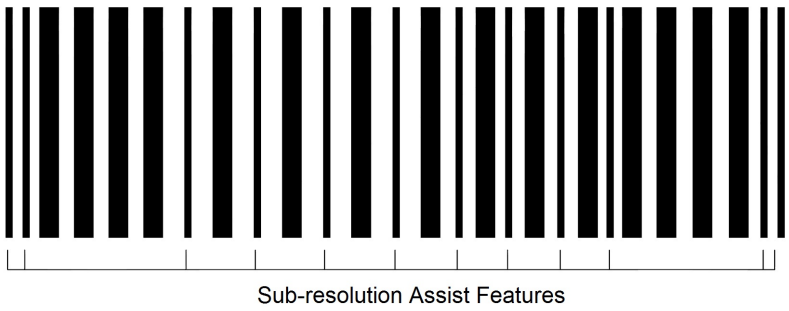
2.5.2 Sub-Resolution Assist Features (SRAF)

Sub-resolution Assist Features (SRAF), also called, Scattering bars (SBAR) are narrow lines or spaces placed adjacent to a primary feature in order to make a relatively isolated line (large pitch) or semi-isolated line (medium pitch) behave lithographically more like a dense line (small pitch) [22] as shown in Figure 2.21 . An SRAF, as the name implies, is a sub-resolution feature that is not meant to print. In fact, it must be carefully adjusted in size so that it never prints over the needed process window. This determines the most important trade-off in SRAF design: make the assist features as large as possible in order to create a more dense-like mask pattern, but not so large as to print. Generally, these assist features are centered on the same pitch for which the Off-Axis Illumination (OAI) was optimized (OAI is a topic that will be discussed extensively in section 2.5.4), though a more careful design will optimize their position and size to maximize the improvement in overlapping process window. As a result, the use of assist features allows the lithographer to design an off-axis illumination process optimized for dense patterns that can also be used to print more isolated features [4].

SRAF are designed to reduce the difference in the focus response of an isolated feature compared to a dense feature by making the isolated feature seem more dense. For illustration, the overlapping process window for an isolated line, when



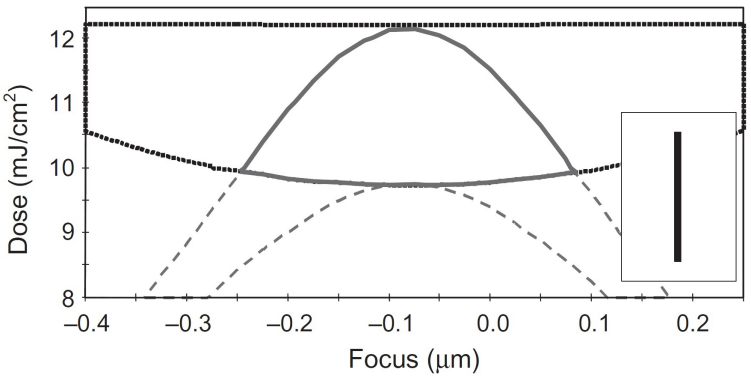
(a) Different pitch distribution with no SRAF



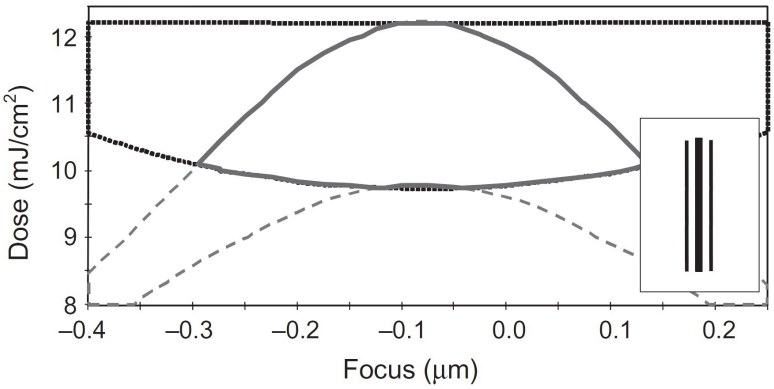
(b) Different pitch distribution with SRAF

Figure 2.20: SRAF are the extra lines. They do not print themselves but help the other features print with larger process latitude.

only bias OPC was used, are shown in Figure 2.21a. By inserting a single sided SRAF as shown in Figure 2.21b, the overlapping DOF increased from 300nm , when no SRAF was inserted, to 400nm. Further improvement can be obtained by using double scattering bars, where a second set of scattering bars is placed further away to create an effective five-bar pattern. Of course, this requires enough free space around the primary feature to actually be able to fit these extra assist features [7].



(a) Isolated line with no SRAF



(b) Isolated line with SRAF

Figure 2.21: SRAF are the extra lines. They do not print themselves but help the other features print with larger process latitude.

While the concept of using SRAF to improve the DOF of isolated features is a simple one, its practical implementation is anything but simple. Unlike the idealized case of an isolated line, real patterns contain lines with a variety of pitches (i.e. nearby patterns with different distances away), each of which must be outfitted

with an optimal assist feature or features, if one can fit [7]. While bias OPC can be used on the intermediate cases where the space between two lines is not large enough to accommodate an assist feature, these intermediate pitches do not benefit from the DOF advantages of SRAF (see Figure 2.22). And then, of course, there is the problem of what to do with line ends, corners, and other 2D patterns. Rule-based SRAF placement is quite common, but has difficulty with 2D placement. Model-based SRAF placement is difficult, but shows promise for complex 2D geometries [23]. These issues can be resolved, however, and sub-resolution assist features are commonly used in many chip designs. Polysilicon gate and contact levels, in particular, have seen benefits from using SRAFs. For contacts and other dark-field mask levels, the SRAF take the form of clear slots (spaces) rather than assist lines [24]. More discussion about SRAF in details is in chapter 4.

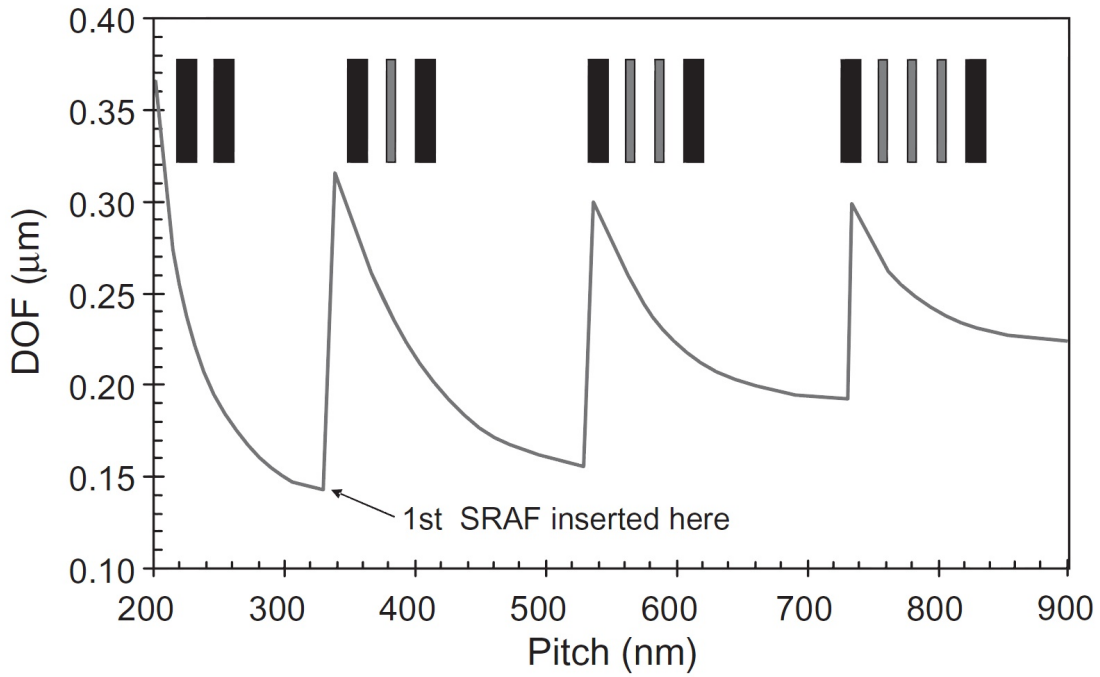


Figure 2.22: Schematic diagram of SRAF placement showing the discontinuous effect of adding an SRAF as the pitch grows (main feature size is 100 nm).
Source: *Fundamental Principle of Optical Lithography, By Chris Mack [7]*

2.5.3 Phase Shift Masks (PSMs)

Another method for addressing the resolution limits imposed by diffraction is phase shifting. While there are now many types of phase-shifting masks, they all employ the same basic concept, which is well illustrated by the original version introduced by Levenson, Viswanathan, and Simpson [25]. The idea behind the alternating phase-shifting mask is to modify the reticle so that alternating clear regions cause the light to be phase shifted 180 deg. This is accomplished by recessing the mask substrate by a small amount in the alternating clear regions as shown in Figure 2.23. With a suitably chosen depth, the light passing through the recessed region will have a 180-deg phase difference from the light that is transmitted through the regions that are not recessed. As a consequence, the light diffracted into the nominally dark area from the clear area to the left of the dark feature destructively interferes with the light diffracted from the right clear area. This improves image contrast relative to non-phase-shifted masks [8], as shown in Figure 2.24. All phase-shifting masks employ this same basic characteristic, where the destructive interference of light of opposite phases is used to improve image contrast. There are several versions of phase-shifting masks known in the research and industry , many of them are discussed in (Levinsion, 2011) [8].

An extremely attractive type of phase-shifting mask, from the perspective of mask fabrication, is the Attenuated Phase Shift Masking (AttPSM) [26]. In this type of mask, the non-clear areas are partially transmitting. With suitable processing, one can achieve up to 180^o phase difference between the clear and non-clear areas, sometimes with an etch of the quartz to an appropriate depth [8]. The partial transmission of the non-clear areas is a problem with this type of mask. For example, the threshold exposure dose for significant resist loss must be less than the amount of light that leaks through. An optimization of the normalized slope of the aerial image may have unacceptable levels of light in nominally dark areas of the mask (Figure 2.25). This places requirements on the resist and on the transmittance of the partially transmitting areas on the reticle. The attenuated

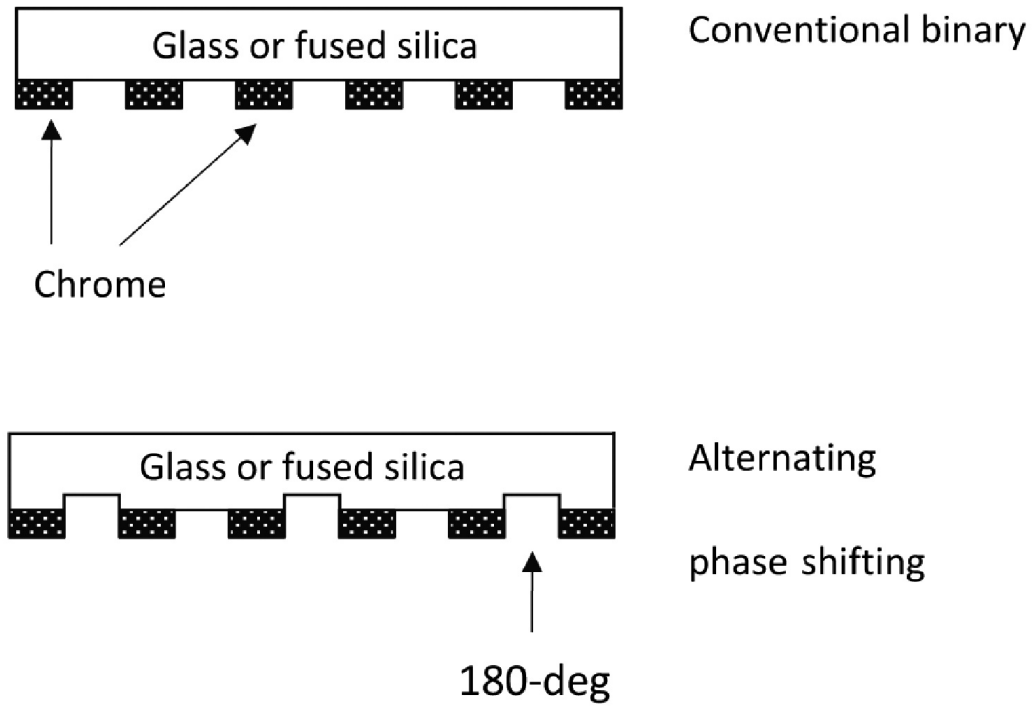


Figure 2.23: Conventional binary chrome-on-glass reticle and alternating phase-shifting mask.
Source: *Principles of Lithography, By Harry J. Levinson [8]*

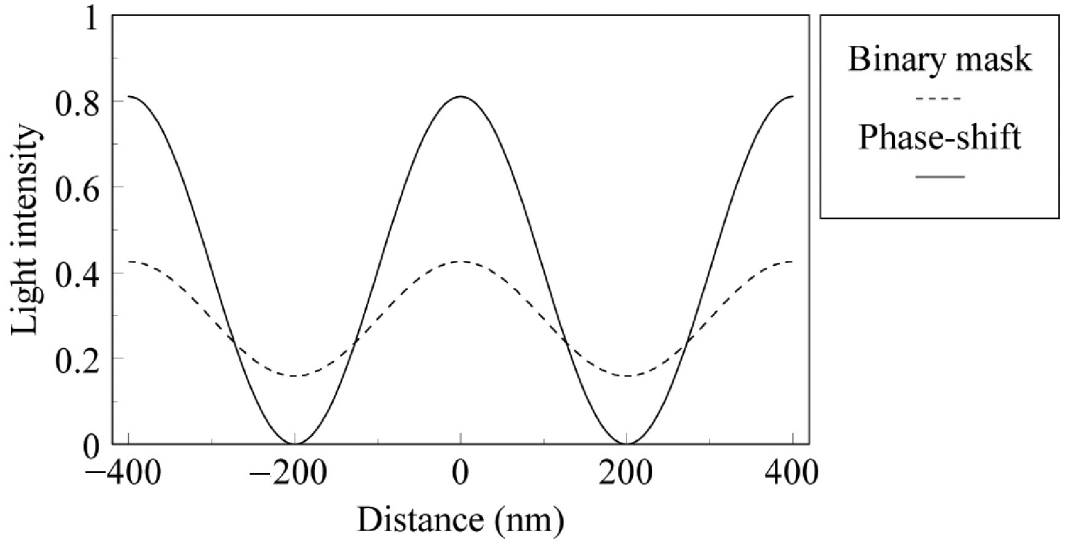


Figure 2.24: Simulated light-intensity distributions of a 400-nm pitch grating with equal lines and spaces, imaged with 0.5 NA optics at a wavelength of 248 nm. For a binary mask image and alternating phase-shifting image.
Source: *Principles of Lithography, By Harry J. Levinson [8]*

phase-shifting mask is attractive because it can be used in a single exposure step, and is relatively easy to fabricate. It is particularly useful for patterning contacts.

Attenuated Phase Shift Masking (AttPSM) lithography improves pattern fidelity by darkening the edges of shapes through destructive interference of light using a mildly translucent photomask. Now commonly called embedded attenuated phase masks, these attPSM use mask substrates that allow a small amount of light (6-10%) to penetrate the normally opaque regions of the mask. Through careful material optimization, the background light penetrates the mask exactly 180^o out-of-phase with the light penetrating the clear regions of the mask. As illustrated in Figure 2.26, this phase shifted background light improves feature contrast at the edges of the printed image. Forcing the electric field vector of the background light to be negative by shifting it 180^o relative to the foreground light causes a dark rim in the intensity profile. It is important to note that the self-consistency of the phase shifting effect in attPSM (i.e. no inter-shape phase interference), allows this technique to be applied to arbitrary layout configurations with no design restrictions [4].

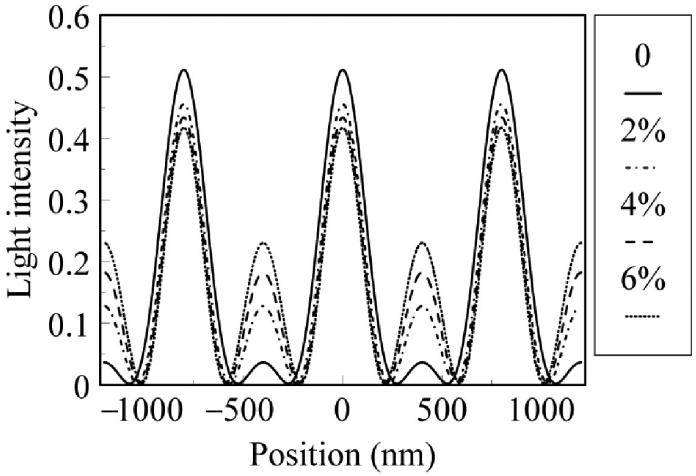


Figure 2.25: Light-intensity distributions from an attenuated phase-shifting mask, calculated with PROLITH2 for various levels of transmission through the leaky chrome.
Source: *Principles of Lithography, By Harry J. Levinson [8]*

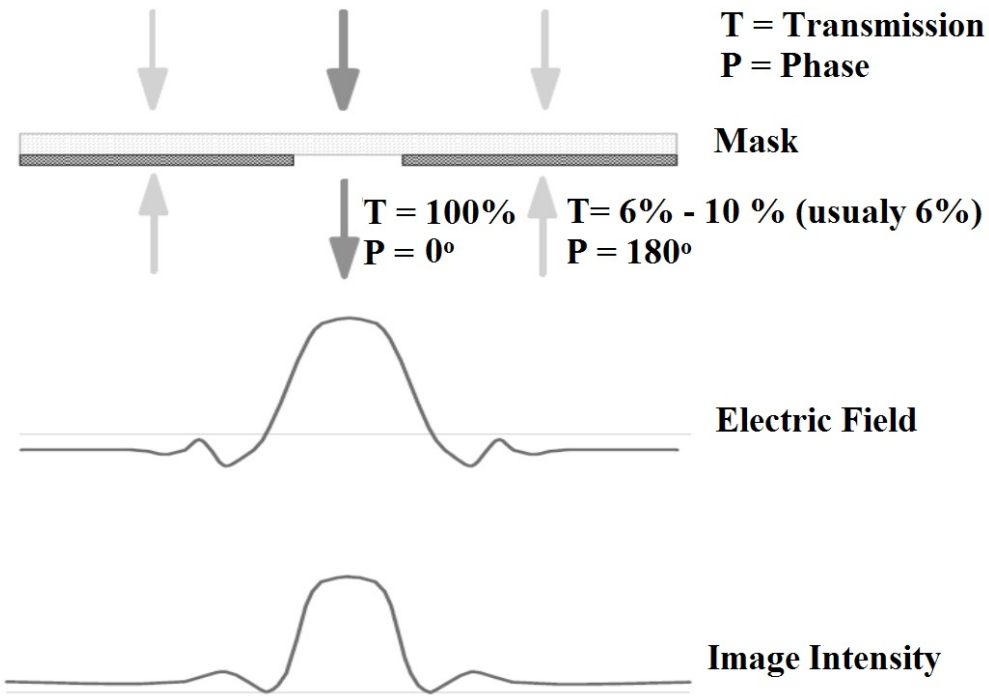


Figure 2.26: Principle of attenuated phase shifted mask (attPSM).

2.5.4 Off-Axis Illumination (OAI)

Off-Axis Illumination (OAI), refers to any illumination shape that significantly reduces or eliminates the on-axis component of the illumination, that is, the light striking the mask at near-normal incidence [27] [28]. By tilting the illumination away from normal incidence, the diffraction pattern of the mask is shifted within the objective lens. For the case of a repeating pattern, the diffraction pattern is made up of discrete diffraction orders. If the pitch of the repeating pattern is small, only a few diffraction orders can actually make it through the finite size lens. OAI will help in passing those higher diffraction orders through the lens, which leads to improved depth of focus (DOF) [7]. Thus, the main advantage of off-axis illumination is an increase in DOF (and thus the resolution) for small-pitch patterns as shown in Figure 2.27 .

OAI takes advantage of spatial frequency shifting of a given object to improve resolution and DOF. It can best be illustrated with a simple grating object. Being

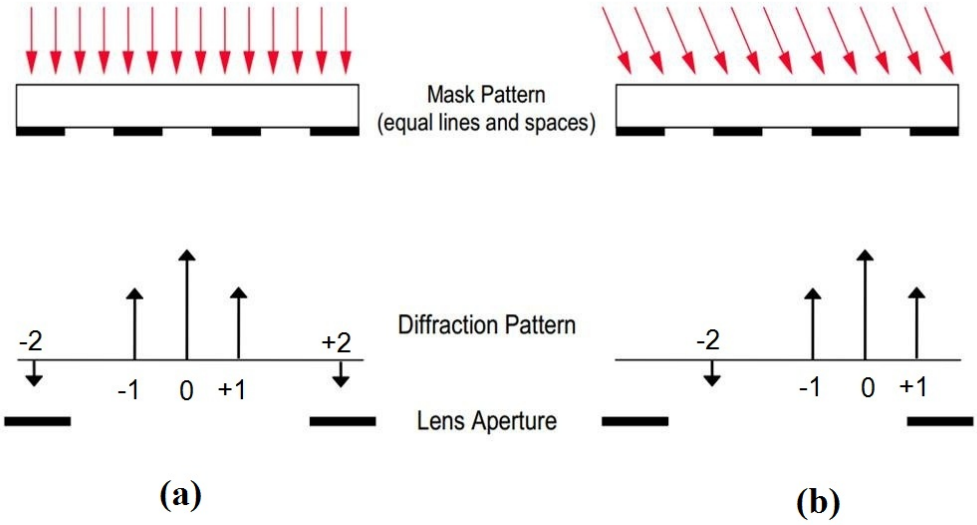


Figure 2.27: Tilt angle path more light (diffraction orders), Off-Axis Illumination (OAI) modifies the conventional imaging of a binary mask shown in (a) by tilting the illumination, causing a shift in the diffraction pattern as shown in (b). By positioning the shifted diffraction orders to be evenly spaced about the center of the lens, optimum depth of focus is obtained.

periodic, the grating contains discrete spatial frequency components, namely, the 0th order, ±1st order, ±2nd order, etc. When the minimum feature is of interest, only the 1st-order frequencies are preserved so that the resolution potential of the imaging lens can be fully utilized. This situation is shown in Figure 2.28(a), The spatial-frequency spectrum consists of the vertically oriented 0th-order beam and the ±1st-order beams, whose angle is a function of the periodicity of the grating. A smaller periodicity produces large spatial frequencies, thus larger diffraction angles in the ±1st-order beams. When the feature size is too small, i.e., the spatial frequency too high, the angle of the diffracted beams becomes larger than the acceptance angle of the imaging lens, and the ±1st-order beams are rejected. Only the 0th-order beam passes (no image).

Figure 2.28(b) shows the situation of a single collimated illumination beam obliquely incident on the mask, thus off axis. The three beams shown in Figure 2.28(a) are now tilted by the incident angle of the illumination. When the angle is adjusted to make the 0th-order, and one of the 1st-order beams symmetrical with

respect to the optical axis, the largest angular spread between the two beams is possible without being cut off by the acceptance angle of the lens; thus, the highest resolution is achieved. However, the other 1st-order beam is cut off, resulting in a lower exposing intensity. In Figure 2.28(c), two symmetrically opposed beams are used. When the angle of the illumination is optimized for a given periodic object, the 0th order of the left beam coincides with the 1st order of the right beam, and the 0th order of the right beam coincides with the 1st order of the left beam, as shown in the figure. The image consists of a single frequency component and is well reproduced.

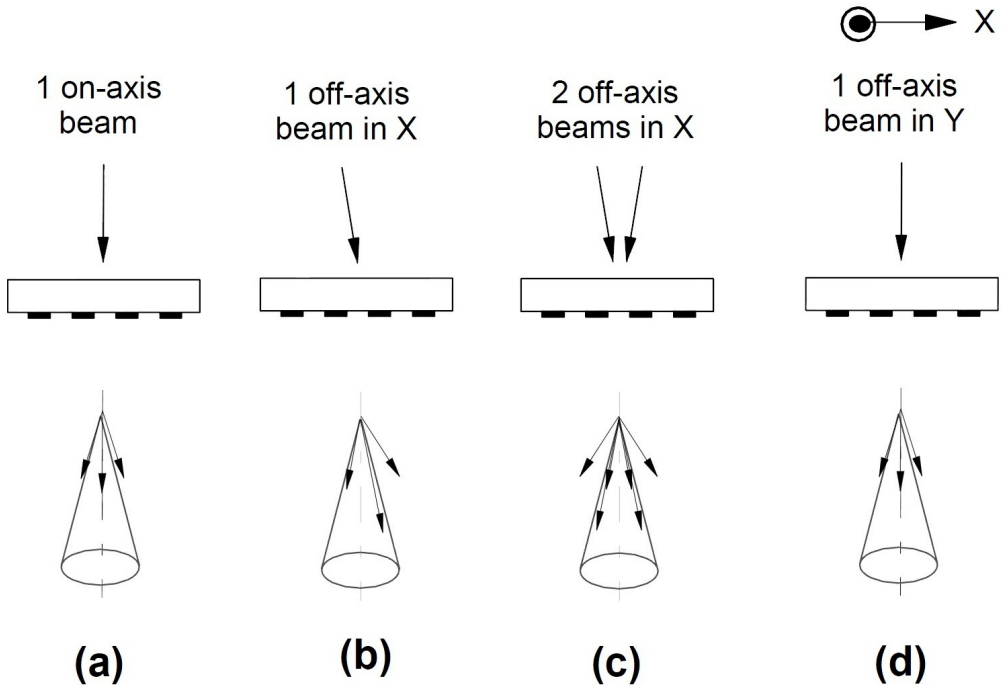


Figure 2.28: On-axis and off-axis illuminations affecting the 0th- and ±1st-order spatial frequency vectors.

Figure 2.28(d) shows that tilting the beam in x does not help to resolve the spatial frequencies in y. However, Most integrated circuit designs will contain many line and space-like features that are oriented both vertically and horizontally. If both vertical and horizontal lines are to be imaged together on the same mask, an illumination shape must be used that provides optimum tilts for both geometries. The simplest shape that provides this optimum tilt for both horizontal and vertical

line/space patterns is called quadrupole illumination (shown in Figure 2.29).

While the quadrupole shape provides optimal performance for vertical and horizontal lines, other orientations (such as a line/space array oriented at 45) will not be optimum. For any orientation of lines, the optimal dipole for that pattern will be spread in a direction perpendicular to the line orientation, and can be shifted parallel to the lines in any amount that keeps the dipoles within the lens. If the mask will contain arbitrary orientations of lines, many rotations of the dipoles will produce an annulus of illumination (and thus is called annular illumination). The optimum center of the annular ring is the same as the optimum dipole position. An example of different source shapes, an annular (outer ring), dipole (two openings), or quadrupole (four openings) are shown in Figure 2.29.

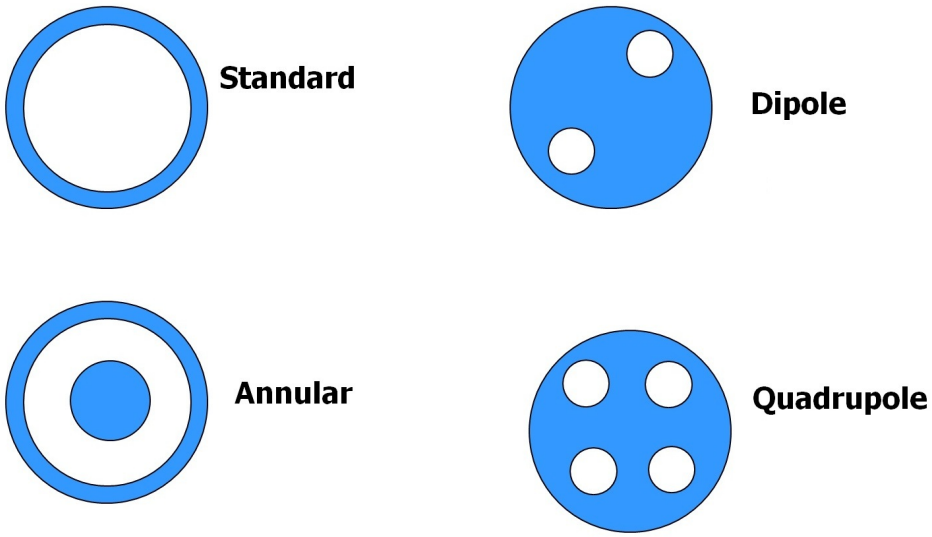


Figure 2.29: OAI Different Source Example

2.6 Summary

An introduction about typical sequence of lithographic processing step in the 45nm and beyond is discussed in brief. The basic of imaging theory including the behavior of an optical imaging system was explained. The Fraunhofer diffraction integral which describes the diffraction effect coming from the mask was explained.

The Fourier optics of light and how it affects the minimum dimension on wafer is discussed comprehensively. The resolution equation which describes the theoretical resolution limit of an imaging system was derived. Lithography metrics used to quantify image quality and ensure a robust feasible solution is then briefly reviewed. The chapter ends with a description of the different types of Resolution Enhancements Techniques (RET) known in the industry including Optical Proximity Correction (OPC), Sub-Resolution Assist Features (SRAF), Phase Shift Mask (PSM) and Off-Axis Illumination (OAI). Further discussion about OPC and SRAF in details is in chapter 3 and chapter 4, respectively.

Chapter 3

Dynamic Feedback Controller for Optical Proximity Correction

3.1 Introduction

A dynamic feedback controller for Optical Proximity Correction (OPC) in a random logic layout using ArF immersion Lithography is presented. The OPC convergence, characterized by edge placement error (EPE), is subjected to optimization using optical and resist effects described by calibrated models (Calibre® nmOPC simulation platform). By memorizing the EPE and Displacement of each fragment from the preceding OPC iteration, a dynamic feedback controller scheme is implemented to achieve OPC convergence in fewer iterations. The OPC feedback factor is calculated for each individual fragment taking care of the cross-MEEF (mask error enhancement factor) effects. Due to the very limited additional computational effort and memory consumption, the dynamic feedback controller reduces the overall run time of the OPC compared to a conventional constant feedback factor scheme. In this work, the dynamic feedback factor algorithm and its implementation, as well as testing results for a random logic layout, are compared and discussed with respect to OPC convergence and performance [2].

Semiconductor manufacturing is continuously ramping up the yield of tech-

nology processes with transistor dimensions well below the exposure wave length. Pushing the limits of the exposure wave length to resolve patterns of smaller dimension introduces light diffraction effects during the lithography stage. Light diffraction prevents printing wafer patterns identical to the shapes drawn on the exposure mask. Optical Proximity Correction (OPC) plays a major role enabling these technologies to be realized. By changing the mask shapes to account for light diffractions, the final pattern on the wafer matches the desired target pattern. OPC achieves this by breaking the layout edges into smaller fragments and using models that simulate the exposure process to calculate the differences between printed shapes and desired shapes. These differences are referred to as Edge Placement Errors (EPE). OPC minimizes the EPE for all fragments in an iterative process. In a given iteration the movement value for each fragment is usually the EPE multiplied by a constant (feedback factor). Convergence of the OPC is achieved if all EPE become zero.

Traditional OPC uses a constant feedback factor [29]. This approach was successful at earlier technology nodes where the EPE of a given fragment was primarily governed by its own displacement, not so much by the movement of other neighboring fragments (an effect described by the cross-Mask Error Enhancement Factor or cross-MEEF). However, OPC convergence is substantially more difficult to achieve in advanced technology nodes like 28nm and below. The influence of many neighboring fragments increases substantially because the printed features are only fractions of the exposure wavelength. A high cross-MEEF is problematic for OPC convergence if it is not considered in the fragment movement equation. Consequently, an increased number of OPC iterations are needed to reach OPC convergence translating into longer OPC runtime. In some locations OPC convergence may not be achieved, limiting the OPC accuracy which may reduce the process window or cause the formation of hotshots. In this work, a dynamic feedback controller is introduced which uses a customized feedback factor for each fragment in every interaction. This approach accelerates OPC convergence and reduces the range of remaining EPE. It has been specifically developed and tested in contact

layer-like applications. The benefit of the new algorithm increases with decreasing target size (technology node) and increasing complexity of the illuminator (conventional, annular, c-quad, dipole, customized). Mentor Graphics nmOPC platform technology, in conjunction with its Lithography Application Interface (LAPI), is used in the implementation of the dynamic feedback algorithm. The results are discussed in terms of OPC convergence (EPE histogram) and runtime of the OPC and compared to traditional OPC using constant feedback factors.

3.2 Constant Feedback OPC

Traditional OPC using constant feedback is common in technology nodes of 65nm and above. OPC convergence is achieved while maintaining a reasonable runtime. In advanced technology nodes beyond 65nm, the specifications of OPC convergence are tightened due to a shrinking common process window. Traditional OPC runs longer since more iterations are required. To combat the increasing OPC runtime, a classification of fragments based on layout geometry assigns different feedback factors dependent on the fragment type, such as line end or space end, in every iteration. These feedback values are stored and displayed in a table format. An example is given in Table 3.1.

The table based feedback approach improved OPC convergence compared to the traditional, constant feedback OPC. Although easily tuneable, complexity of OPC recipes increased and the quality of the OPC became increasingly dependent on the sophistication of the layout classification into fragment types, associated bins and their underlaying rules. Validation of the feedback table required exhausting pattern generation (and test OPC runs) while still leaving a risk of missing the most critical pattern in full chip layout. Optimization of a feedback table using a simulation annealing method are described in (Desouky, 2010)[30].

As an example, two different fragment types, nested contacts at minimum pitch and an isolated contact are depicted in Figure 3.1 to explain the optimization of

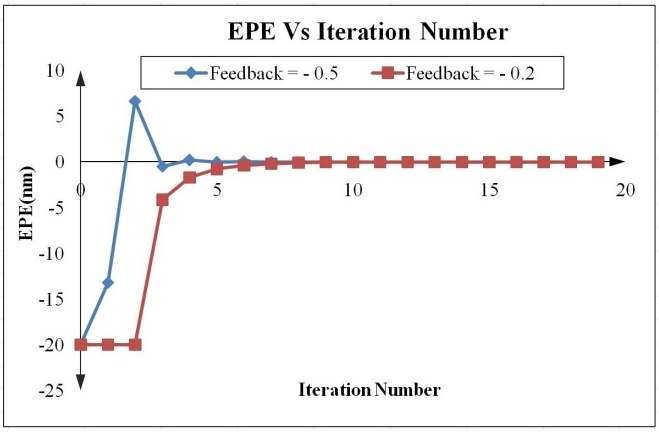
Table 3.1: OPC Feedback versus iteration for various fragment types. Each fragment type is split into different bins based on a set of geometric rules.

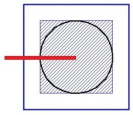
Bin	**Rule**			**Feedback**			
	Length	**Space**	**Frag Type**	**Iter1**	**Iter2**	**Iter3**	**Iter4→end**
cv_cat1	≤ 0.1	$\leq$0.04	Concave	0.1	0.4	0.2	0.25
cv_cat2	> 0.1	>0.04	Concave	0.3	0.25	0.1	0.1
le_cat1	≤ 0.08	$\leq$0.06	Line End	0.2	0.5	0.1	0.4
le_cat2	> 0.08	>0.06	Line End	0.3	0.25	0.3	0.5
cx_cat1	≤ 0.12	$\leq$0.05	Convex	0.1	0.4	0.2	0.2
cx_cat2	> 0.12	>0.05	Convex	0.3	0.25	0.3	0.5

their feedback factor per OPC iteration by plotting their EPE versus the iteration number for different feedback settings. An optimized feedback of -0.5 for the isolated contact is inappropriate for the nested contact at minimum pitch because a much larger MEEF does not allow the OPC to converge. For the nested contact, a more conservative feedback closer to zero is required. This humble example constitutes the need for different feedback factors in different layout locations. Instead, setting a global conservative feedback factor close to zero will require a very large number of OPC iterations to achieve OPC convergence. This certainly increases OPC runtime beyond the acceptable limit. The process of studying convergence and feedback values in a full chip layout is an exhausting task of OPC runtime optimization. An automatic feedback optimization approach is clearly favorable.

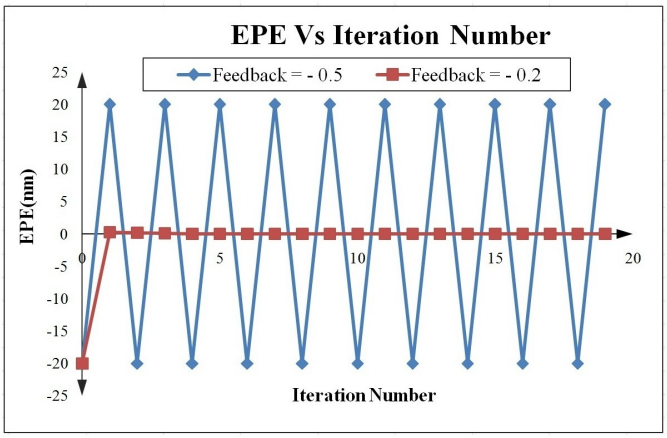
3.3 Dynamic Feedback OPC

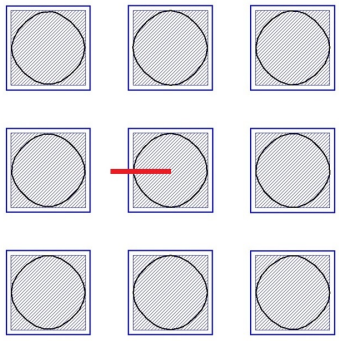
The dynamic feedback method proposed in this work calculates the feedback value for each fragment based on the relationship between the sensitivity of the image formed on the wafer and the change in the fragment position. Since the fragment movement is proportional to the product of feedback and EPE, the resulting fragment movement value will allow OPC to better control the image that is being





(a) Isolated Contact





(b) Nested Contacts

Figure 3.1: OPC Iteration Number versus Edge Placement Error (EPE) for isolated and nested contacts using constant feedback values. A feedback of -0.5 is suitable for an isolated contact, but inappropriate for nested contacts at minimum pitch. Nested Contacts require a feedback of -0.2.

formed on wafer.

$$MEEF = \frac{\Delta CD_{wafer}}{\Delta CD_{mask}} \tag{3.1}$$

The Mask Error Enhancement Factor[6] (MEEF) is the ratio between the Critical Dimension (CD) change on wafer, ΔCD_{wafer}, to the CD change on mask (represented on 1x scale), ΔCD_{mask}, as shown in Equation 3.1. Deriving the feedback factor from the MEEF value may provide the OPC with the required control over the fragments movement to improve OPC convergence [31]. MEEF for a given structure is not a fixed value but changes with the OPC iterations due to proximity change in the surrounding environment. According to the MEEF definition, the change in mask CD should be a global constant (uniform sizing) which is applied to all the features on the mask, regardless if OPC is applied to them or not.

While an accurate determination of MEEF for each fragment in each iteration would require additional computational effort which would increase runtime, the OPC iterative algorithm itself provides mask pattern changes when progressing from iteration to iteration. Contrary to the definition of MEEF, these layout changes are *not* uniform. In general, every fragment moves differently - sometimes in opposing directions - and some mask patterns, like scatter bars, may not move at all.

$$EPE\ Sensitivity = \frac{\Delta EPE}{\Delta Displacement} \tag{3.2}$$

The dynamic feedback algorithm uses an "EPE sensitivity" which is defined as the ratio between EPE difference, ΔEPE, and the difference in fragment displacement, $\Delta Displacement$, as shown in Equation 3.2. Mathematically similar to MEEF, the EPE Sensitivity does not require a uniform change of the mask, but allows independent movement of the fragments. It therefore spans a much wider range compared to MEEF, including negative EPE sensitivity, because the effects of the movements of neighboring layout may over-compensate the effect of the movement of the fragment under consideration. Like MEEF, EPE sensitivity changes

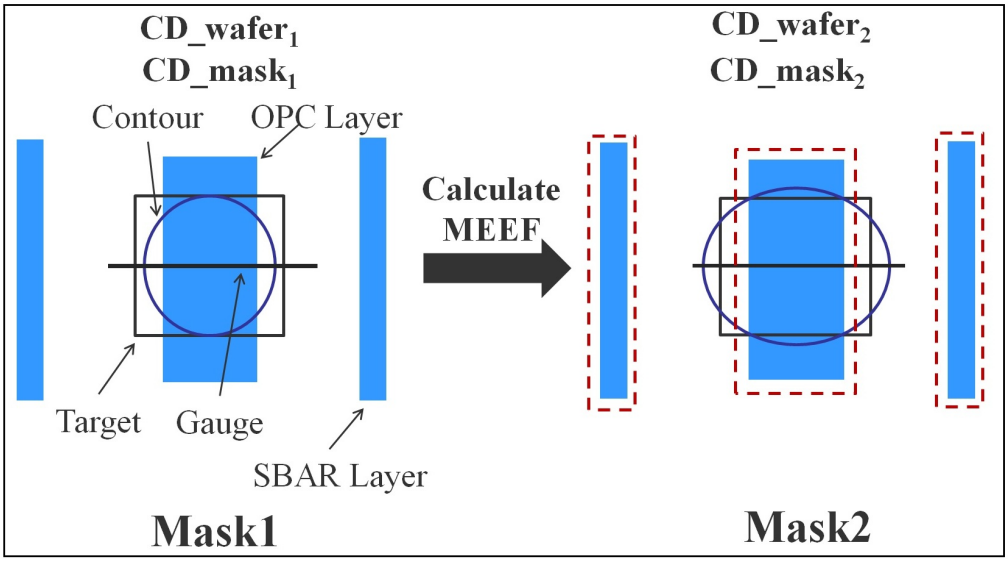
during the OPC iterations. Figure 3.2 illustrates the difference between MEEF and EPE Sensitivity

$$Sensitivity_i = \frac{epe_i - epe_{i-1}}{disp_i - disp_{i-1}} \tag{3.3}$$

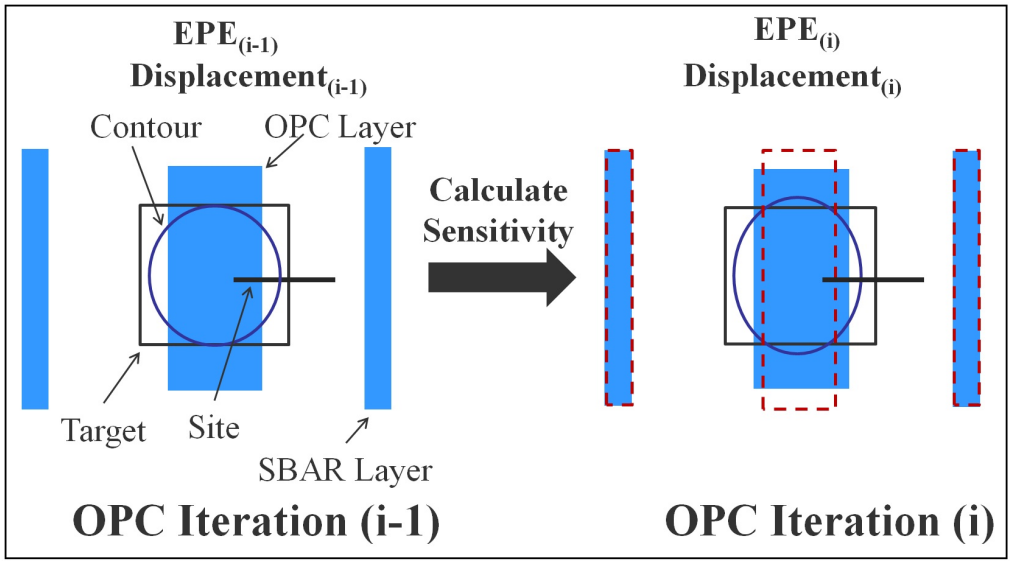
During model based OPC, determination of the EPE sensitivity for each fragment in each iteration does not require additional optical simulation effort, but demands memorization of the displacements and EPE values of the previous iteration. For a given single fragment in the i-th iteration, Equation 3.3 approximates the difference in EPE as the difference of EPE in the current iteration with respect to the previous iteration. Similarly, the difference in fragment displacement is defined as the displacement difference between the current iteration and the previous iteration. Figure 3.3 explains how the feedback is calculated in the dynamic feedback algorithm as compared to the constant feedback method.

$$Feedback = \frac{-1}{Sensitivity} \tag{3.4}$$

Equation 3.4 constitutes a "poor engineer's approach" for a dynamic OPC controller. Figure 3.4a plots this relation and explains its limitations. For negative EPE sensitivity the feedback would become positive which may drive the fragment away from convergence. The EPE sensitivity may easily become zero or very close to zero. In this case, Equation 3.4 diverges, leading to unreasonably large positive or negative displacements which will cause OPC "overshooting" and convergence problems. Finally, in case the EPE sensitivity is positive and very large, the feedback factor becomes almost zero which may cause the OPC to "freeze", preventing necessary changes in displacement in subsequent OPC iterations while not yet converged.

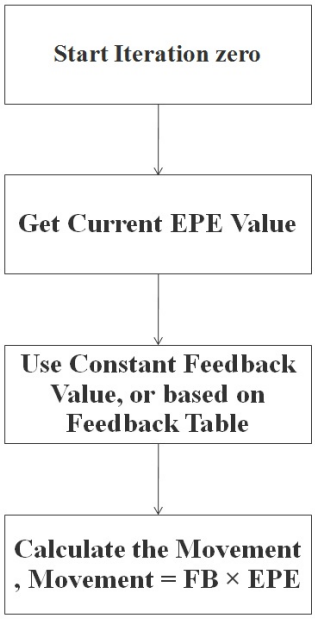


(a) MEEF Calculation Method

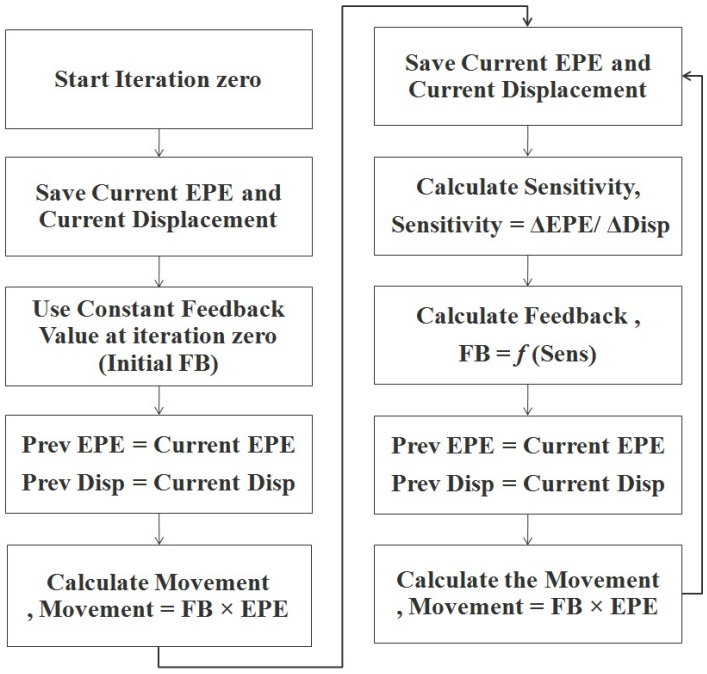


(b) Sensitivity Calculation Method

Figure 3.2: Difference between MEEF and EPE Sensitivity. By its definition MEEF demands a global uniform sizing of all mask features. EPE Sensitivity requires memorization of the EPE and displacement from the preceding OPC iteration. EPE Sensitivity may become zero or even negative due to individual movements of the surrounding fragments.



(a) Constant Feedback OPC Flow



(b) Dynamic OPC Feedback Controller Flow

Figure 3.3: Dynamic OPC feedback controller flow versus traditional, constant feedback algorithm. In the dynamic OPC feedback flow the feedback value is calculated as a function of EPE sensitivity. In the traditional, constant feedback algorithm the feedback value for each fragment is fixed and predefined.

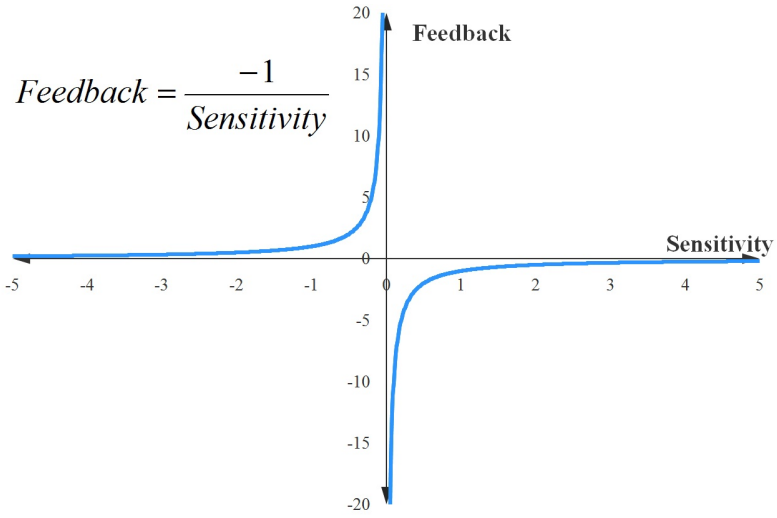
$$Feeback = \begin{cases} ScaleFB \times SafeFB & , Sens \leq 0 \\ ScaleFB \times SafeFB(1 - (1 + \frac{(1-SmallFB) \times Sens}{SafeFB})) & , 0 < Sens \leq 1 \\ ScaleFB \times \left(SmallFB - \frac{1}{Sens}\right) & , 1 < Sens \end{cases} \tag{3.5}$$

As an alternative, Equation 3.5 presents a modified relationship which is plotted in Figure 3.4b. To avoid the shortcoming of the "poor engineer's approach", a constant negative feedback, SafeFB, is defined for negative EPE sensitivities; and the OPC "freeze" is avoided by definition of SmallFB which governs the regime of very large positive EPE sensitivity. The singularity of the "poor engineer's approach" is replaced by a linear dependence. The majority of fragments will have EPE sensitivities close to 1. The new dynamic feedback OPC controller needs three parameters to tune: SmallFB, SafeFB and ScaleFB. Their tuning is subject to an optimization of OPC accuracy and runtime.

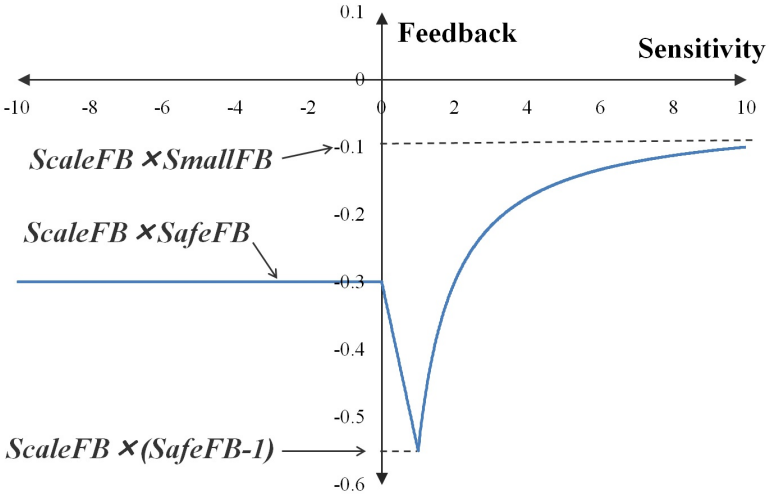
3.4 Results And Discussion

For a nested contact, the EPE, the displacement, the EPE sensitivity and the feedback factor of a single fragment in every OPC iteration are displayed in Figure 3.5b. For comparison, Figure 3.5a represents similar information for an isolated contact. The parameters of the dynamic feedback controller algorithm introduced in Figure 3.4b are chosen after completion of tests in small layout and test patterns: SafeFB = -0.4, ScaleFB = 1, SmallFB= -0.2 and InitialFB = -0.2.

For the nested contact pattern, Figure 3.5b shows the evolution of the OPC. Starting from the "initial feedback factor" at -0.2 in the zero iteration (which must be pre-defined since there is no previous iteration yet). There is no EPE sensitivity defined in the zero OPC iteration. After completion of the first OPC iteration the fragment receives a displacement of +4nm and accordingly the EPE drops down from -20nm at the zero iteration to +0.3nm at first OPC iteration. Because of the



(a) Simple Feedback Controller



(b) Bounded Continuous Feedback Controller

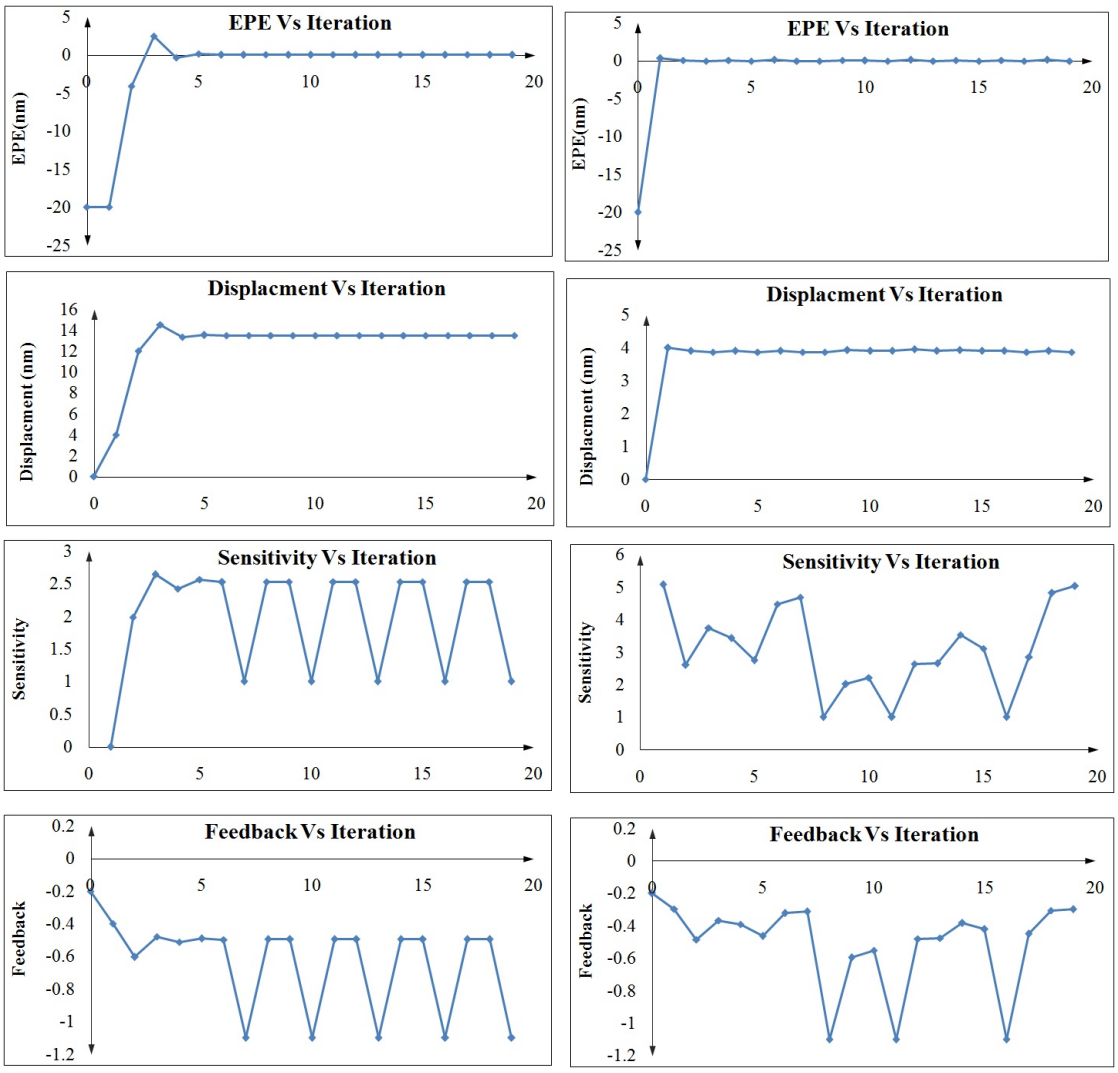
Figure 3.4: Feedback versus EPE sensitivity for a bounded, dynamic OPC feedback controller.

very large EPE difference (20.3nm) when compared to a relatively small difference in displacement (4nm), the EPE sensitivity calculated at the first iteration is large and approximately equal to 5. Consequently, the feedback factor moves closer to zero in the first iteration (-0.25). In the second OPC iteration the EPE reaches 0.044nm and in subsequent OPC iterations the changes in EPE and fragment displacement stay very small and within specification. OPC convergence is achieved very quickly. Although EPE and displacement stay small, the EPE sensitivity may reach larger values (largely positive or negative) and may even change from iteration to iteration without hurting the convergence of the OPC. The controller handles large changes of the EPE sensitivity by limiting the feedback factors within an interval of [0 to -1.1]. The lower bound of the interval, -1.1, is derived from the product of ScaleFB and (SmallFB - 1). For this reason the large changes in the EPE sensitivity do not significantly affect the OPC convergence after the fourth OPC iteration.

Table 3.2: OPC convergence: dynamic feedback controller compared to a constant feedback approach for nested and isolated contacts

Used Feedback Controller	**How Many OPC Iteration Needed to Converge**	
	Nested Contacts	**Isolated Contact**
Feedback = -0.2	3 iterations	8 Iterations
Feedback = -0.5	Can't Converge	5 Iterations
Dynamic Feedback	2 iterations	4 iterations

Figure 3.5a illustrates the evolution of the OPC of an isolated contact pattern. Starting from the "initial feedback" at -0.2 in the zero iteration, the fragment receives a displacement of 4nm after first iteration. This leaves the EPE unchanged at -20nm because the ±20nm is the limit of EPE range allowed during OPC correction. As a result, the EPE difference between first and zero iteration is zero and the EPE sensitivity also becomes zero in the first iteration. Accordingly the feedback factor increases up to -0.4 (the safe feedback value). In the second iteration the fragment receives a larger displacement of 12nm, the EPE drops down to -4nm and the EPE sensitivity becomes equal to 2.0. The feedback factor increases to -0.6 which causes the EPE sensitivity to rise further in the third OPC iteration



(a) Isolated contact (b) Nested Contact

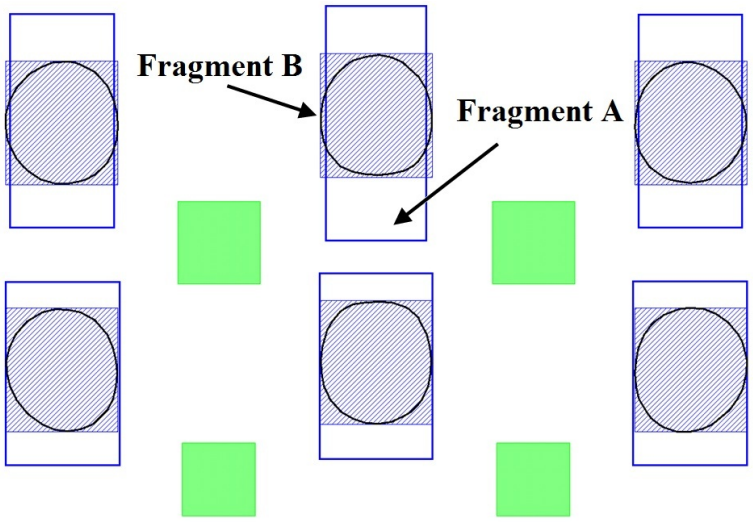
Figure 3.5: OPC results for nested and isolated contacts using the dynamic feedback controller. EPE, feedback factor and EPE sensitivity versus OPC iteration. The dynamic feedback controller achieves OPC convergence in fewer iterations compared to an optimized feedback scheme using a constant feedback shown in Figure 3.1.

where the EPE sensitivity increases to 2.5 and feedback factor drops to -0.47. OPC convergence is achieved in less than 5 OPC iterations. In the case of an isolated contact pattern the EPE changes in the later OPC iterations become very small and the corresponding EPE sensitivities vary between +1 and +2.5 (and related changes in feedback values between -1.1 and -0.5) without any negative impact to the EPE histogram showing the accuracy of the OPC.

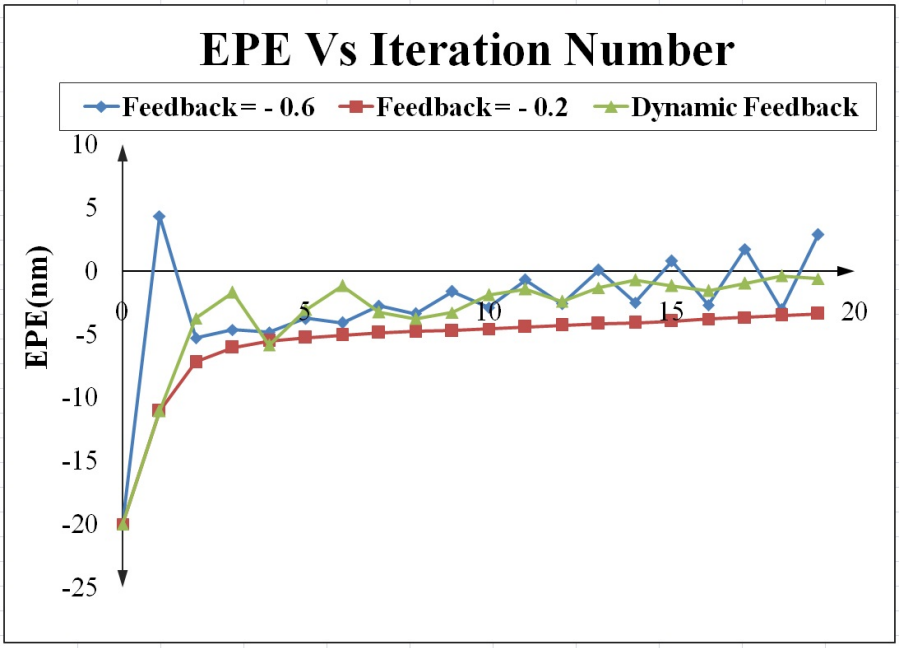
Figure 3.5 compares results using the dynamic EPE controller to the results using a constant feedback controller as shown in Figure 3.1. Table 3.2 summarizes the results of the comparison. Two constant feedback values are used to test a constant feedback scheme (feedback = -0.2 and -0.5). For the isolated contact, the OPC convergence is achieved in 4 iterations using the dynamic controller compared to 8 and 5 iterations in case of constant feedback of -0.2 and -0.5 . For the nested pattern, the OPC convergence is achieved in 2 iterations compared to 3 iterations and no convergence (due to oscillation) in the case of constant feedback of -0.2 and -0.5. The dynamic feedback controller could achieve the OPC convergence in fewer OPC iterations compared to a constant feedback scheme for nested contacts as well as isolated contact.

The dynamic feedback controller offers an additional advantage: there is no need for any optimization of feedback factors for each pattern type, and the time consuming creation and validation of tables comprising feedback factors becomes obsolete. In any OPC iteration and for every given fragment, the dynamic feedback algorithm converges the OPC properly and automatically, regardless of pattern type, fragment type, length or proximity.

Figure 3.6 introduces a pattern in which OPC convergence is more difficult to achieve. During the evolution of the OPC, neighboring fragments A and B shown in Figure 3.6a are forced to move very differently. At the zero iteration, fragment A has a negative EPE value and Fragment B has a positive EPE value. Fragment A needs to move outward (positive displacement) while fragment B needs to move inward (negative displacement). When Fragment A moves outward this affects



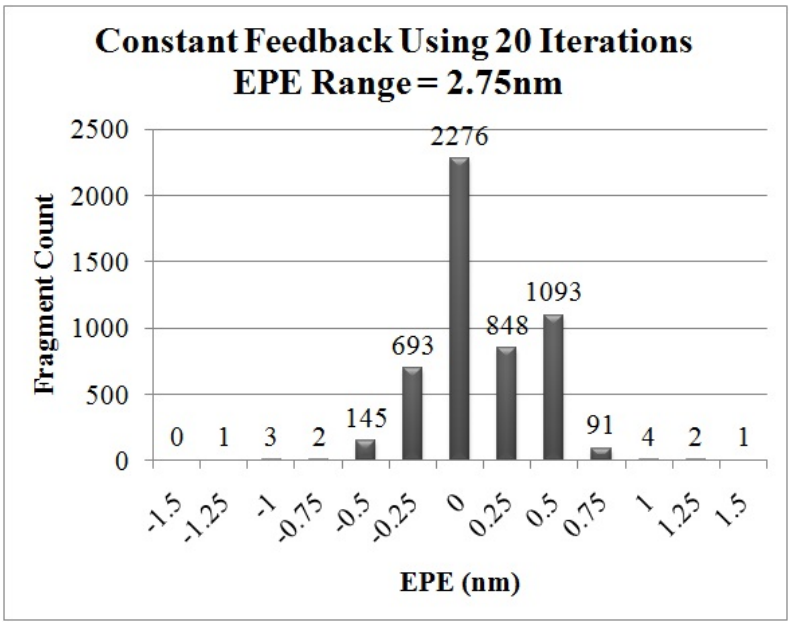
(a) Challenge Pattern



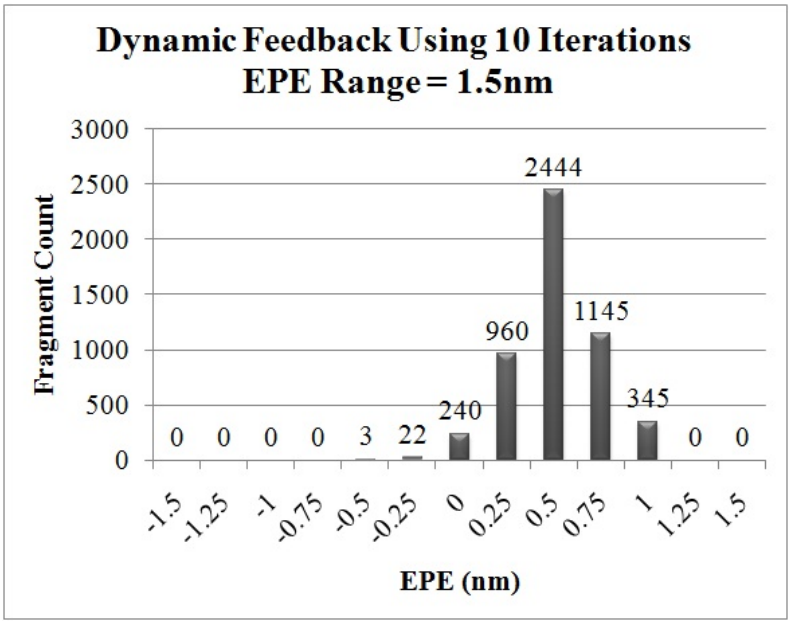
(b) EPE Vs. Iterations for different feedback scheme

Figure 3.6: Evolution of the EPE of fragment A along progressing OPC iterations. Comparing three different feedback algorithms: constant feedback factor of -0.2 , constant feedback factor of -0.6 and the dynamic feedback controller. The dynamic feedback controller proves superior in terms of OPC accuracy since it achieves the smallest remaining EPE.

the EPE at fragment B causing its EPE to become more positive. Likewise, the inward movement of fragment B causes the EPE of fragment A to become more negative driving it even further outward. During the course of OPC iterations, fragment A receives a very large positive displacement while fragment B adopts a very large negative displacement. Such a process and the resulting rectangular OPC shape with a large aspect ratio (though the target pattern is a square contact) constitutes a challenge for the OPC convergence, since a very large number of OPC iterations may be needed in a constant feedback approach to converge such a pattern for which three different OPC feedback algorithms are compared: a constant feedback factor of -0.2, a constant feedback factor of -0.6 and the dynamic feedback controller using the same parameters as described above. Figure 3.6b depicts the evolution of the EPE as the OPC iterations progress. The relatively large fixed feedback factor of -0.2 (closer to zero) avoids any OPC oscillation, but the OPC convergence is very slow, especially at the later stage of the OPC closer to the final iterations. The feedback factor of -0.2 achieves OPC convergence but requires a lot more OPC iterations increasing OPC runtime. The EPE at the 20th OPC iteration reads -3.363nm whereas the use of a fixed feedback factor of -0.6 seemingly achieves the OPC convergence at the 13th OPC interaction. However, due to the simultaneous movements of the fragment A and B affecting each other's EPE, the EPE increases again in the latter stage of the OPC. After the 13th OPC iteration the EPE continues growing larger and oscillates around zero, finally ending the OPC cycle with a remaining EPE of +2.902nm at the 20th OPC iteration. Instead, the dynamic feedback controller decreases the EPE of fragments A and B gradually and continuously from iteration to iteration. The OPC is steadily converging with no oscillation around zero EPE. In the 6th iteration applying the dynamic feedback controller the EPE reads -1.151nm, but due to the effect of fragment B the EPE increases again in subsequent iterations. Unlike using the constant feedback of -0.6, the dynamic feedback reaches final EPE of -0.595nm at the last OPC iteration. The dynamic OPC controller provides a more accurate OPC solution compared to the constant feedback controller.



(a) Constant Feedback

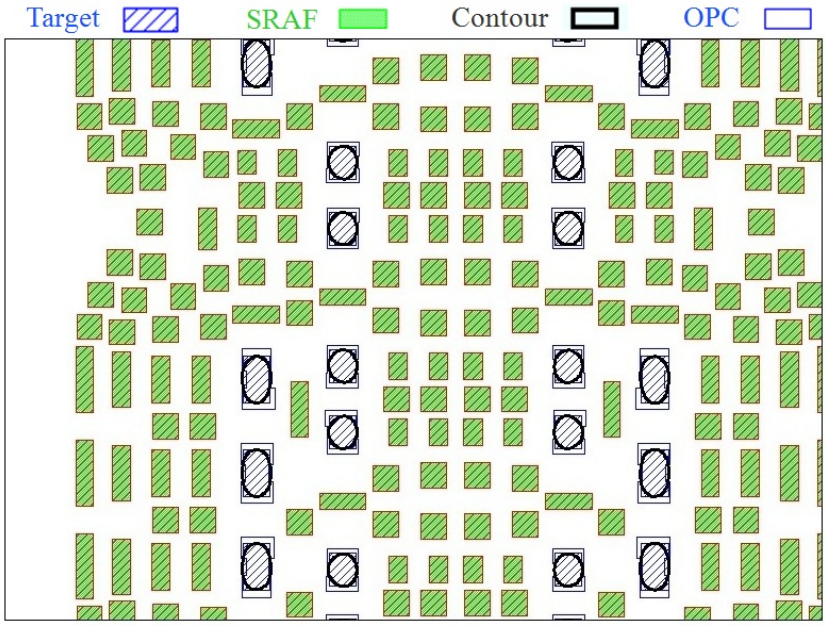


(b) Dynamic Feedback

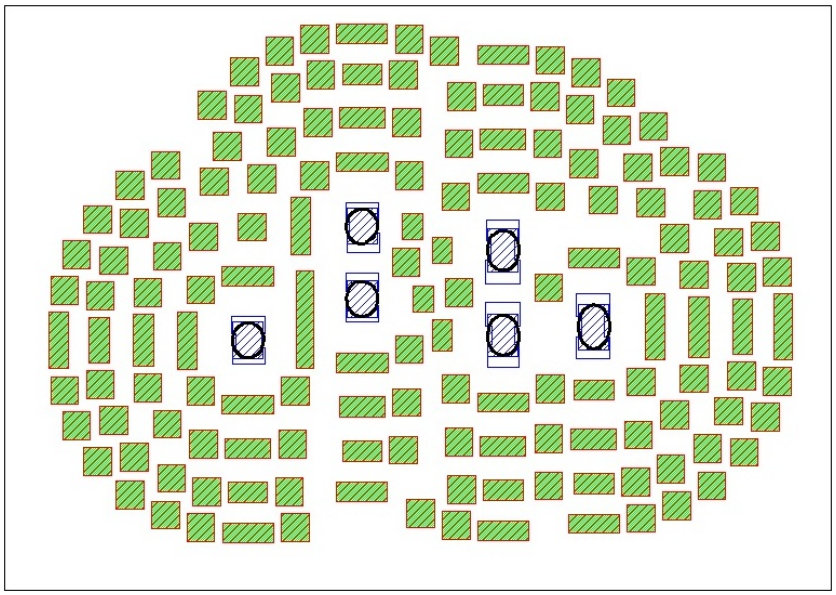
Figure 3.7: EPE histogram for a medium size layout ($30\mu m \times 20\mu m$). Comparing a constant feedback controller and the dynamic feedback algorithm. The dynamic feedback algorithm using 10 iterations achieves a better OPC accuracy characterized by an EPE range of 1.5nm, compared to a constant feedback controller characterized by an EPE range of 2.75nm using double the number of OPC iterations (20 iterations). The dynamic feedback controller causes a 50% run time reduction and leads to improved OPC accuracy (smaller remaining EPE range).

A larger test case was required to prove statistically that the dynamic feedback controller provides a more accurate OPC result. For this test, we used a medium size design ($30\mu m \times 20\mu m$) of a random logic interconnect layer (square contact only). All the patterns described above were part of this larger layout. The table based feedback OPC algorithm and the dynamic feedback OPC algorithm were compared in terms of OPC accuracy (remaining EPE histogram) and runtime. The OPC convergence characterized by an EPE histogram for both algorithms are shown in Figure 3.7. The dynamic feedback algorithm (Figure 3.7b) displays a narrower EPE distribution characterized by an EPE range of 1.5nm with a smaller number of "EPE outliers" at the far end of both sides of the distribution. On the other hand, the constant feedback algorithm displays a much wider distribution of remaining EPEs characterized by an EPE range of 2.75nm as shown in Figure 3.7b. This result is especially remarkable since the constant feedback approach used double the number of iterations compared to the dynamic feedback controller (20 iterations for constant feedback compared to 10 iterations for the dynamic feedback controller). This is approximately equivalent to a 50% run time reduction with an improved OPC accuracy. It is fair to notice the EPE histogram for the dynamic feedback controller appears to be shifted towards positive EPE according to an average EPE of +0.5nm, while the table based feedback controller does not show a shift (average EPE of 0nm). This phenomena requires further investigation. A step size of 0.25nm has been used during OPC correction. (A smaller step size is likely to improve these results even further.)

As an example Figure 4.13 shows two patterns in the medium size layout used for generation of the results described in Figure 3.7. This interconnect layer is comprised of contacts in varying proximities. It includes square and rectangles of different aspect ratio. The SBAR layer is inserted using Mentor Graphics Calibre® nmSRAF software. The SBAR insertion is guided by the results of Calibre® model based SBAR insertion (pixel-based, inverse Lithography engine, ILT, described in (Chou, 2008)[32].)



(a) Layout Clip 1



(b) Layout Clip 2

Figure 3.8: Two snapshots taken from the medium size design: Different random pattern for interconnect layer, square and rectangles with different aspect ratio. The SBAR layer is also shown.

Several works have been done before to speed up OPC convergence based on MEEF. A method using global OPC convergence by MEEF-based correction combined with proportion-integral-derivative (PID) controller was introduced in (Choi, 2006) [33], where the run time is reduced by 40% for a memory bit-line layer composed of complicated 2D patterns with k1 factor smaller than 0.27. A solution for the cross-MEEF problem is introduced in (Cobb, 2002)[31] using Matrix OPC. Previous work in (Su, 2008)[34] is related to classic PID control theory. PID controllers have been applied to improve OPC convergence for 90-nm 6-T SRAM cells for both Active and Poly layers. A different idea for an OPC controller based on the optimization of the normalized image log slope (NILS) has been introduced in (Komirenko, 2011)[35] to achieve better process window. In this work the concept of EPE sensitivity has been introduced and investigated. The difference between MEEF and Sensitivity has been pointed out. The dynamic feedback controller has been tested on a medium size design ($30\mu m \times 20\mu m$) of a random logic interconnect layer. It is capable of achieving a run time reduction up to 50% with better OPC accuracy (quantified by the range of the remaining EPE) when compared to traditional OPC feedback schemes using constant or table driven feedback approaches. Further testing and investigation using larger layout including full chip layout is planned. The impact of the controller on OPC consistency and the implementation of MRC (mask rule check) rules (which are not considered in the current work) is an interesting topic for further studies.

3.5 Summary

A dynamic OPC feedback controller algorithm is introduced and compared to traditional, constant feedback OPC algorithms. By memorizing the EPE and displacement of each fragment from the preceding OPC iteration, an EPE sensitivity factor is introduced and calculated for each fragment. The feedback value for each fragment is decided based on the EPE sensitivity using a continuous, bounded function to assure continuous feedback values for better OPC convergence (and presumably

better OPC consistency). This algorithm shows improved performance in terms of OPC accuracy and run time compared to the conventional table driven feedback schemes. For the layout under test the dynamic feedback algorithm achieves an improved OPC accuracy characterized by an EPE range of 1.5nm compared to a constant feedback controller characterized by an EPE range of 2.75nm. An up to 50% run time reduction is realized since the dynamic feedback controller is using only half the iterations used by the constant feedback scheme. Additionally, the time for developing an OPC recipes using the dynamic feedback controller is shorter compared to the development time of a table driven feedback controller. Further testing and investigation for larger cases including full chip level is planned, especially in terms of OPC accuracy and consistency.

Chapter 4

Toward Golden Rules of SRAF Insertion

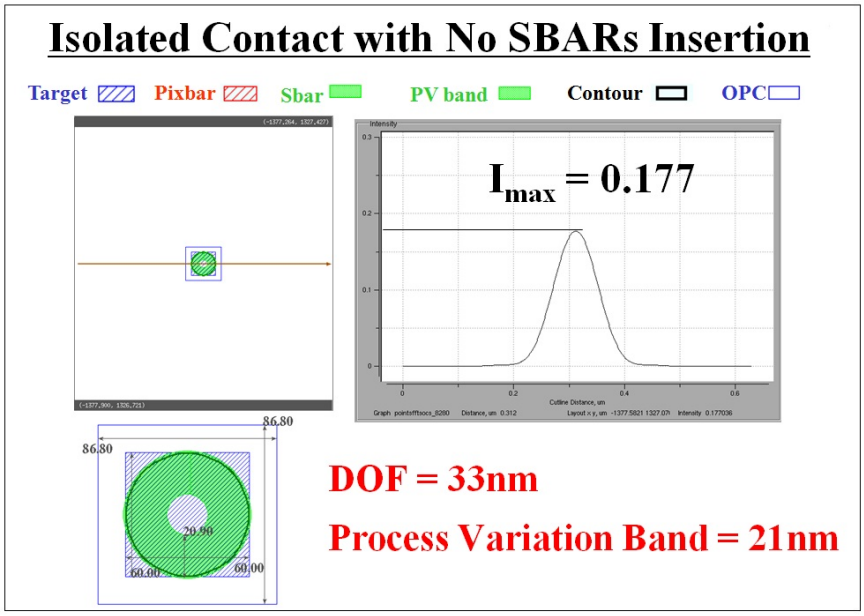
4.1 Introduction

A two-step full-chip simulation method for optimization of sub-resolution assist feature placement in a random logic Contact layer using ArF immersion Lithography is presented. Process window, characterized by depth of focus (DOF) , of square or rectangular target features is subject to optimization using the optical and resist effects described by calibrated models (Calibre® nmOPC, nmSRAF simulation platform). By variation of the assist feature dimension and their distance to main feature in a test pattern, a set of comprehensive rules is derived which is applied to generate raw assist features in a random logic layout. Concurrently with the generation of the OPC shapes for the main features, the raw assist feature become modified to maximize process window and to ensure non-printability of the assist features. In this work, the selection of a test pattern, the generation of a set of "golden" rules of the raw assist feature generation and their implementation as well as the assist feature coverage in a random logic layout is presented and discussed with respect to performance [1] .

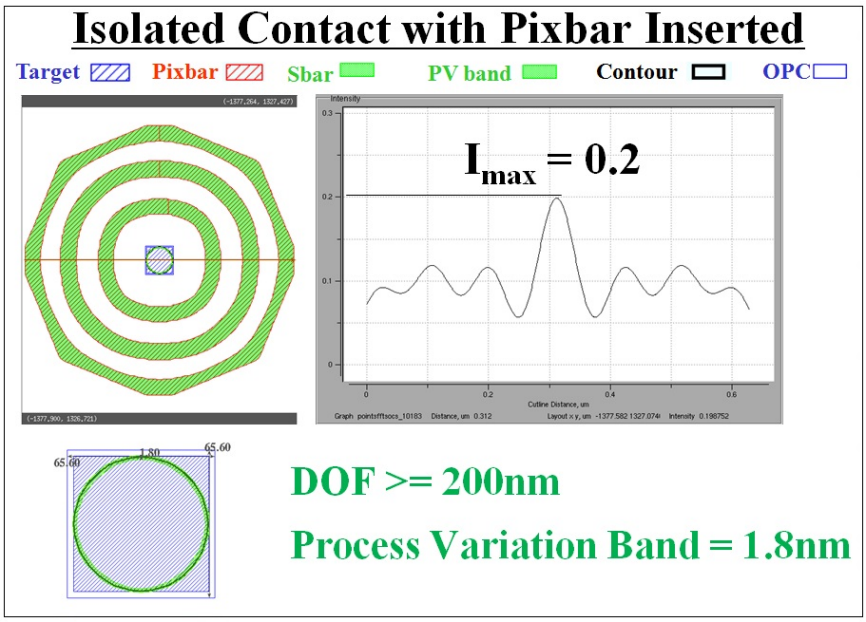
Semiconductor manufacturing is continuously ramping up the yield of technology processes with transistor dimensions well below the exposure wave length. Light diffraction effects limit the resolution of pattern with ever smaller dimension in ArF lithography using a fixed exposure wave length of 193nm and prevent printing wafer patterns identical to the shapes drawn on the exposure mask. Resolution enhancement techniques such as Optical Proximity Correction (OPC) enable new technologies to be realized in wafer manufacturing. Sub-resolution assist features (SRAF), or scatter bars (SB), provide critical process window enhancements in the lithography process. Traditionally, SRAF generation is based on geometric rules, which are extracted from a large amount of simulation and empirical wafer data from printing test masks.

4.2 SRAF Concept and Some Definitions

Before answering whether rule based SRAF will provide a sufficient process window for manufacturing, the effect, importance and value of SRAF insertion is illustrated in Figure 4.1. An isolated contact with no SRAF provides a small depth of focus (DOF) of $33nm$, a small I_{max} of 0.177 and a large process variability band (PVband) width of 21nm as shown in Figure 4.1a. A Pvband is the inverse intersection of images taken through focus and dose. The smallest image is created out of focus with small exposure dose, and the largest image is created in focus with a large dose. A decreasing Pvband correlates to increasing image quality, so a minimal PVband is desired. The Pvband where generated at $\pm$50nm defocus and $\pm$2.5% dose, the Pvband has been widely used to qualify image quality against process variation (dose, focus) as described in both (Kempsell, 2009)[20] and (Jayaram , 2007)[19]. The DOF is calculated at $\pm$100nm focus variation and 5% exposure latitude (EL) using the methodology described in (Lin, 2010)[6] and (Mack, 2008) [7]. After insertion of pixilated SRAF generated from Mentor Graphics Pixbar inverse lithography routine described in (Granik, 2008)[36] the Pvband width is reduced to 1.8nm, I_{max} increased to 0.2 and DOF increased to 200nm as shown in



(a) Without SRAF

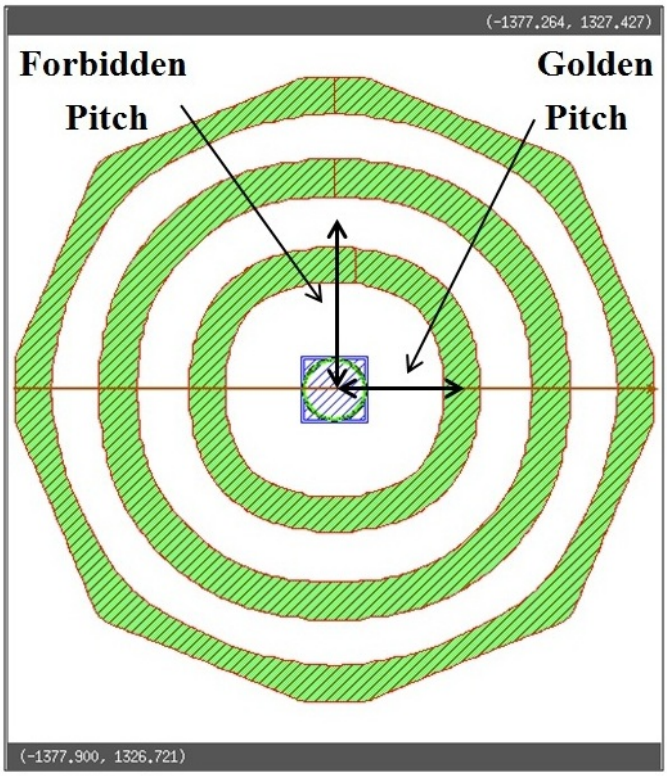


(b) With SRAF

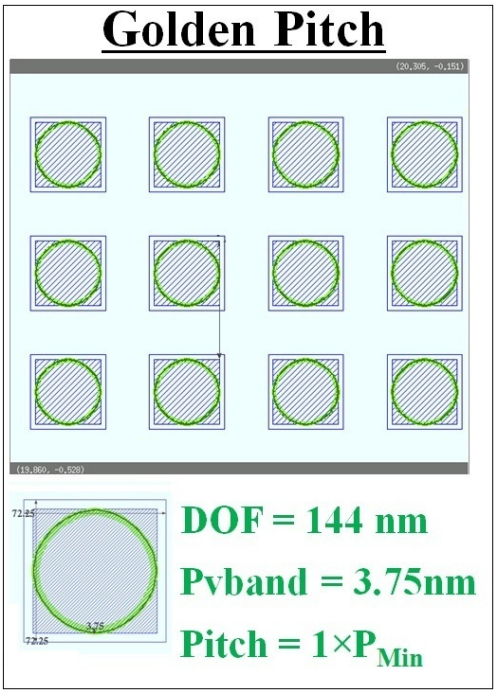
Figure 4.1: Aerial Image, DOF and process window variation band (pvband) for isolated contact without and with SRAF insertion (Pixbar). An Isolated contact with no SRAF exhibits a small DOF = $33nm$, a small $I_{max} = 0.177$ and a large pvband width of 21nm. The isolated contact with SRAF generated from Pixbar shows a larger DOF $\geq 200nm$, a larger $I_{max} = 0.2$ and a much narrower pvband width of 1.8nm

Figure (1-b). Pixbar optimizes pixels on mask with respect to a build-in objective function in order to meet a given target dimension and process window requirement without changing the shape of the illuminator. Ideally, Pixbar SRAF insertion brings all pattern as close as possible to the isofocal condition, therefore, maximizing DOF and common process window by, firstly, changing the spatial frequency of the mask closer to the preferred frequency that the fixed, pre-selected illumination source does support best, and, secondly, allowing more light passing through the mask without printing SRAF and maximizing the intensity (I_{max}) of the main feature contacts, and, thirdly, increasing the contrast and the normalized intensity log slope (NILS) of the main features. A narrower process variation band (PVband) is the result of the resolution enhancement (exposure latitude (EL) expansion and depth of focus (DOF) increase) caused by optimized SRAF insertion.

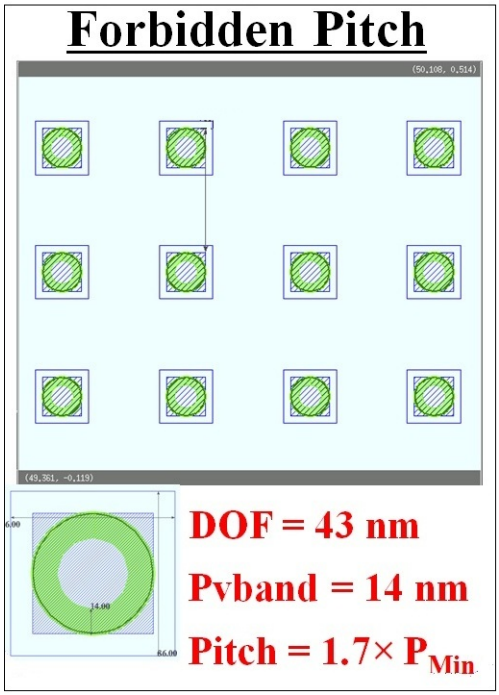
In many Lithography Processes the iso-focal condition is met, or nearly met, by the smallest contact pitch that is allowed by the design rule for a given technology node. In symmetric, repeating pattern this pitch is sometimes refered to as the "Golden Pitch" because it provides maximum process window characterized by the largest DOF and the smallest Pvband width. Except for the outer boundaries of these regular patterns there is no space and no need for any SRAF insertion. For a fixed source shape of the illuminator, Pixbar will generate an SRAF pattern which matches the golden pitch closely, therefore, the isolated contact with Pixbar generated SRAFs much closer to the iso-focal condition. The optimum spacing of the SRAFs with respect to the isolated, main feature contact (first, second, third ring of SRAF) is determined from the Pixbar insertion result of isolated contact pattern depicted in Figure 4.2a. The distance between the center of the main feature to the center of the first ring of Pixbar generated SRAF is refered to as the golden pitch. Figure 4.2b shows an example of a contact array inserted at the golden pitch, providing a DOF of 144nm accompanied with a Pvband width of 3.75nm.



(a) Golden and Forbidden Pitch Definition



(b) Golden Pitch Example



(c) Forbidden Pitch Example

Figure 4.2: Definition and determination of the forbidden pitch and golden pitch

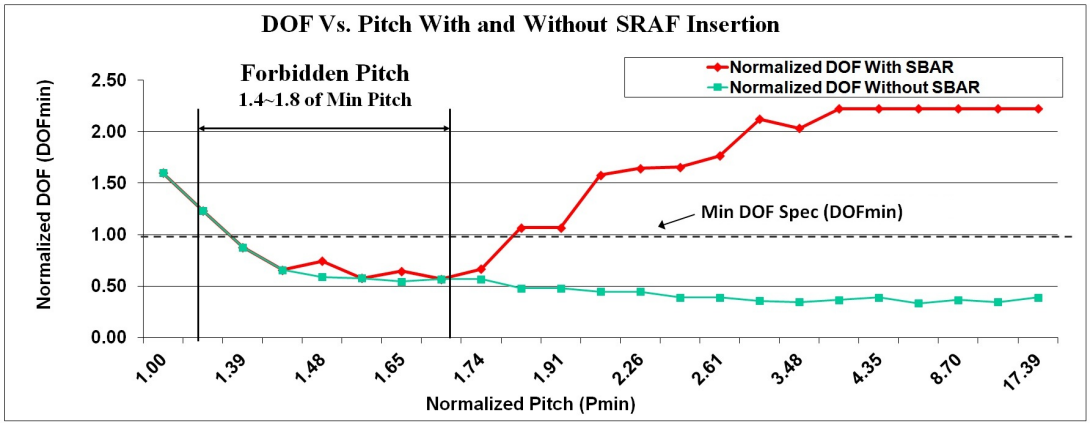


Figure 4.3: Pitch versus DOF with and without SRAF insertion in a symmetric 2D array of contacts. SRAF insertion is improving the DOF of semi-dense and isolated contacts, but fails to substantially increase the common process window limited by the forbidden pitch.

In contrast, the forbidden pitch provides the narrowest process window (smallest DOF and widest Pvband). Since the forbidden pitch is limiting the common process window, its exact determination in a manufacturing process is important. Dependent on the shape of the illuminator, the forbidden pitch is found in a range between 1.4 and 1.8 times the minimum pitch (P_{min}) or design rule of a given technology node. If the mask manufacturing rules allow SRAF insertion at the forbidden pitch, the common process window increases substantially. If not, careful source optimization is one option to increase the common process window. Prior to mask manufacturing, a massive amount of simulations are usually performed to find a compromise between resolution needed at the golden pitch and depth of focus required at the forbidden pitch, by changing SRAF insertion rules optimized for a changing source shape of the illuminator. A good estimation of the forbidden pitch is found from the Pixbar SRAF insertion results of an isolated contact as shown in Figure 4.2a. The distance between the center of the main feature to the center of the free space between the first and second ring of Pixbar generated SRAF is referred to as the forbidden pitch. Figure 4.2c show an example of contact array inserted at forbidden pitch, the DOF at this pitch is equal to 43nm with a large Pvband

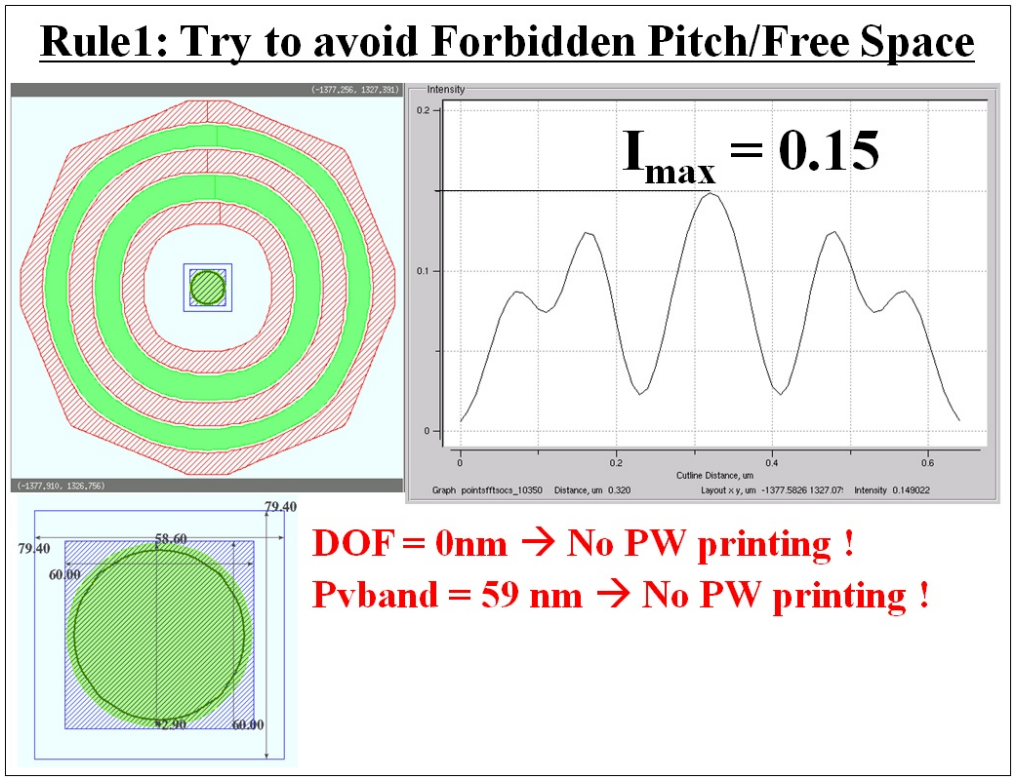
width of 14nm. Insertion of SRAF at locations that creates a forbidden pitch is highly unfavorable because it usually decreases the DOF of the main features, and a mask with incorrect SRAF will provide a smaller process window compared to a mask without SRAF.

Figure 4.3 illustrates the concept of the forbidden pitch. The DOF of a nested contact array with and without SRAF insertion are plotted as a function of the pitch of symmetric 2D array. Without SRAF insertion the golden pitch (P_{min}) exhibits the highest DOF, but isolated and semi-isolated contact arrays exhibit no or a very small simulated DOF. With SRAF insertion, the simulated DOF at the golden pitch is unchanged (because there is not enough space to insert SRAF), but isolated and semi-isolated contact arrays exhibit a substantially improved DOF. However, in this case study the DOF at the forbidden pitch may still be unacceptable, because SRAF insertion fails to improve the common process window limited by the forbidden pitch.

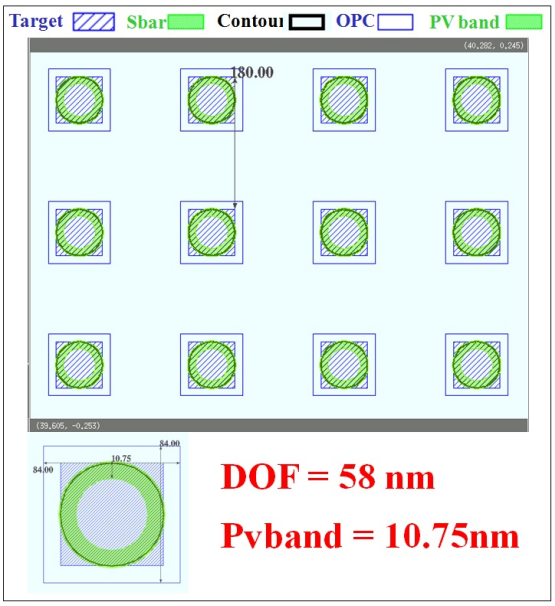
An ArF scanner setting of NA 1.32 in conjunction with an annular illumination source is used for all simulations in this work. Source shape variation of the illuminator and their effects on SRAF insertion and common process window are beyond the scope of this work, however, the effect of various source shapes on SRAF generated by Pixbar is described in (Sturtevant, 2010)[37].

4.3 Golden Rules of SRAF Insertion

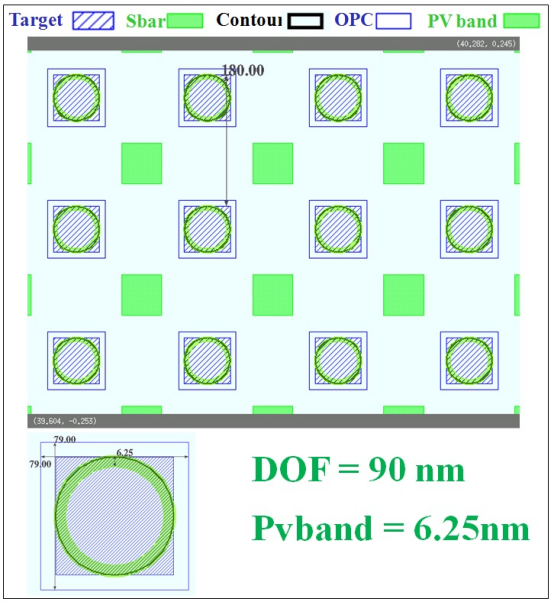
In this section the determination of a set of SRAF building rules is described based on the Pixbar SRAF result obtained for the isolated contact pattern. Figure 4.4 illustrates the "Avoid forbidden pitch or free spaces" SRAF placement rule. For demonstration SRAFs have been inserted at a distance of the main feature isolated contact which is close to the forbidden pitch (this is between the rings of the Pixbar generated SRAF) as depicted in Figure 4.4a. The isolated contact may not print, there is no process window, the DOF equals 0nm and the PVband has no inner



(a) Avoid Forbidden Pitch

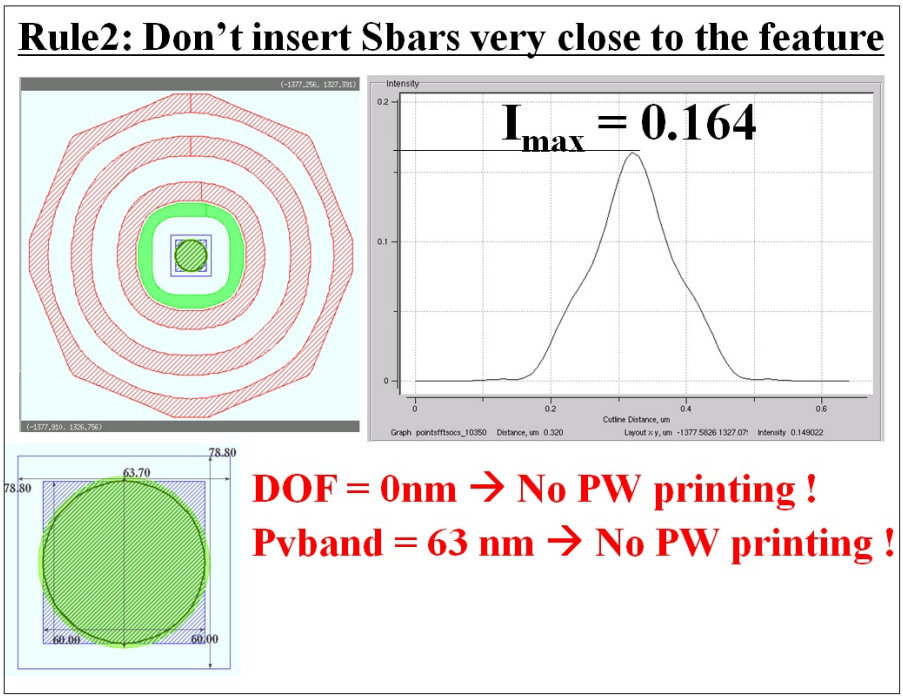


(b) Missing SRAF

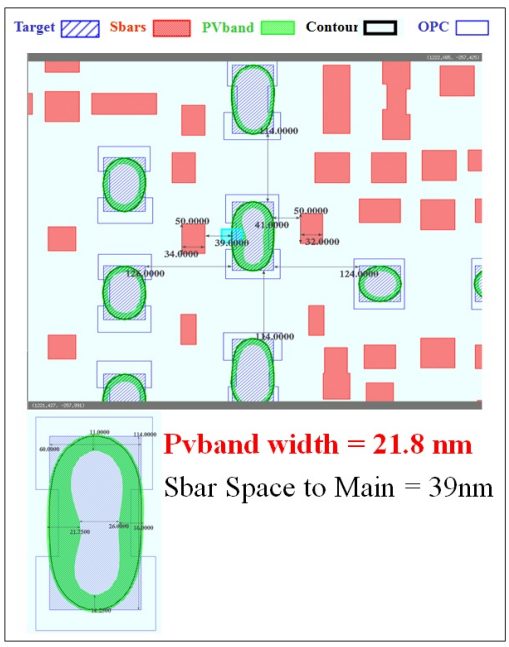


(c) Inserted SRAF

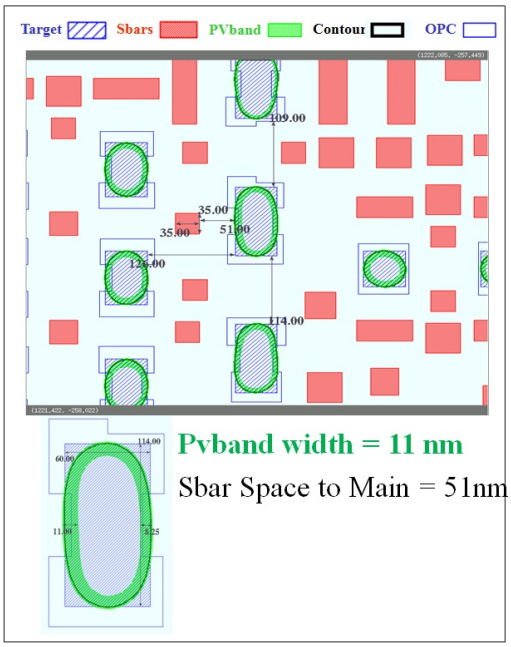
Figure 4.4: a) Islolated contact pattern with Pixbar and badly placed SRAF near the forbidden pitch reducing the DOF compared to a pattern with no SRAF. b), c) Demonstration of the critcial SRAF insertion close to the forbidden pitch



(a) Avoid Small Space



(b) Too Close SRAF



(c) Good SRAF

Figure 4.5: a) Isolated contact with the first ring of inverse Pixbar generated SRAF, b) real layout of random logic design with SRAF at 39nm space from main feature providing no process window improvement c) Increaing the space between main feature contact and the SRAF by addional 12nm, the process window improves substantially.

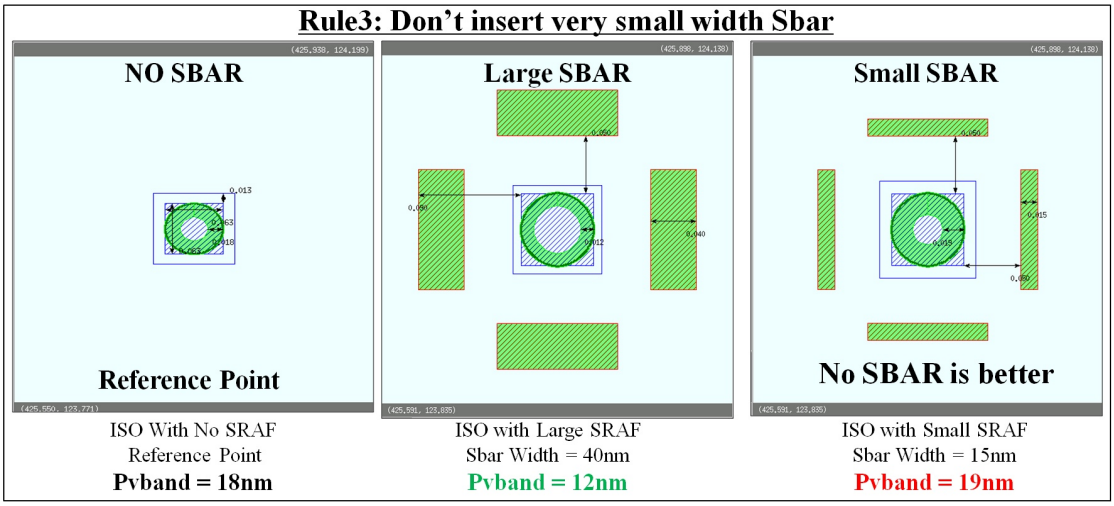


Figure 4.6: Insertion of very small size SRAF may be worse compared to no SRAF insertion.

contour (closed Pvband) equal to 59nm, therefore, covering the entire contact. The process window and PVband width is worse compared to an isolated contact without SRAF shown in Figure 4.1a. The process window reduction is due to the insertion of SRAF at a location which is not supported by the illuminator. Figure 4.4b and Figure 4.4c show a nested contact array with and without SRAF insertion. The main feature contact pitch is close to the forbidden pitch ($1.8P_{min}$). With no SRAF insertion the DOF measures 58nm and a Pvband width of 10.75nm. However, with SRAF insertion the process window is improved substantially, and the DOF reaches 90nm and a Pvband width of 6.25nm. As a conclusion, SRAF insertion must avoid forming any forbidden pitch. This is relatively easy in regular, symmetric 2D arrays of contacts, but not intuitively achievable in complex random logic patterns. On the other hand, a maximum number of SRAF placed to leave as little as possible uncovered space with no SRAFs is favorable, if the formation of the forbidden pitch is avoided. Avoiding placement of SRAFs in the wrong position is a high priority because it may cause the formation of a hot spot location with little or no DOF at all.

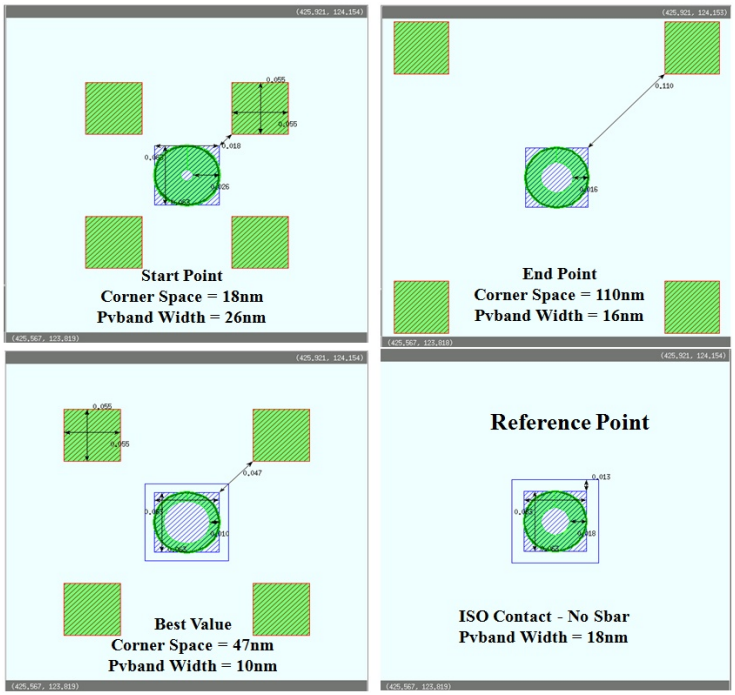
Figure 4.5 illustrates the "Don't insert SRAFs too close to the main feature" rule. Figure 4.5a depicts the insertion of SRAF too close to the main feature. The isolated contact may not print due to a lack of process window, the simulated DOF reads 0nm, and the PVband has no inner contour (closed Pvband) and covers the entire contact (63nm). In terms of process window this result is worse compared to the isolated contact without SRAF shown in Figure 4.1a. The placement of SRAF too close to the main contact feature is causing the collapse of the process window. Figure 4.5b depicts a real case from random logic layout (contact layer). Insertion of SRAF at a distance of 39nm to the rectangular contacts shows a small process window and a wide Pvband of 21.8nm. Pulling back the SRAFs by 12nm, the process window improves substantially as shown in Figure 4.5c. The Pvband narrows and reaches a width of 11nm. Insertion of SRAF too close to the main feature must be avoided. Sometimes in order to comply with the rule "Avoid forbidden pitch or free spaces" there is a temptation to place too many SRAF too close to the main features. A better strategy for SRAF placement may be a lesser number of SRAF but all placed at the correct distances avoiding the forbidden pitch and a placement too close to the main features.

Figure 4.6 illustrates the "Don't insert very Small SRAF" rule. Inserting SRAF at 50nm space to main contact with two different sizes (40nm and 15nm) are compared. The Insertion of the larger 40nm SRAF width improves the process window causing a moderate PVband width of 12nm. Contrary, the Insertion of a 15nm wide SRAF does not improve the process window as can be seen from the wider 19nm PVband. Insertion of the small 15nm wide SRAF provides smaller PVband width compared to the isolated contact without SRAF (18nm PVband width). Insertion of a small SRAF leads to the formation of a smaller pitch (in symmetric pattern, sum of half of the contact width and half of the SRAF width and the distance between them). This example illustrates that the insertion of very small SRAF does not improve the process window substantially and may be avoided as much as possible. In general, the insertion of larger non printing SRAF at a favorable distance to the main feature and to each other is preferred.

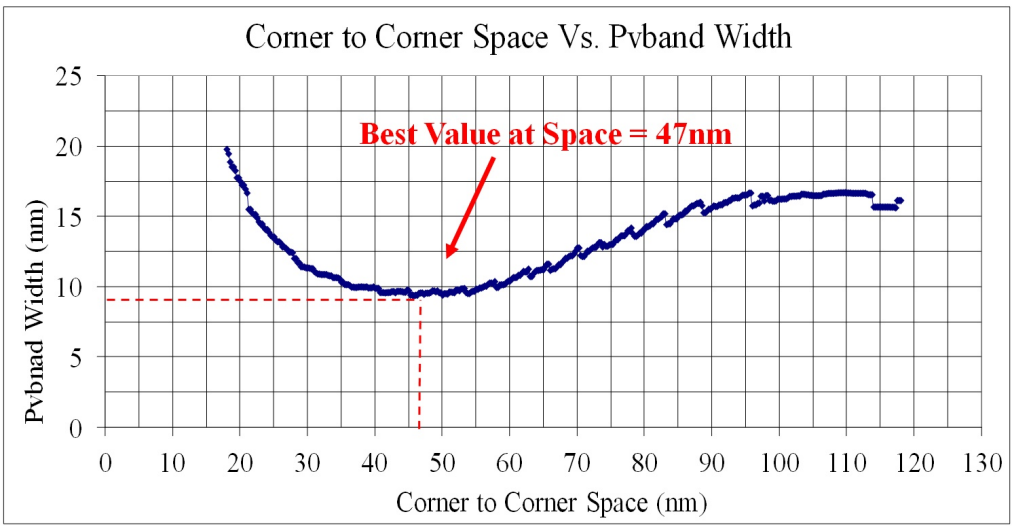
4.4 Optimization of SRAF insertion

Identification of the optimum placement of SRAFs in relatively simple patterns such as the isolated contact provides a reasonable starting point for the creation of a SRAF recipe. Figure 4.7 outlines an experiment for identification of optimum SRAF placement. In an isolated contact pattern four SBARs are inserted corners to corner with a fixed size of 55nm. The corner to corner distance between main feature and SRAF is varied from very close (18nm) to very far (110nm) in small steps of 1nm and the Pvband width is measured in each of the resulting patterns and plotted as a function of the corner to corner distance. The results are compared to the isolated contact without SRAFs (reference) as shown in Figure 4.7a. Figure 4.7b plots the Pvband width versus the corner to corner distance between SRAF and main feature space. A wide PVband width results for very close SRAF to main feature corner to corner spacing (18nm) indicating a relatively poor process window (Pvband width of 26nm). A PVband width of 16nm corresponds to a SRAF corner to corner placement of 110nm also indicating an insufficient process window. An optimum corner to corner placement of 47nm emerges. The maximum achievable process window is characterized by a PVband width of 10nm.

Figure 4.8a shows a range of corner to corner SRAF to mainfeature distances in which the PVband width is not changing significantly (flat plateau in the graph from 35nm to 55nm corner to corner distance and with a Pvband width of $\sim$10nm). This region of spaces is favorable for SRAF placement and it is a specific signature for a given illuminator. The wider this plateau provided by the illuminator the easier the writing of a SRAF insertion recipe with good SRAF insertion coverage and lesser chance for a missing or badly placed SRAF. This plateau is an important characteristic of an illuminator, because it provides a degree of freedom for SRAF rule creation. The larger the plateau the more compact the SRAF insertion recipe is. The lesser complexity of the SRAF recipe also simplifies its maintenance, documentation and version control. Predominantly it also speeds up the process of SRAF recipe creation and testing. Figure 4.8b shows the effect of varying SRAF

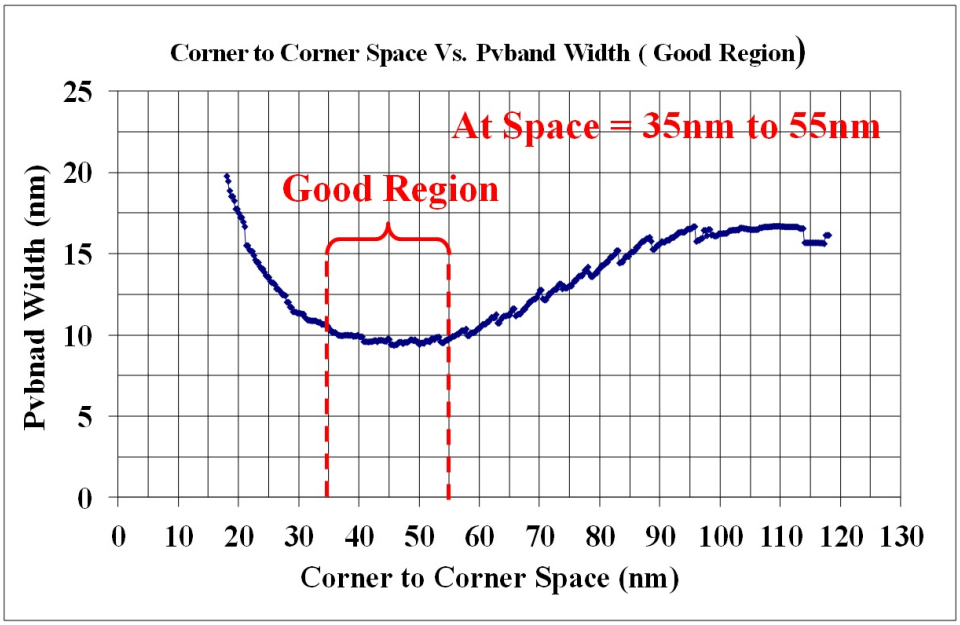


(a) Pvband Vs SBAR Space Experiment

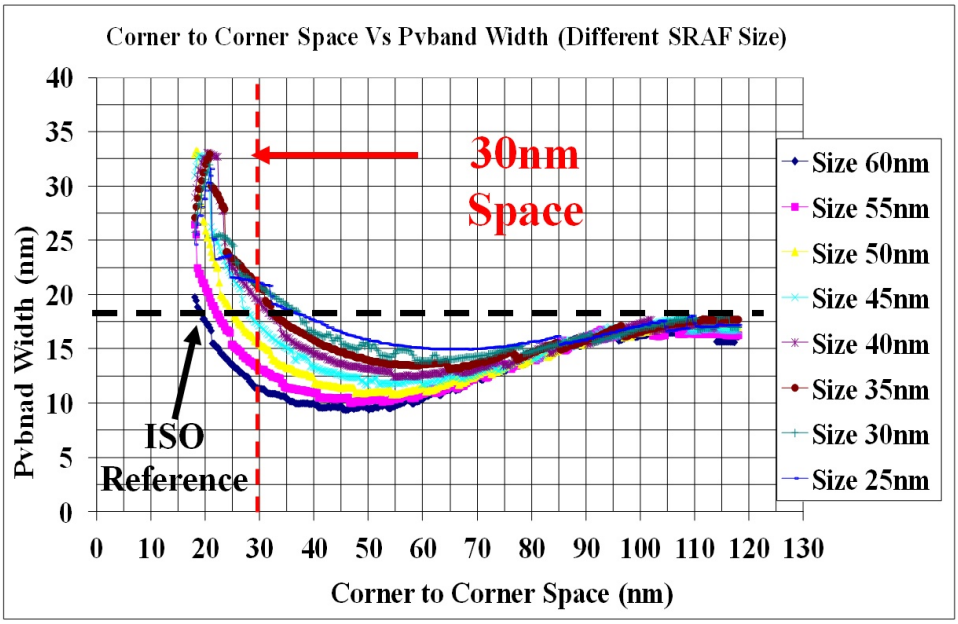


(b) Best SRAF Location

Figure 4.7: Pvband width versus Corner to Corner spacing between SRAF and the main feature contact: Insertion of four corner SRAFs with fixed size, varying their distance to the main feature from very close (18nm) to very far (110nm) in steps of 1nm. A SRAF placement too close to the main feature cause a wider PVband and a SRAF placement too far from the main feature is inefficient and also causes a larger PVband indicating poor process window. There is an optimum spaceing inbetween. The optimum corner to corner SRAF to main feature distance reads 47nm.



(a) Good Region



(b) Different SRAF Sizes

Figure 4.8: a) For the given annular illuminator, there is relatively wide region of "good" SRAF to main feature spacing, in which the Pvband width is almost constant (flat from space 35nm to 55nm). b) PVband width versus SRAF spacing to main feature at different SRAF width. A larger SRAF width provides narrower PVbands indicating a larger process window. Smaller SRAF width causes the SRAFs placement too close to the main feature and is not favorable. This graphs reconfirms the optimimum spaceing of the SRAF to main features again.

size (width) on process window. The SRAF width is chosen from 25nm to up to 60nm in 5nm steps.The 60nm SRAF provides the optimum process window (narrowest Pvband) where as 25nm SRAF width exhibits the poorest process window indicated by the widest Pvband. At a space of 30nm indicated by the vertical red dashed line shown in Figure 4.8b the PVband width is larger (22nm) for the 25nm wide SRAF compared to the isolated contact without SRAF showing a PVband width of 18nm indicated by the horizontal black dashed line. On the contrary, a SRAF width of 60nm leads to a very narrow PVband (11nm) indicating a sufficient process window, however, careful checking of the SRAF printing margin raises concerns. The optimum SRAF size is inbetween. A concurrent adjustment to the size of the SRAF along with the convergence of the OPC for the main features may be necessary to ensure maximum process window for the main features along with insurance of a predefined SRAF printing margin.

Pixbar SRAF insertion results are shown in Figure 4.1b. The Pixbar results provide a reference for the generation of a first SRAF recipe trying to match the Pixbar results as close as possible. In some regular pattern Pixbar may find two or more different SRAF placements with very similar or same process window. This may cause an inconsistent SRAF placement by Pixbar. The matched rule-based SRAF recipe will chose only one of the Pixbar solutions and therefore will avoid inconsistency in the SRAF placement during tape out.

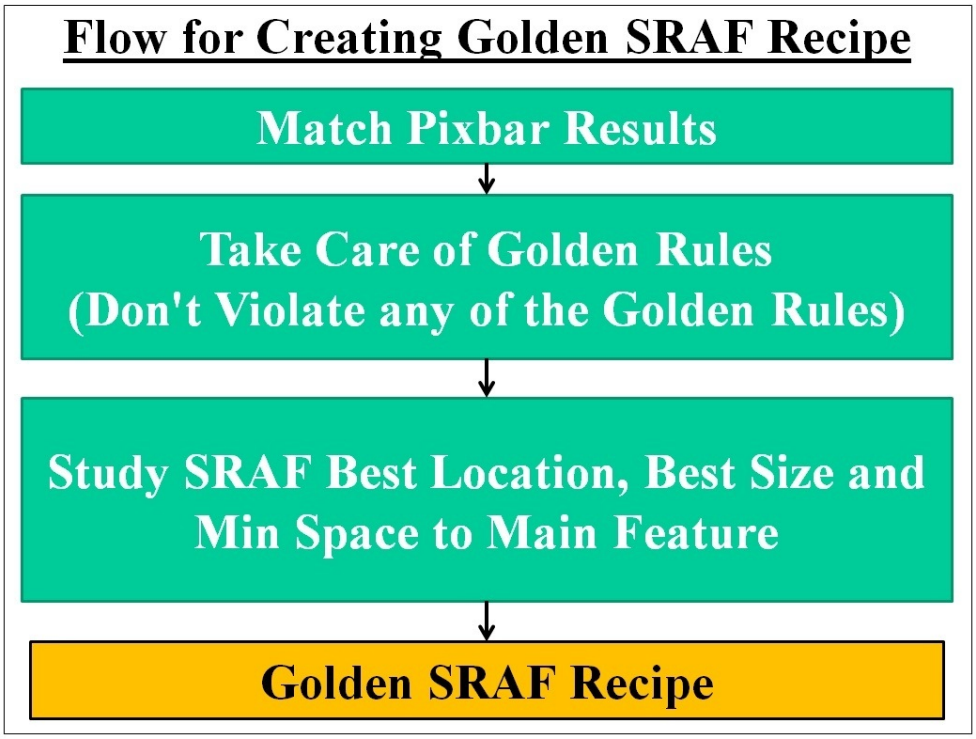
Figure 4.9a illustrates a methodology for rule based SRAF recipe creation. Firstly, Pixbar provides a reference for SRAF generation in test patterns which are matched by a rule based SRAF recipe using nmSRAF. The rules are designed to comply with the set of "golden" rules described in section 4.3. Secondly, a detailed analysis to find the optimum SRAF placement in relatively simple and regular patterns helps the generation of compact SRAF recipes as described in this section 4.4. Careful testing of a SRAF recipe is required. Automatic generation of test layouts helps to debug an SRAF recipes, especially to avoid missing SRAFs or violations of the golden SRAF placement rules. The test pattern used for creation

of the golden SRAF recipe is described in Figure 4.9b. Compared to many Model based SRAF solutions, rule based SRAF generation is very fast, allowing testing of a vast amount of layout for ensuring SRAF recipe quality.

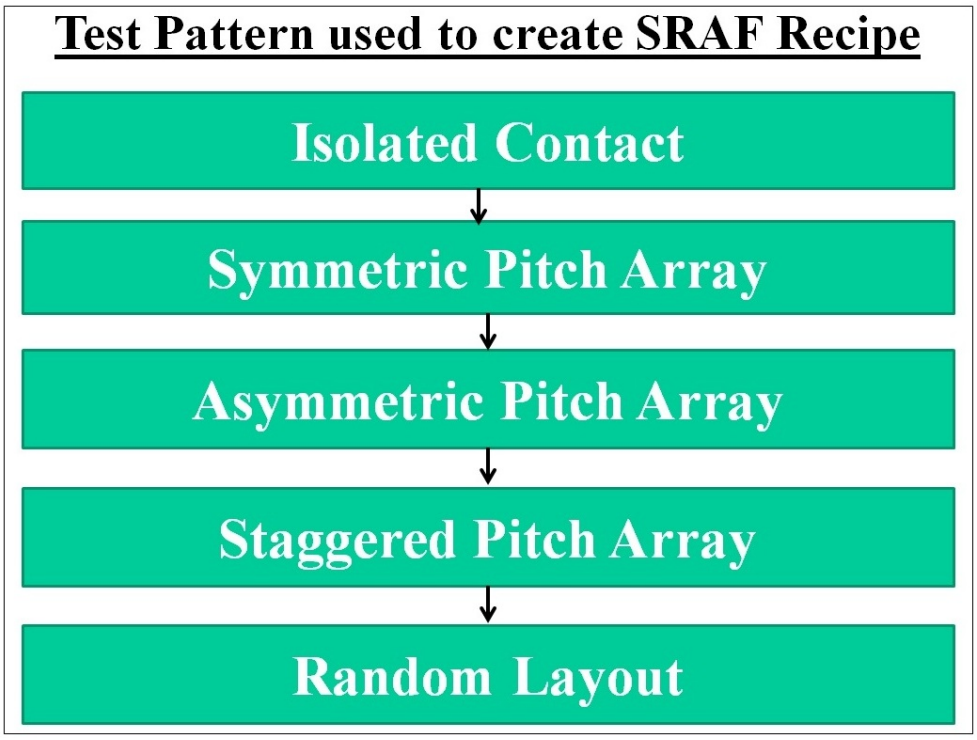
4.5 Experiment And Results

A larger test case contact layout is required to prove statistically that the new SRAF insertion algorithm provides a larger process window compared to the traditional flow. A medium size design ($30\mu m \times 20\mu m$) of random logic interconnects are used for testing. The new SRAF insertion flow shown in Figure 4.10b and the traditional SRAF insertion algorithms are explained in Figure 4.10a and are compared in terms of process window, DOF and mask error enhancement factor (MEEF) described in (Levinson, 2011) [8]. To avoid SRAF printing, both SRAF insertion flow rely on Calibre® nmOPC to adjust SRAF sizes as described in (Chou, 2008)[32]. DOF, Pvband width and MEEF are calculated using Calibre® OPCVerify. The DOF histogram comparing both SRAF insertion algorithms are shown in Figure 4.11. The new SRAF insertion algorithm (Figure 4.11b) displays a significantly improved focus distribution characterized by a normalized DOF ranging from 1 to 2.25 with a zero number of "DOF outliers" at the far left end side of the distribution. The traditional SRAF insertion flow displays a much wider normalized DOF distribution ranging from 0.25 to 1.25 of minimum DOF as shown in Figure 4.11a.

The MEEF histogram for both algorithms are depicted in Figure 4.12. The new SRAF insertion algorithm (Figure 4.12b) shows a histogram of MEEF ranging from 2 to 5 with a zero number of "MEEF outliers" at the far right of the distribution. The traditional SRAF insertion algorithm is characterized by a much wider range of MEEF ranging from 2 to 8 as shown in Figure 4.12a. This result is remarkable since, both, the new SRAF insertion flow as well as the traditional flow, used the same algorithm for SRAF size adjustments applied concurrently to OPC. This emphasizes the importance of an optimized SRAF seed placement. Remarkably,

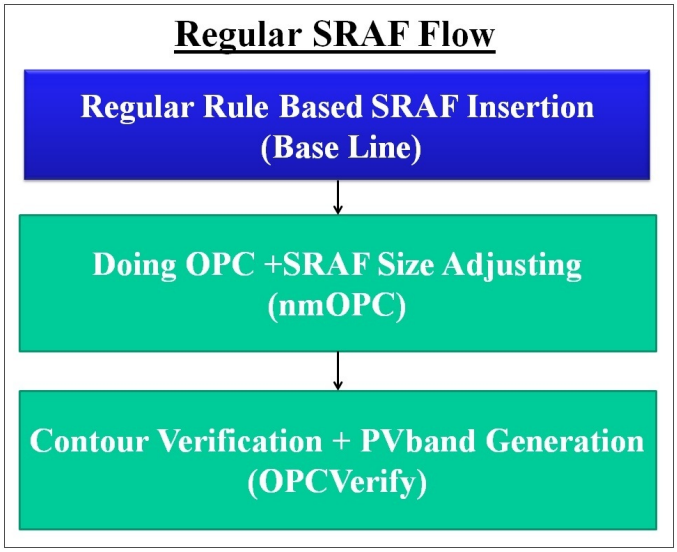


(a) Creating SRAF golden recipe flow

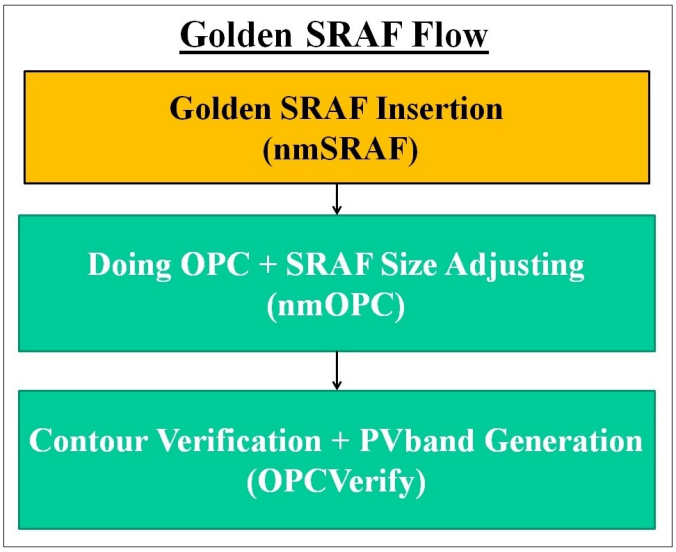


(b) Test pattern used

Figure 4.9: Creation of a SRAF recipe

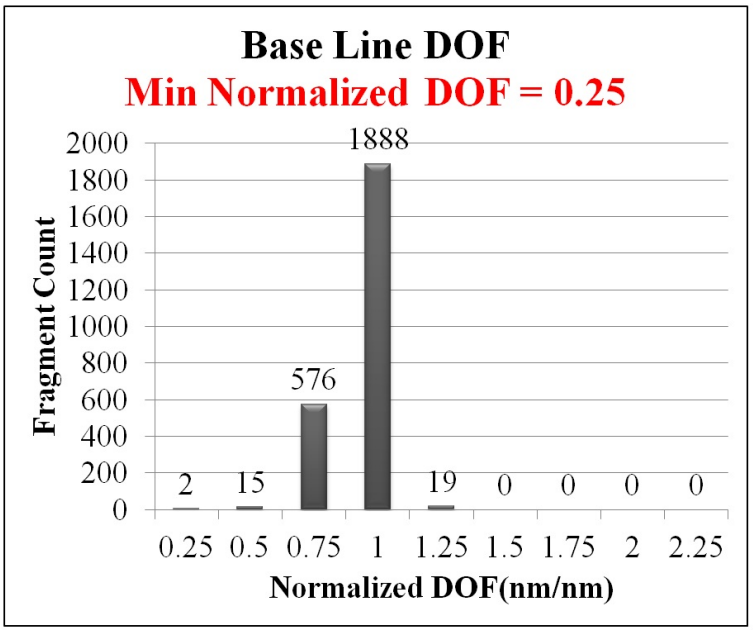


(a) Base Line

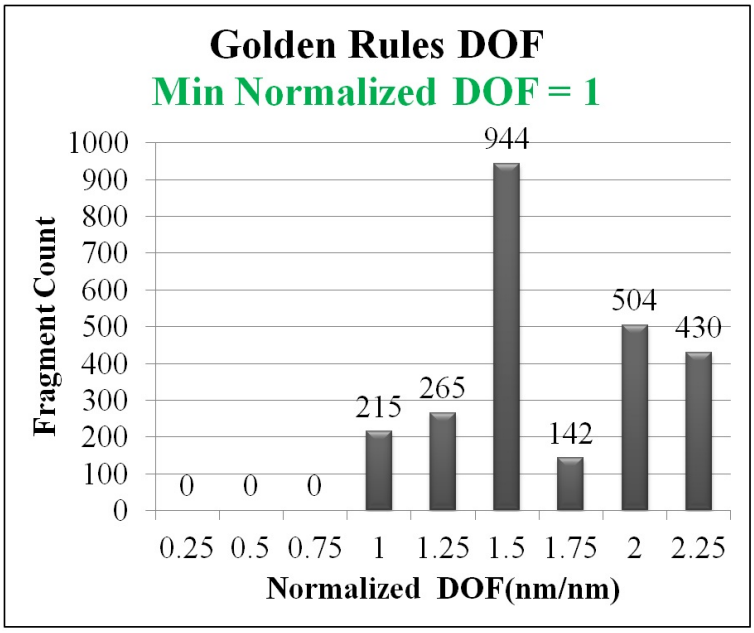


(b) Golden SRAF

Figure 4.10: New SRAF insertion flow versus traditional SRAF insertion flow. In the new SRAF flow, seed SRAF shapes are created by rules considering the location of main feature contacts as well as other SRAF seed shapes using Calibre® nmSRAF. Concurrently with the OPC, the SRAF seed shapes are subject to modifications (movements of SRAF seed edges) based on algorithms which consider mask making constrains as well as the optical image as generated from opc models. In the traditional SRAF insertion flow, final SRAF shapes are generated prior to OPC using tables. In both flows during the application of nmOPC, the SRAF size is adjusted only if SRAF printing in Calibre® nmOPC is detected. Final confirmation is obtained from Calibre® OPCverify measuring DOF, Pvband width, MEEF and extra printing.

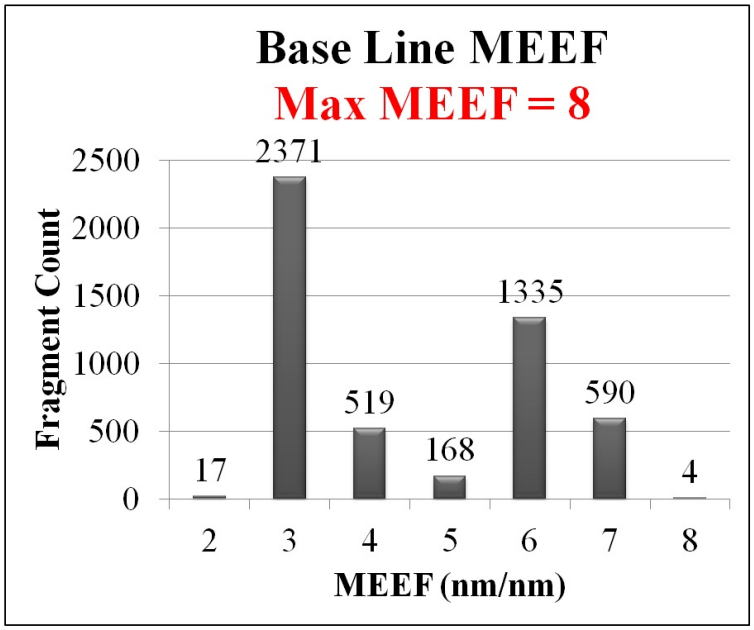


(a) Base Line

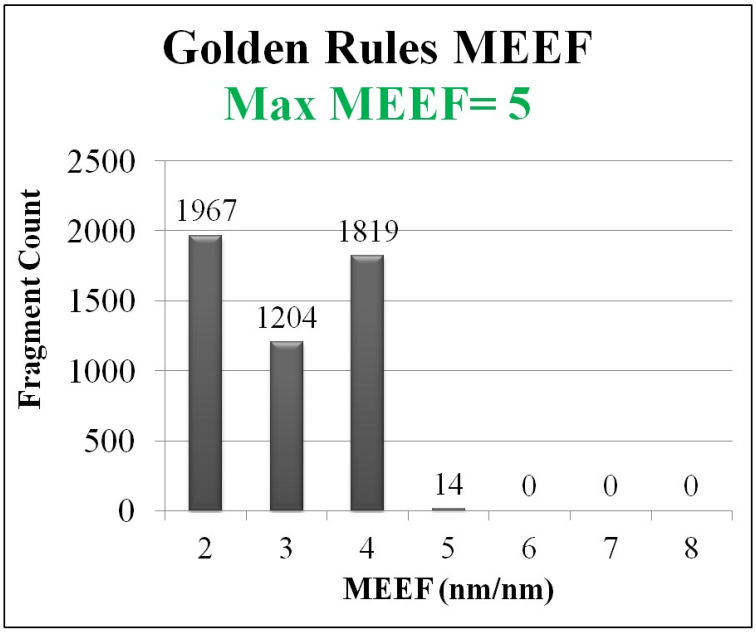


(b) Golden SRAF

Figure 4.11: DOF histogram for a medium size layout ($30\mu m \times 20\mu m$). The new SRAF insertion algorithm achieves a larger process window characterized by a normalized DOF ranging from 1 to 2.25, compared to the traditional SRAF insertion characterized by a normalized DOF ragning from 0.25 to 1.25. The new SRAF insertion algorithm causes a 75% increase for the Minimum DOF and the common process window.



(a) Base Line



(b) Golden SRAF

Figure 4.12: MEEF histogram for a medium size layout ($30\mu m \times 20\mu m$). The new SRAF insertion algorithm shows a maximum MEEF of 5, compared to a maximum MEEF of 8 for the traditional SRAF insertion. The new SRAF insertion algorithm significantly reduces the maximum MEEF from 8 to 5.

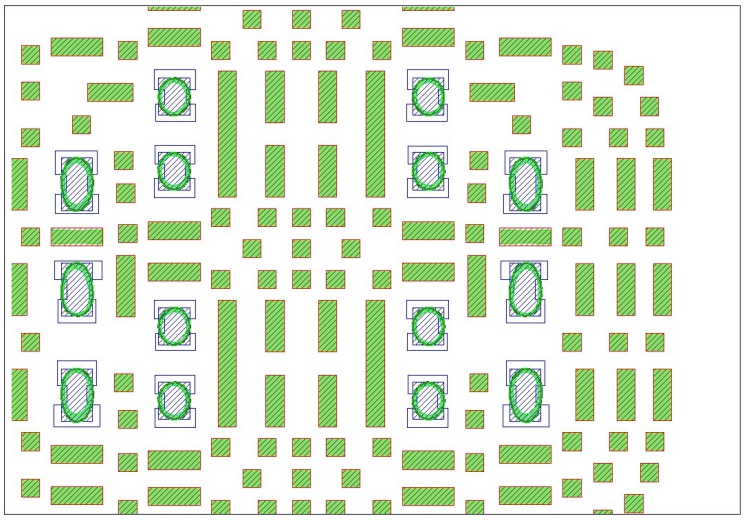
the common process window increases by 75% (minimum DOF) accompanied by a significant reduction of MEEF from 8 to 5.

The new SRAF seed placement recipe consists of a larger number of rules compared to the traditional SRAF placement table. It is therefore more difficult to build and takes more effort to test and debug. In our case study two weeks of an experienced engineer were needed to create the SRAF recipe. Testing and debugging may require a similar time dependent on the depth of the test. Automated layout generation as well as a set of full chip layouts along with a selection of previously collected hotspots may be useful for testing and debugging. Generation of the SRAF seeds is rule based and quick compared to completion of the full OPC. The quality of the SRAF seed placement may be checked by DRC before investing more cpu resources for checking the post OPC layout in terms of process window, DOF and MEEF and convergence of the OPC.

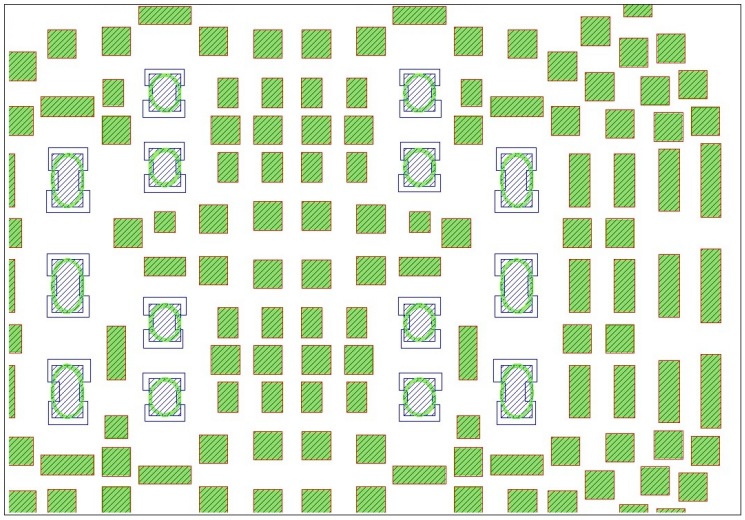
As an example, Figure 4.13 shows two pattern in the medium size layout used for generation of the results described in Figure 4.11 and Figure 4.12 . Various proximities and interconnect shapes are included such as squares and rectangles of various aspect ratio. SRAF generation is using Mentor Graphics Calibre® nmSRAF software. Figure 4.13b shows a symmetric design of main feature contacts. Since the SRAF seed generation is rule based, it is consistent and symmetric, therefore, the SRAF seed placement does not break the symmetry of the main features, if a sufficiently high resolution of the resulting layout is used. After OPC is applied the consistency and symmetry may be broken by 1 to 2 database units (dbu) per side of either SRAF or main feature after OPC. Such differences may be larger, if either SRAF or main feature OPC is constrained by mask rules.

4.6 Summary

A new two step SRAF insertion flow (rule based SRAF seed placement followed by model based growth of the SRAF seeds concurrent to OPC) is compared to a trac-



(a) Base Line



(b) Golden SRAF

Figure 4.13: Two snapshots taken from the medium size design using 2 different SRAF insertion algorithms: a) the new SRAF insertion algorithm, and b) the traditional SRAF insertion algorithm. Square and rectangular interconect shapes with various aspect ratio as part of an interconect layer of a medium size random logic design are shown along with PVbands. The new SRAF insertion alogrithms shows visibly narrower PVbands which indicates a significantly larger process window. Please notice that "missing SRAF" is not the reason for the process window improvement since both algorithms fill the area around the main features with SRAF well. The exact position and size of each SRAF shape creates the differece (There is no significant difference regarding the convergence of the OPC in both cases).

tional rule based SRAF insertion flow. Consistent SRAF seed placement is achieved by rules generated from inverse Lithography (Pixbar) results in test pattern. For a given annular illuminator a set of basic SRAF insertion rules is derived from process window analysis in test pattern. A medium size random logic interconnect layout (square and rectangular contact shapes) is used for SRAF recipe testing and process window analysis. The new SRAF insertion flow increases the common process window by 75% and reduces maximum MEEF from 8 to 5 when comparing to the tractional SRAF insertion flow. The rule based SRAF seed generation completes in $\sim$3.5% of the model based OPC (nmOPC) runtime over a full chip layout in a distributed cpu cluster. An analysis of DOF and MEEF is presented to compare process window for both SRAF insertion flows. The new SRAF insertion flow requires setting up a more complex nmSRAF insertion recipe which also requires more time for testing and debugging before tape out. During the early stage of process development, frequent changes of the illuminator would require changes to the SRAF recipe which may not be practical, however, in the stage of a more mature process closer to production, the new flow provides significant improvements in terms of performance and consistency of the resulting mask.

Chapter 5

Conclusions and Future Work

Survey about different advanced Lithography steps in the 45nm and beyond is presented. The Fourier Optics and how it affects the minimum dimension on wafer is briefly discussed. Lithography metrics and how we measure its quality is then reviewed. A study about the different aspects of the Resolution Enhancement Techniques used currently in the industry for the 45nm technology node and beyond is presented. Focusing on both Optical Proximity Correction (OPC) and Sub-Resolutions Assist Features (SRAF) as a key techniques to enable theses advanced technologies to be realized.

A dynamic OPC feedback controller algorithm is introduced and compared to traditional, constant feedback OPC algorithms. By memorizing the EPE and displacement of each fragment from the preceding OPC iteration, an EPE sensitivity factor is introduced and calculated for each fragment. The feedback value for each fragment is decided based on the EPE sensitivity using a continuous, bounded function to assure continuous feedback values for better OPC convergence (and presumably better OPC consistency). This algorithm shows improved performance in terms of OPC accuracy and run time compared to the conventional table driven feedback schemes. For the layout under test the dynamic feedback algorithm achieves an improved OPC accuracy characterized by an EPE range of 1.5nm compared to a constant feedback controller characterized by an EPE range

of 2.75nm. An up to 50% run time reduction is realized since the dynamic feedback controller is using only half the iterations used by the constant feedback scheme. Additionally, the time for developing an OPC recipes using the dynamic feedback controller is shorter compared to the development time of a table driven feedback controller. Further testing and investigation for larger cases including full chip level is planned, especially in terms of OPC accuracy and consistency.

A new two step SRAF insertion flow (rule based SRAF seed placement followed by model based growth of the SRAF seeds concurrent to OPC) is compared to a tractional rule based SRAF insertion flow. Consistent SRAF seed placement is achieved by rules generated from inverse Lithography (Pixbar) results in test pattern. For a given annular illuminator a set of basic SRAF insertion rules is derived from process window analysis in test pattern. A medium size random logic interconnect layout (square and rectangular contact shapes) is used for SRAF recipe testing and process window analysis. The new SRAF insertion flow increases the common process window by 75% and reduces maximum MEEF from 8 to 5 when comparing to the tractional SRAF insertion flow. The rule based SRAF seed generation completes in ∼3.5% of the model based OPC (nmOPC) runtime over a full chip layout in a distributed cpu cluster. An analysis of DOF and MEEF is presented to compare process window for both SRAF insertion flows. The new SRAF insertion flow requires setting up a more complex nmSRAF insertion recipe which also requires more time for testing and debugging before tape out. During the early stage of process development, frequent changes of the illuminator would require changes to the SRAF recipe which may not be practical, however, in the stage of a more mature process closer to production, the new flow provides significant improvements in terms of performance and consistency of the resulting mask.

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