SAMPLE PLAN CREATION AND FULL CHIP COVERAGE FOR OPTICAL PROXIMITY CORRECTION MODELS

By

Mohammad Kamel Abdelfattah Kamel Moawad

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
ELECTRONICS AND COMMUNICATIONS ENGINEERING

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
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Key Words:
Photolithography; Resolution Enhancement techniques; Optical Proximity Correction; Modeling; Simulation

Summary:

Photolithography is used in integrated circuit manufacturing. Feature reduction challenge requires resolution enhancement techniques with the limitations imposed on the wavelength used. Optical proximity correction is one of the resolution enhancement techniques. Optical proximity correction requires predictive process models. In this study, a new methodology is introduced for the sample plan creation based on full chip image parameter coverage analysis. The generated sample plan aims to provide more predictive photoresist models for the lithography process.

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Dedication

To Kamel & Hoda

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Abstract

The semiconductor industry is driven by the need to place more devices onto a single chip providing faster processors and larger memories. Every step in the integrated circuit fabrication process needs to be optimized and enhanced to meet the market demand and to achieve a sustainable profit. Lithography became a crucial process that has seen tremendous enhancements during the past 30 years. For advanced technology nodes (32nm and below) the cost of manufacturing increased. Achieving a higher yield became a challenge for manufacturers. The fabrication process simulation tools reduce the cost allowing a large amount of trials to optimize the yield. The aim of this study is to develop a new methodology for the generation of accurate process models (optical and photoresist models) for lithography process simulations. Process models are used for optical proximity correction (OPC) which is required for the mask making. Accurate mask patterns help to reduce the manufacturing cost and avoid unpredicted failures. Accurate process models help predicting hotspots during the early full chip design through litho-friendly simulations utilizing process models.

This study is conducted with an understanding of the lithography process steps starting with a plain silicon substrate until the pattern is etched into the silicon. Firstly, the final resist image relationship to the aerial image parameters is identified. Second, the dependency of resolution enhancement techniques on process models is studied. Finally, the use of image parameters as a qualifier for enhancing the model coverage is examined based on an industrial quality models. The image parameters are evaluated for the full chip layout. Test patterns mask is created to cover the full chip layout image parameter space. Sample plan test structures are selected based on the closeness of the test patterns image parameter to the full chip image parameter in a 4D space. Then the full chip sample plan is compared to heuristic sample plan by calibration and verification of two resist models based on the two sample plans.

The outcome of this study is the introduction of image parameter based sample plan creation to provide an accurate/predictive process models for optical proximity correction and other resolution enhancement techniques, moreover reduce the risk

of unexpected model failures due to model predictability. The new methodology is integrated in the modelling development cycle and a modified flow with recommendations of the sample plan generation and sampling process is introduced. The new model building flow can be fully automated.

Chapter 1

Introduction

1.1 Motivation

Semiconductor manufacturing is the backbone of the integrated circuits industry. The strive to achieve faster circuits with bigger memory is a market demand and industry booster making the semiconductor manufacturers try to meet the demand. More and more devices are crammed on a single chip maintaining smaller devices to achieve the optimum cost. The semiconductor industry maintained almost a constant feature reduction roughly every two years [5].

The semiconductor manufacturing is a chain of many process modules. Across the history of the industry many processes have been introduced. And for each process many steps were introduced or enhanced. Feature reduction on wafer as well as achieving higher yield are the primary motivators for the manufacturing processes modifications. Among the new processes are Design For Manufacturing (DFM) flows that help to increase the yield and mask splitting for multiple patterning to enable further feature reductions. Figure 1.1 shows a simplified representation of semiconductor manufacturing process for new technology nodes.

With the feature reduction and the stringiest requirement to achieve higher yield the development cycle of a technology node becomes a complex and high cost process. Many fabrication facilities are not able to go in the continuous quest for feature reduction due to high cost of the development process and stop the development at certain technology nodes.

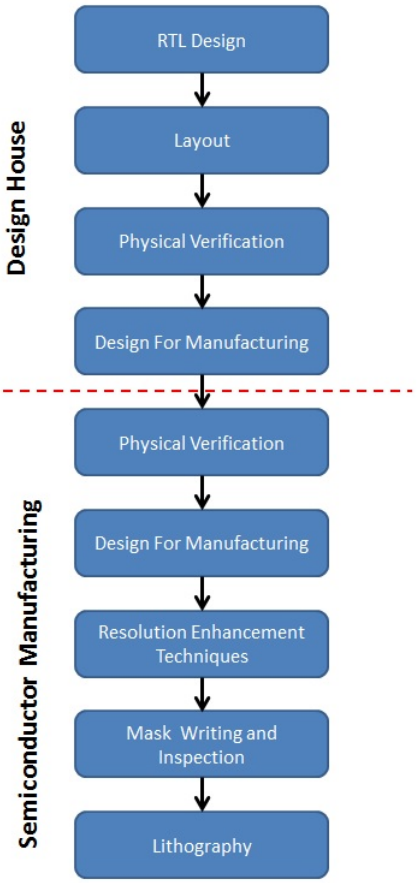

Figure 1.1: Design to Silicon Flow

Electronic Design Automation (EDA) helps providing accurate simulation for the process to simulate almost each step in the fabrication before manufacturing. Accurate simulation of each step avoids additional cost of new steps in the flow. Lithography is one of the processes that the EDA industry invested to reduce the development cost of technology nodes. Cost optimization is achieved by reducing the experimental on the wafer, hence, effectively use the masks and exposure scanner without wasting too many wafers. The lithography process uses a light source to from a photographic image that will be translated to a photosensitive polymer known as a photoresist to from a 3D image on the substrate. This process is commonly known as photo lithography or optical lithography. Optical lithography aims to have a photoresist image that has the exact shape of the required pattern in the substrate plane. The final photoresist profile is binary after development, such that some parts are totally covered with the resist and other locations are totally resist

free with no residual resist left behind. The uncovered locations mark the locations where the substrate will be etched or implanted.

The lithography impacts the electrical performance. Critical dimension (CD) control is one of the metrics of the lithography process that is directly related to the electrical performance of the fabricated integrated circuit. Critical dimension shrinks down to get faster transistors, the signal propagates through the transistors of a chip to perform an operation, there are several paths that operate in parallel to perform a certain operation. At each clock cycle the transistors perform a certain operation that is passed to other transistors, the overall speed is limited by the slowest transistor (transistor with the largest gate) in the critical path. Variations in the critical dimension are inevitable, if these variations are high, they may deviate the electrical characteristics required by the designer.

The lithography impacts yield. With the increase of the chip density and the reduction of the features dimensions, complex geometries started to appear in the designs. Complex geometries may not be printed on the wafer with good fidelity across all the process variations, therefore, these complex geometries will be flagged as hotspots. Hotspots may impact the final yield, if the exposure conditions went off the nominal conditions. The impact on the yield may take the form of non-functional chip or degraded performance of the chip. Many iterations are made to minimize the risk of reduced yield due to process variations. Rules are set to forbid some design geometries in advanced technology nodes to ensure the manufacturability of the designs.

Due to the high impact of the lithography process on the yield, the EDA industry invested in providing accurate process models, which predicts the resist and the optical system. Failure of the process models simulation have a great impact on the cost, electrical performance, and yield of a certain process.

This thesis provides a methodology to improve the prediction of the models used for simulation of the lithography process. Firstly, an understanding of the image transfer from a mask to a wafer is required. The feature reduction is maintained

according to Moore's law by adopting Resolution Enhancement Techniques (RET) such as Optical Proximity Correction (OPC) which provides final mask shapes and depends on the process model accuracy.

1.2 Thesis Structure

Chapter 2 explains the lithography process. An overview of the patterning processes is provided. A simplified case of exposure is used to understand the image formation. The final image in air is simplified to be based on Fourier optics. Finally, the formed image in resist is explained.

Chapter 3 describes resolution enhancement techniques (RET) such as Optical Proximity Correction (OPC) and Sub-Resolution Assist Features (SRAF). A simple example is used to explain the OPC and SRAF implementation nowadays. The predictive power of the process models is limited and has severe impact on the resolution enhancement techniques. This problem is explained in chapter 3 as well.

Chapter 4 introduces a new methodology of sample plan creation based on image parameter analysis of full chip. Definition of the image parameter domain of post optical proximity correction is performed. A test pattern mask creation process is developed with thousands of structures that cover the image parameter domain of the full chip mask. A new sample plan creation method reduces the number of required wafer measurements to an affordable level. The selection criteria is based on the test patterns image parameter closeness to the actual design post optical proximity correction using the simplified heuristics optical model.

Chapter 5 compares the new method to other method used to generate a sample plan. A discussion closes each section in this chapter.

Chapter 6 provides a summary of this thesis.

Chapter 2

Lithography and Image Formation

2.1 Introduction

This chapter gives a brief overview over the integrated circuit fabrication process and the lithography process steps. This chapter is divided into 3 main sections, Section 1 describes the main three patterning processes that are used to stack the functional materials to generate a functional transistor. In section 2 an overview of the lithography process is introduced where the details of the patterning process is discussed. In section 3 the image formation is described together with the image propagation from the mask to the wafer and how the photoresist reacts with the incident wave to form the final image in the resist.

2.2 Integrated Circuit Fabrication

Integrated circuits are a group of 3D electrical devices stacked on a semiconductor wafer, typically silicon. Electrical devices are interconnected with conductors and insulators in order to perform a desired electrical function.

Silicon has physical characteristics between insulators and conductors. Silicon conductivity is altered by heat, light, impurity doping or by applying an electrical field. Electrical fields and impurity doping are the core basis of transistors formation.

Complementary Metal Oxide Semiconductor (CMOS) is a fundamental transistor for the digital electronics. CMOS process requires to have n-channel (NMOS) and p-channel (PMOS) transistors built on the same wafer. Impurities doping helps in the generation of both transistors on the same wafer, the PMOS transistor has to be built in an n-well or on a n-type substrate and an NMOS transistor has to be built in a p-well or a p-type substrate. Wells are formed by the semiconductor doping process as shown in Figure 2.1.

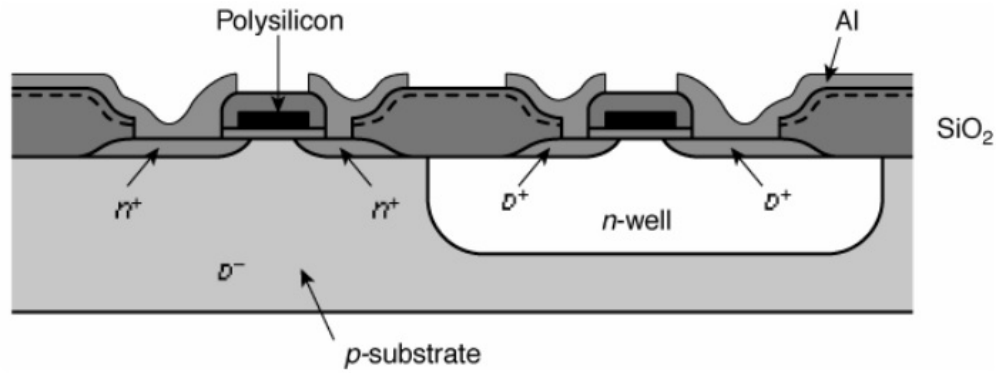

Figure 2.1: Cross Section of n-well CMOS Process

2.2.1 Patterning Process

A CMOS fabrication process is an iterative process for stacking the layers over each other. Stacking a layer is done through a sequence of basic operations. These basic operations are done repetitively in the process of manufacturing as patterning, etching, and selective doping. These operations could be done as many times as required to fulfil the circuit connectivity to build up a functional IC.

Patterning, etching, and semiconductor doping are the main three processes that involve the basic CMOS manufacturing process. The control of the sequence of these three patterning process enables the generation of a functional transistor as shown in Figure 2.1.

2.3 Lithography Process Basics

Lithography marks the locations where the deposition, selective doping, or etching will be taking place. Lithography is the process of planographic printing from a metal or stone surface; Lithography comes from the Greek lithos, meaning stones, and graphia, meaning to write. This literally means writing over the stone. Semiconductor industry utilize the lithography to form the desired patterns on the wafer where the stone is the silicon.

Optical lithography is used to achieve the control of the patterning process. Optical lithography transfers a pattern from mask to a light sensitive polymer known as photoresist forming a 3D image intensity profile on the wafer. The ideal photoresist image has the exact shape of the patterns on the mask with a 90 degree vertical walls across the resist thickness. After developing the final resist pattern is expected to be binary where the parts of the substrate is covered by the substrate whereas other locations are uncovered to be operated on by etching, or doping.

Optical lithography is a sequence of processes to transfer the pattern from the mask to the substrate that are performed in the following order: substrate preparation, photoresist spin coat, post-apply bake, exposure, post exposure bake, development and post bake and finally metrology and inspection to detect the final resist profile is meeting the acceptance criteria. Then finally resist striping. The lithography sequence is shown in Figure 2.2. In the next section we will explain each step in details.

2.3.1 Substrate Preparation

Substrate preparation is intended to enhance the adhesives of the photoresist to the substrate and reduce the process contamination in the process since the resist typically do not adhere to untreated silicon surfaces [6]. This process is done in mainly three steps:

- Cleaning of the substrate and particle removal
- Dehydration bake to remove water

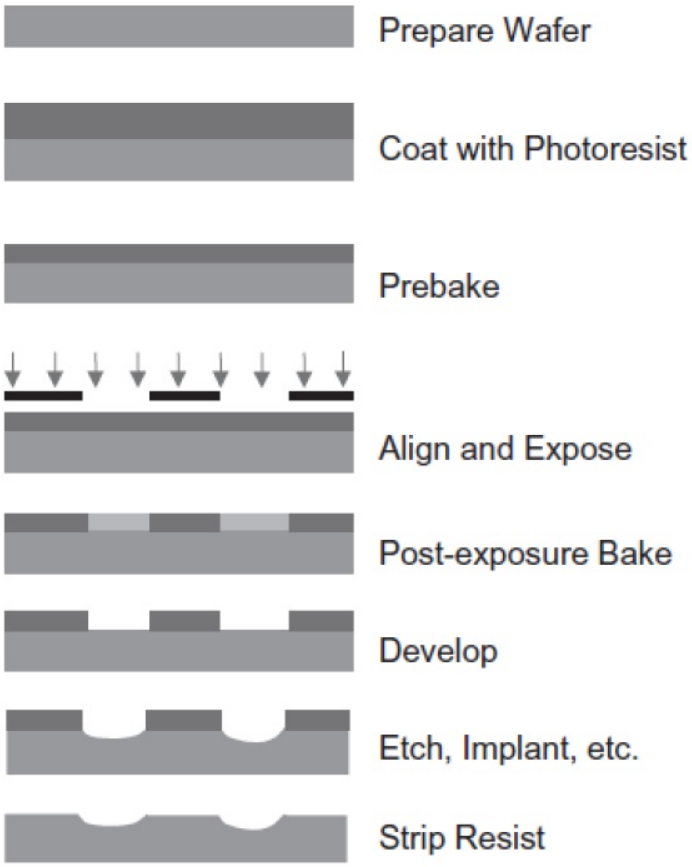

Figure 2.2: Lithography process sequence [1]

- Addition of adhesion promoter

Cleaning of the substrate and particle removal, Particles usually result from airborne or contaminated liquids like the adhesion promoter. Cleaning the particles is done through chemical and mechanical cleaning. Organic films such as remaining left over polymers from various processes and inorganic films such as native oxides or salts are removed through chemical, or plasma stripping.

Dehydration bake to remove the water, the main reason for the water absorption usually the substrate undergo high temperature processing such as thermal oxidation where the Silicon is being oxidized if the substrate is being left to dry in humid environment the water will be absorbed. Dehydration bake at temperature of 200 to 400 Celsius for about 60 minutes can remove the water from the surface, however, if silanol is formed at the surface due to the bonding between the silicon forming the silanol group (SiOH), this layer can be removed by dehydration bake

of temperature exceeding 600 Celsius to remove this layer or by chemical processing.

Finally, addition of adhesion promoter to increase the photoresist adhesiveness, since the wafer surface can get oxidized very easily in humid environment forming a strong hydrogen bond with the water absorbed from the air, so if the resist is being spun on this surface, it will suffer from poor adhesion to the surface leading to failure in the development due to resist lift off or pattern collapse. It is very beneficial to add adhesion promoters to react with the silanol surface and replace it with an organic function group that prevent the re-absorption of the water in the surface [7].

2.3.2 Photoresist Coating

A uniform photoresist layer is spun on with a tight thickness control of 1-2 nm across the wafer and wafer-to-wafer, to be ready for the resist processing. The photoresist is transformed into liquid form by dissolving the solid component into a solvent, then poured onto the wafer which is then spun on a turntable at high speed to spread the resist across the wafer where the centrifugal forces push the photoresist on the wafer towards the edges of the wafer such that excessive resist are flung off the wafer. The centrifugal force decreases as photoresist film gets thinner and due to the evaporation of the solvent in the resist the viscosity of the photoresist increases dominating the forces acting on the photoresist this stage is known as the coating stage, this usually occurs at the first few seconds in the spinning and the remaining spin cycles cause the evaporation of the solvent with no flow of the resist across the wafer surface which is known as the drying stage [8].

The photoresist film thickness is inversely proportional to the spin speed and proportional to the liquid viscosity, however other parameters controls the final film thickness that need to be also considered such as the choice of static and dynamic dispensing, spin acceleration, volume of the resist dispensed, also the conditions at which the dispensation process take place plays an important role on the final photoresist thickness such as the humidity, and resist temperature.

The photoresist coating is a tightly controlled process as the deviation on the

uniformity of the resist on the wafer may induce defects at later stages on the lithography process producing unexpected line widths and spaces.

2.3.3 Post-apply Bake

Post-Apply bake evaporates the solvent in the resist to stablize the film at room temperature. This evaporation process changes the resist characteristics. Post-Apply bake changes the film thickness, development characteristics, and enhances the adhesion film to the substrate.

2.3.4 Alignment and Exposure

Before exposure alignment of the image, generated by the previous mask, with the previously placed patterns on the wafer is done. As the main objective to print smaller critical feature, alignment and the resulting overlay of the two or more lithographic patterns is required to be done with fine control. Any misalignment of the mask image with the previously placed patterns may lead to catastrophic failures on the chip functionality. Wafer leveling is done with the alignment process at several fields. Wafer leveling is done to ensure that the exposure field is at the proper focus.

Exposure is the change in the solubility of the photoresist in developer due to exposure to the light transferring the patterns on the mask to the photoresist. In other words building an image in the resist that corresponds to the aerial image of the patterns on the mask which is known as latent image. Photoresist undergoes chemical reactions by light exposure changing the dissolution rate as a function of the exposure energy, such that the difference in the dissolution between the exposed and unexposed locations makes the development stage selectively removes one of them depending on the type of the resist. There are two types of photoresists, positive photoresists and negative photoresist, where the exposed regions in positive photoresist dissolves during the development, whereas for the negative photoresist unexposed regions dissolves during the development. The left over photoresist acts as a protective film during ion implantation and etching processes.

Projection printing projects the image of the mask to the wafer. projection printing is used nowadays compared to contact and proximity printing. Projection printing is done using what is known as scanners. Scanners used the g-line (436nm), i-line (365nm), KrF excimer lasers (DUV) 248 nm, and finally ArF excimer laser at 193 nm to expose the wafers for the most advanced technology nodes in the industry.

Photoresists for g-line (436nm) and i-line (365nm) basically consists of Novolak resin, diazonaphthoquinone (DNQ), and solvent. Photoresists typically respond to specific wavelength. Novolak resin a binder that provides mechanical properties. Novolak is soluble in base solution in water and can comprise the developers of DNQ resists. Solvent is used to dissolve the resin, allowing the resin to be applied in a liquid state. DNQ is insoluble material in novolak resin solutions but when the DNQ is mixed with novolak resin the resulting mixture dissolves at extremely slow rates in basic solutions. when the DNQ is exposed to light energy it is turned into acid that is soluble in basic solutions of the developer. This is the basic operation of the photoresist.

DNQ resist type of suffered from technical limitation with KrF excimer lasers (DUV) 248 nm as this type of lasers is weaker than g-line and i-line. DUV resists needed to be more light sensitive compare to DNQ resists. Also DNQ has a high optical absorption which makes it difficult for the light to reach the bottom of the resist hence the space may not be developed. Chemically amplified resist was invented [9] [10]. Chemically amplified resist (CAR) was invented to have higher light sensitivity hence enables higer wafer throughput and resolve the high optical absorption of the DNQ resists. Chemically amplified resist performs similar to conventional resist when exposed to the DUV however the solubility of the resist do not change sufficiently to be developed, another reaction is done during the post exposure back that is catalyzed by the photoacid generator (PAG) resulting in a change in the resist solubility.

As the light waves travel down in the photoresist and with a reflective substrate, the waves are reflected back forming a standing wave in the resist. High and low intensity are formed along the depth of the photoresist forming ridges in the sidewalls

of the formed patterns as shown in the Figure 2.3, as the feature size shrinks and gets comparable to the wavelength the ridges performs a negative impact on the feature fidelity. Standing wave effect is reduced by adding Bottom Anti-reflective coating (BARC) reducing the reflectivity of the substrate.

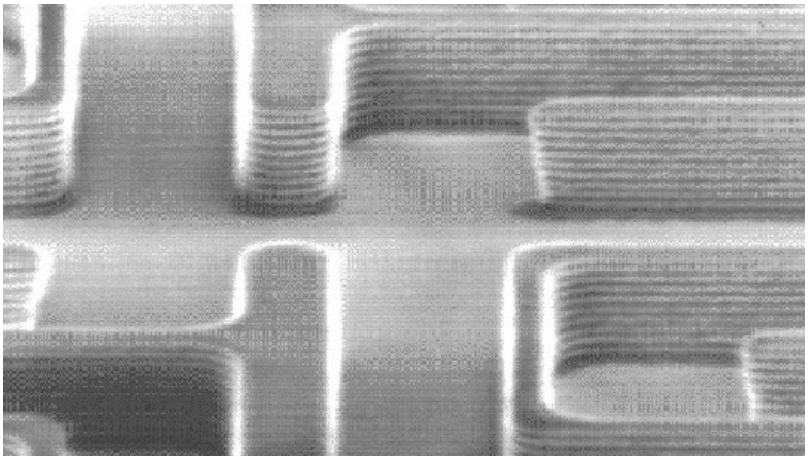

Figure 2.3: Standing waves effect in the photoresist [1]

2.3.5 Post-exposure Bake

Post-exposure bake is the application of high temperature to the wafer after exposure aiming to reduce the standing wave. PEB leads to the diffusion of the PAC hence smoothing the standing wave ridges and improving the line width control [2] as shown in Figure 2.4. For CAR PEB is an mandatory step to complete the exposure process where the PAG catalyzes the reaction changing the solubility of the exposed regions defining the exposed patterns. PEB for the CAR is very critical and requires a fine control.

2.3.6 Resist Development

Development forms the pattern on the wafer which will serve as the protective film covering areas on the wafer that need to be protected from chemical attack during etching, implantation, in other words carving the latent image in the resist to produce the final resist image.

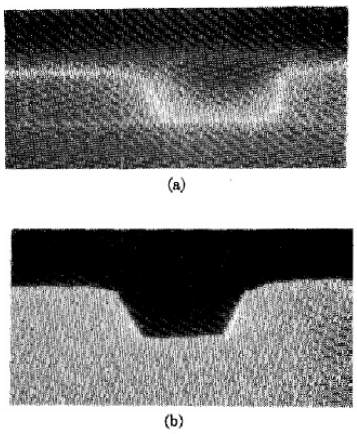

Figure 2.4: SEM photography showing influence of post-exposure bake on residual standing-wave ridges in AZ-1350J resist. [2]

Development is done by applying an aqueous base solutions (developers) to the photoresist. In the past development was done in batch of 10 - 20 wafers immersed into developer tanks. The process has been replaced with single wafer development as it has improved uniformity and control. Among the major techniques used for development is spin development spray development and finally puddle development. The most common method is the puddle development [11]. Resist development is critical as it defines the final resist uniformity and the linewidth control.

2.3.7 Postbake

Postbake is exposure of the resist to high temperature (120 °C, 150 °C). When the resist exposed to high temperature the resin polymer in the photo resist will cross link and hence making the image more thermally stable.

Postbake aims to harden the resist to undergo the harsh environment of the implantation or etching processes. Also it helps to remove the residual solvent, water or gasses in the resist and improve the adhesion of the resist to the substrate.

2.3.8 Measure and Inspect

Wafer inspection could be done before and after postbake. Inspection is done to some sample of the resist patterns to ensure the pattern quality. Inspection aims

to inspect the critical features to measure their dimension and the overlay of the patterns with respect to the previous layers. There are two types of inspection after development inspection (ADI) and final inspection (FI).

ADI is a process that may help in avoiding defects. ADI helps in detecting wafers that are not meeting the required CD or does not meet the overlay specifications. These wafers are reworked by stripping off the resist and return to the start of the lithography process. On the other hand at the FI if the wafer does not meet the specification, this wafer will be discarded as it can not be reworked.

2.3.9 Pattern Transfer

Patterns are lithographed onto the photoresist. Those patterns need to be transferred to the substrate. Patterning takes one of the three forms, etching, selective deposition, and selective doping.

2.3.9.1 Deposition

Deposition adds new layer to the substrate. The lithography patterns opens where the new layer will be added. Then the resist is removed and the new layer is deposited on the substrate such as the copper layer uses electroplating.

2.3.9.2 Selective Doping

Selective Doping is the process of changing the dopant concentration for some parts of the material after patterning step. Locations on the wafer that are uncovered by the photoresist receives the dopant impurity.

Dopant type are either p-type dopants or n-type dopants. Doping changes the electrical characteristics of the silicon, hence, the required voltage to turn on and off the transistors. Doping techniques includes diffusion implantation or Ion implantation. Doping is done for selective locations on the wafer such as source and

drain formation.

2.3.9.3 Etching

Etching is the process of selective removal of the deposited material. There are two techniques used wet etching and dry etching. Wet etching is the process of applying an acid or base solution depending on the target material. Wet etching is an isotropic process that may lead to cutting other location under the protection layer. Dry or plasma etching is an anisotropic etching where an ionized gas, plasma is used to etch the target material.

2.3.10 Resist Strip

Resist stripping is the total removal of the remaining photoresist from the wafer. There are two methods of the photoresist stripping: wet stripping and dry stripping. This process is getting more critical in advanced technology nodes where ultra-shallow junctions, 3D structures, double pattering are used. Resist stripping in advanced nodes are getting more to be an interacting process with the underneath layers removal, Also poor removal of the residual has lower throughput and alters junction/dopant characteristics causing defects [12].

2.4 Basic Physics of Optical Lithography

In the previous section, we have gone through the basic pattern transfer process from the mask to the wafer. As seen above the pattern transfer process is a complex process.

The exposure process is explained in this section. The exposure process is the change in the solubility of the photoresist due to exposure to the light transferring the patterns on the mask to the photoresist, therefore optical knowledge is required to understand how the light propagates from the illumination source through the

mask to the wafer. Also chemical knowledge is required to understand the chemical reaction that is triggered in the photoresist due to the exposure to the light. The understanding of the exposure process helps in understanding the limitation of the lithography system and the enhancements that improve the optical resolution.

2.4.1 Basic Imaging Theory

Considering a basic projection imaging system shown in Figure 2.5. This system represents the basic concept of a lithography system which consists of: the light source and the condenser lens represent the illumination system that is responsible to deliver light to the mask with the required specifications (uniformity, spectral characteristics). The delivered light passes through the transparent parts from the mask to the objective lens. The objective lens is responsible of collecting the light passed through the mask and project it onto the wafer.

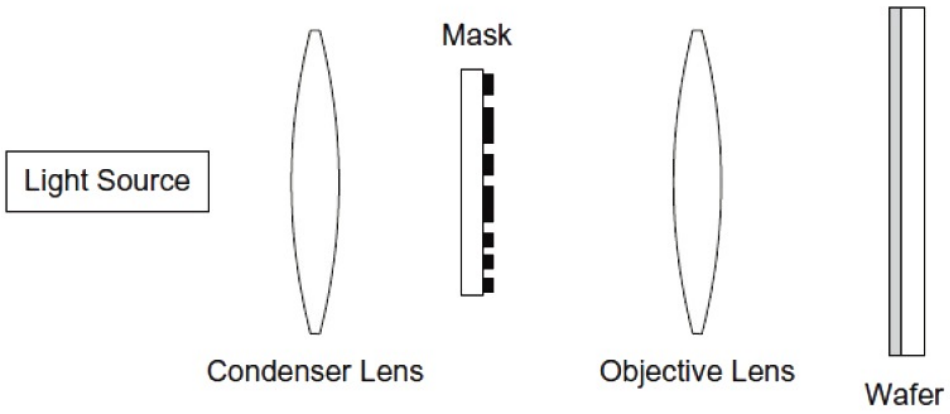

Figure 2.5: Generic Projection Imaging System

2.4.1.1 Diffraction

As the desired final feature size gets smaller compared to the light source wavelength light diffraction occurs. Several approaches were used to calculate the image after the mask due to diffraction. The most accurate method in classical optics is Maxwell's equations. Maxwell's equations describe how an electromagnetic wave propagates and this will result in complex partial differential equations for a general

boundary conditions. These equations requires super computers to evaluate.

Light is an electromagnetic wave. Assuming a homogeneous isotropic medium with a constant refractive index, light can be treated as a scalar quantity. Scalar diffraction theory could be used in optical systems which takes the form of numerical integration to describe the light wave. This theory was used by Kirchoff in 1882. Assuming the slit is the mask and the diffraction plane is the objective lens of the system described in Figure 2.5. This theory was further simplified by Fresnel when the distance from the mask to objective lens is greater than the wavelength. At the end, when the distance to the objective lens is very far from the mask Fresnel diffraction turns into Fraunhofer diffraction. This is known as far field diffraction as shown in Figure 2.6.

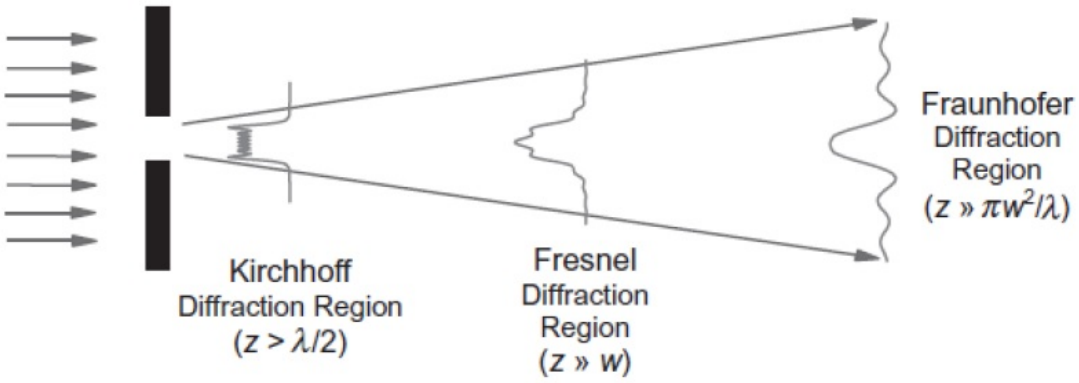

Figure 2.6: Comparison of the diffraction regions where various approximations are accurate. Diffraction is for an aperture with width w illuminated by light of wavelength λ, and z is the distance from the mask [1].

Without going through the mathematical derivation of the approximation, the Reader may refer to Book [13] chapters from 2 to 4 for the mathematical derivation of Fraunhofer diffraction integral. Assuming a simple chrome binary mask with the t_m(x,y) defined as the electric field transmittance of the mask for a normally incident plane wave $E_i(x, y)$ under Kirchohoff boundary condition such that t_m(x,y) is 1 under the glass and 0 under the chrome. The plane of diffraction x'-y' is the entrance of the objective lens, and z is the distance from the mask to the objective

lens assuming a monochromatic light source of wavelength λ and the entire medium is homogeneous with a constant refractive index n. Defining the spatial frequency of the diffraction patterns as $f_x = nx'/(z\lambda)$ and $f_y = ny'/(z\lambda)$, the electric field of the diffracted pattern is given by Fraunhofer diffraction integral,

$$T_m(f_x, f_y) = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} E_i(x, y) t_m(x, y) e^{-2i\pi(f_x x + f_y y)} \, dx \, dy \tag{2.1}$$

Equation 2.1 looks like the Fourier transform and the base of Fourier optics. Equation 2.1 defines the electric field distribution at the entrance of the objective lens. Hence the diffraction pattern is just the Fourier transform of the mask pattern transmittance.

2.4.1.2 Diffracted Image Reconstruction

The image is defined at the objective lens using inverse Fourier Transform. First we will define the nature of the generated wave at the entrance of the objective lens, then we will see the effect added by the objective lens to the image reconstruction.

Assuming an equal line-space mask infinitely long in the y direction with a pitch p and feature width w illuminated by a uniform normally incident plane wave. The mask transmittance resembles periodic square wave as shown in Figure 2.7. The resulting Fourier transform is a set of discrete diffraction orders. Reader may refer to Book [14] for the mathematical analysis of Fourier transforms.

Looking over the diffraction patterns in Figure 2.7 it consists of zero order which is the highest component in magnitude located at the center of the objective lens. Beside the zero order the first two frequency components occurring at $\pm 1/p$ these are known as the first order components. The first order components location carries the pitch information, and the next frequency component occurs at $\pm j/p$. Ideally to fully reconstruct the mask patterns all the frequency components should be captured by the objective lens.

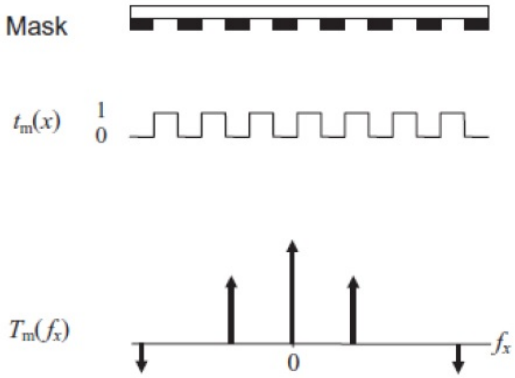

Figure 2.7: Array of equal lines and spaces and the resulting Fraunhofer diffraction patterns when illuminated by a normally incident plane wave [1].

The Objective lens being of finite size hinders the full image reconstruction. Therefore at least the first order components should be captured by the objective lens in-addition to the zero's order to resolve the mask patterns. In other words the objective lens has to be wide enough to capture the zero and the first order components. The wideness of the lens is a feature that controls the minimum pitch that could be captured by the system. The wideness of the lens aperture could be defined by the lens radius since lenses used in microlithography are circular lenses, therefore a more common definition is the maximum angle at which the diffracted light can enter the objective lens as shown in Figure 2.8.

The Numerical aperture is defined as the sine of half-angle of the diffracted light that can enter the lens multiplied by the refractive index of the surrounding medium n.

$$\text{NA} = \text{n } \sin(\theta_{max})$$

referring to Equation 2.1, the spatial frequencies are defined in both x and y direction, which may be expressed in terms of the angle of diffraction,

$$f_x = nx'/(z\lambda) = n\sin(\theta_x)/\lambda \tag{2.2}$$

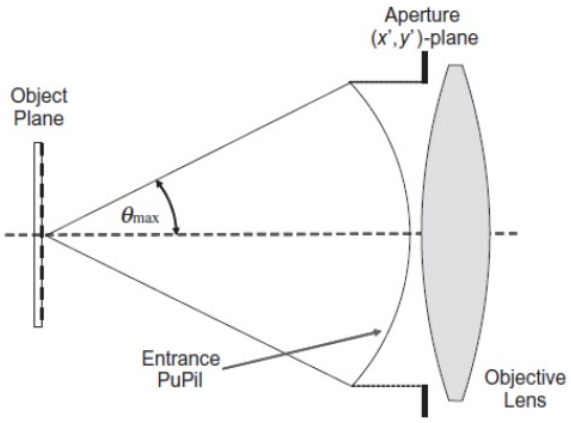

Figure 2.8: Numerical Aperture defined as NA = n $\sin(\theta_{max})$, where the θ_{max} is maximum half-angle of the diffracted light that can eneter the objective lens, and n is the refractive index of the medium between the mask and the lens [1]

Using the numerical aperture definition, The maximum spatial frequency that can be collected by the objective lens is given by,

$$f_{max_x} = NA/\lambda \tag{2.3}$$

Since the location of the first diffraction order in the frequency domain occurs at the $\pm 1/p$ then the objective lens should be able to capture this order of frequency to reconstruct the image. This puts a lower limit on the minimum resolvable pitch that can be imaged by this system. The smallest pitch that could be captured by this system is given by,

$$1/p_{min} = NA/\lambda \tag{2.4}$$

If we defined the resolution as the minimum resolvable (linewidth or spacewidth) for our assumed equal line/space pitch, the theoretical resolution is given by,

$$TheoreticalResolution = 0.5\lambda/NA \tag{2.5}$$

Ideally the objective lens is designed to act as an inverse Fourier transform of the diffracted patterns. If the objective lens of infinite size, the mask patterns is fully

reconstructed at the wafer surface. However due to the fact that the objective lens is of finite size, objective lens does not collect all the diffracted orders of the mask. it collects only the diffracted orders that are within the numerical aperture limit. The quality of the reconstructed image at the wafer is a function of the collected diffraction orders by the objective lens. This formed image at the wafer surface is known as the aerial image.

2.4.1.3 Latent Image

In the previous section we described the generated image at the surface of the wafer. The diffracted plane waves interferes at the surface of the resist forming the aerial image. The aerial image propagates inside the photoresist material. Reflection and refraction of the waves occur due to the medium difference from air to resist forming standing waves.

Continuing with the equal line space pitch p on the mask, illuminated with a coherent light source with wavelength λ. Assuming that the objective lens is able to capture the zero order and the first order of the diffracted waves. The first order components occurs at angles,

$$n\sin(\theta) = \pm\frac{\lambda}{p} \tag{2.6}$$

The aerial final image is formed by the interference of three components, DC term with magnitude a_0, and the first order components. The resulting aerial image electric field will be,

$$E(x,z) = a_0 e^{ikz} + a_1 e^{ikx\sin\theta} e^{ikz\cos\theta} + a_1 e^{-ikx\sin\theta} e^{ikz\cos\theta} \tag{2.7}$$

The previous equation could be simplified to be,

$$E(x,z) = e^{ikz}(a_0 + 2a_1\cos(2\pi x/p)e^{-ikz(1-\cos\theta)}) \tag{2.8}$$

The aerial image undergoes reflection and refraction due to the propagation from one medium to another. By the same procedure as above in the presence of a reflecting substrate the electric field is modified and taking into account the air-resist interface and the multiple reflection that can take place inside the resist. The diffraction order magnitude will be changed to be to the effective amplitudes in the resist a_{0r} and a_{1r}.

$$E(x,z) = e^{ikz}(a_{0r}[1+\rho(0)]e^{-ik2z} + 2a_{1r}\cos(2\pi x/p)[1+\rho(\theta)e^{-i2kz\cos\theta}]e^{-ikz(1-\cos\theta)}) \tag{2.9}$$

such that $\rho(\theta)$ is reflection coefficient as a function of the θ which is the angle in the resist. Equation 2.9 is interpreted as the interference between the plane waves causes variation in the electric field in the x-direction defining the image and the z direction defining the standing wave and the image defocus in the resist.

As a simplification, Equation 2.9 is written as function of the standing wave in the resist,

$$E_{sw}(\theta,z) = e^{ikz\cos\theta} + \rho(\theta)e^{-ikz\cos\theta} \tag{2.10}$$

$$E(x,z) = a_{0r}E_{sw}(0,z) + 2a_{1r}E_{sw}(\theta,z)\cos(2\pi x/p) \tag{2.11}$$

The resulting electric field in the resist is different from the electric field in air due the propagation in an absorbing and reflecting medium. The final intensity inside the resist is a function of the initial exposure electric field, reflection occurring in the resist, and finally the absorption of the taking place by the resist.

Photoresist material is a light sensitive material as discussed in Section 2.3.4. Photoresist DNQ molecules characteristics changes by absorption of light. The understanding of the resist changes due to exposure is guided by 2 main effects the rate of absorption of the energy by the resist and the rate of change of the photoresist material due to the absorbed energy.

The change in the intensity of light in the resist as it propagates in the resist is given by Lambert's law of absorption,

$$\frac{\mathrm{d}I}{\mathrm{d}z} = -\alpha I \tag{2.12}$$

where the z is the direction of the light propagation, and α is the absorption coefficient.

Dill's Equation is used to describe the exposure kinetics of the photoresist such that,

$$\frac{\mathrm{d}m}{\mathrm{d}t} = -CIm \tag{2.13}$$

where m is the relative concentration of the photosensitive material, C is the exposure rate constant, and t is the exposure time.

Solving the two Equation 2.12 and 2.13 we get the initial transmittance of the resist at the start, the rate of change of transmittance, and the transmittance when fully exposed as explained in [15]. Now the resist is ready for the rest of the processing step discussed in Section 2.3 where the coming steps do slight change in the exposed resist to enchance the quality of the final resist image.

To sum up the final image in the resist after the complete processing is a function of the intensity of light in the resist. The light intensity in the resist is function of the initial incident wave on the resist after the objective lens. The understanding of how the image transfer from the mask to the wafer will help to get a better control of the final wafer image and have a better image predictability of what we will get on the wafer.

Chapter 3

Resolution Enhancement Techniques and Modelling

3.1 Introduction

In the previous chapter, The patterning process is described for patterning a wafer. A simple projection system is introduced for optically image formation. The resist interaction with the light during exposure is explained.

The lithography process is required for printing of smaller features and to ensure quality of mass production despite the process variability.

In this chapter, resolution enhancement techniques are introduced. The technology node development cycle is introduced. Finally we will spot the light over a bump that hinders the accuracy of implementing some of the reduction techniques.

3.2 Resolution Enhancement Techniques

3.2.1 Resolution

Resolution is defined in Equation 3.1. To derive this equation, an equal line and space pattern on mask is illuminated by a normally incident wave with monochromatic wavelength. The resolution limit is pattern dependent. A generalized form

of the resolution equation is given by,

$$Resolution = K_1\lambda/NA \tag{3.1}$$

where K_1 is a coefficient that depends on process-related factors. λ is the wavelength of the exposure source. NA is the numerical aperture of the objective lens.

Is the smallest pitch the minimum resolvable feature on wafer?. No, because there is another requirements that must be met to use the lithographic system for mass production. The feature resolution is limited by the ability to control the critical dimension (CD) of the feature within a process window. This control is required for mass manufacturing. Controlling the feature dimension on the wafer has an impact over the device electrical performance. Critical devices are designed to work over small range of feature sizes, therefore any deviation in the feature size may degrade the electrical device performance.

Process control is required to meet the designer specifications. Electrical performance degradation is detected by delays of the signal propagating through a chain of transistors which operates in parallel and interconnected with each other. At each clock cycle transistors are turned on or off. The fastest speed of the circuit is controlled by the slowest transistor with the largest CD in the signal path. Transistors which have a large gate length provided by a low driving current result in reliability issues. Transistors which have a small gate length increase the leakage current and induce power consumption problems. If the transistors gates are within the expected range of CDs, the better the circuit performance will be, the lesser timing problems will occur and power leakage problems will decrease, moreover the overall chip speed meets the designer specifications.

The International technology roadmap for Semiconductor (ITRS) defines the lithography technology requirements for the three basic types of devices: DRAM half-pitch (contacted), MPU/ASIC Metal half-pitch, and Flash half-pitch (uncontacted poly). The DRAM CD control is required to get smaller with the feature reduction [16]. With the continuous reduction of the feature size a tighter control

on the lithography process is required to be able to generate the smaller feature on wafer.

Year of Production	2011	2012	2013	2014	2015	2016	2017	2018
DRAM ½ pitch (nm) (contacted)	36	32	28	25	23	20.0	17.9	15.9
DRAM								
DRAM ½ pitch (nm)	36	32	28	25	23	20	18	16
CD control (3 sigma) (nm) [B]	3.7	3.3	2.9	2.6	2.3	2.1	1.9	1.7

Figure 3.1: Critical dimensions defining digital semiconductor circuits for the poly layer between 2011 to 2018 [3].

3.2.2 Resolution Enhancement Techniques

Several techniques have been introduced to achieve the reduction. Recalling the generalized resolution Equation 3.1, three parameters describe the reduction of the minimum printable features. Those three terms are NA, λ, and K_1 that are tuned to minimize the printable feature. Also tighter process control is required by reducing the process error.

The resolution is achieved by several ways. Mainly they are classified into two parts. Firstly the optics improvements. Secondly the process control improvements. Our focus is limited to optics improvements. Below is a list of resolution enhancements techniques,

Optics improvements

- Reducing the exposure wavelength
- Increasing the imaging lens numerical aperture
- k_1 reduction techniques

Process control improvements

- Increasing the process window size of the lithography process.
- Improving the control of dose and focus

3.2.2.1 Optics Improvement

Wavelength Reduction

Reducing the wavelength is the most powerful technique to enhance the resolution. Wavelength reduction is governed by the development of the exposure equipment and the photoresist materials that respond to the exposure wavelength, as shown in Figure 3.2, showing the relationship between the wavelength and the minimum integrated circuit feature.

An ArF excimer laser emitting 193nm is the most widely used light source for the nodes (90nm and below). Further wavelength reduction is challenging. The F_2 excimer laser emitting 157nm wavelength was on the roadmap. Since the limitations were too high to make it to the production environment it was dropped. Sufficient transparency to the 157nm with the fused silica as lens material was difficult to achieve. New lens material is introduced. CaF_2 was a good candidate but large scale lens with the required transparency was difficult to manufacture.

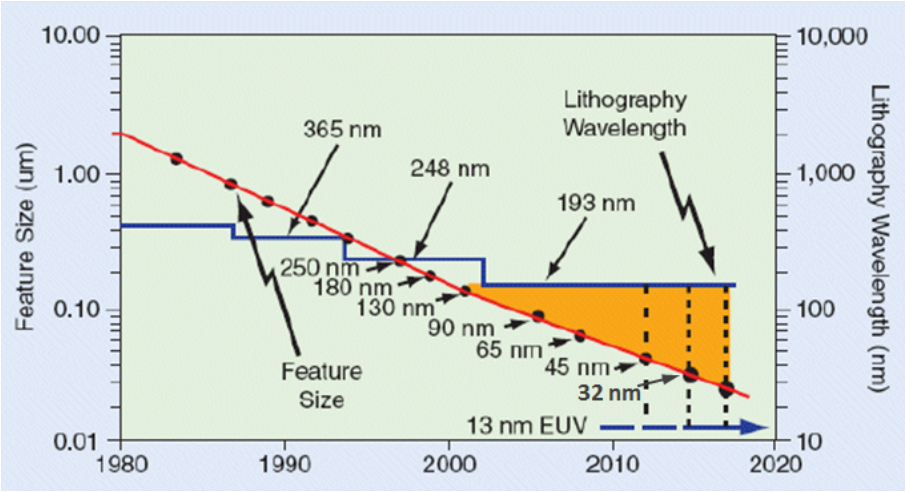

Figure 3.2: Wavelength in nm and the min. feature size versus time in years

Further wavelength reduction is not possible beyond the 193nm wavelength without dramatic change in the exposure system and the materials used. These changes are not cost effective and do not add value to the industry. Until now immersion lithography with 193nm is used in combination with other RETs methods. As shown in [17], the 193nm wavelength is still being considered as a possible source for the sub-10nm nodes using multiple patterning.

Numerical Aperture

Increasing the numerical aperture of the lens is achieved by having a wider lens or changing the surrounding medium refractive index. Wider lens enables the capture of a wider spectrum for imaging and hence resolves smaller features, but increasing the size of the lens faces two main challenges in the lens; Firstly, a wider lens are difficult to produce without lens aberrations and the assembly makes the lens expensive. Secondly, a larger NA reduces the depth of focus as shown in Figure 3.3.

Hence, there is an optimum numerical aperture that achieves a good feature resolution and process control. For a certain technology node, an NA optimization methodology has been introduced in [18], the optimum NA is not the highest available setting in the exposure tool, but is a function of the feature size, structure shape, wavelength.

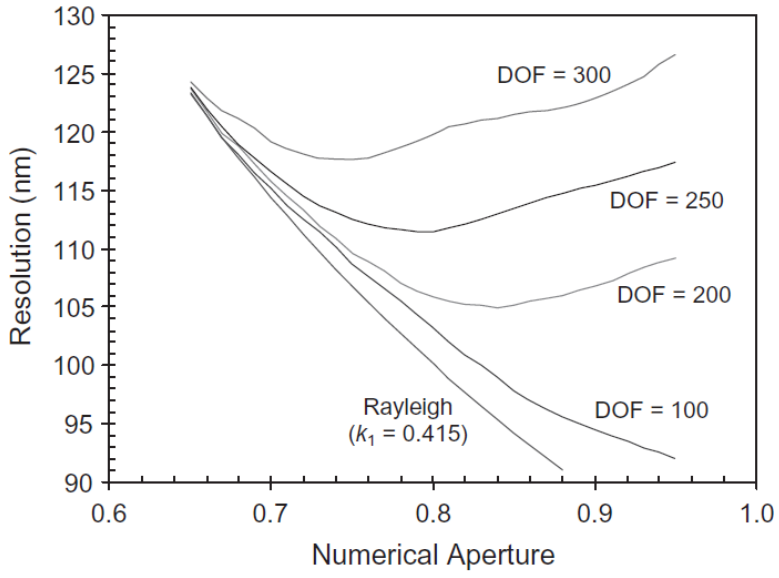

Figure 3.3: Resolution in nm as a function of the numerical aperture NA, $k_1 = 0.415$, $\lambda = 193$nm, equal line and spaces , DOF refers to the depth of focus. Depth of focus is defined as the range of focus that keeps the resist profile for a given feature within the specifications line width [1].

3.2.2.2 K_1 Reduction Techniques

There are several techniques to reduce the K_1. Generally all the K_1 reduction techniques aim to improve the process by improving the quality of the image in the resist. Among the most important resolution enhancement techniques is the Optical Proximity Correction (OPC) and insertion of Sub-Resolution Assist Features (SRAF).

- **Optical Proximity Correction**

In chapter 2 the final image is a partial reconstruction of the Fourier transformation mask image. The final image suffers from distortion during the reconstruction of the mask image. The examples of an isolated line and a dense line/space structure with the same CD is patterned into positive resist. The aerial image generated by the two structures is different. The difference in the aerial image is an effect of the optical proximity difference between the two patterns. This difference adds up with other non-idealities in the lithography system such as lens aberrations, resist processing after exposure and takes the form of completely distorted wafer image as shown in Figure 3.4. The difference between the printed linewidth needs to be compensated to meet the designers' required linewdith. To compensate for the differences between the mask shapes of different proximity and the printed CDs a correction is required. Modification of the originally designed mask structures such that the printing process imperfections are compensated to generate an image on silicon that look as close as possible to the original designed mask. This modification is known as optical proximity correction.

Typically large patterns have a similar diffraction patterns independent whether they are isolated lines or dense structures. As the feature size gets smaller the differences in the aerial image gets pronounced. The image diffraction patterns differences manifest a great degradation in the printed linewidth quality that requires OPC.

Across the history of the semiconductor industry several methods were introduced to compensate for proximity effects. The amount of complexity increases as the minimum feature size shrinks. The major two methods that were used are rule based OPC and model based OPC.

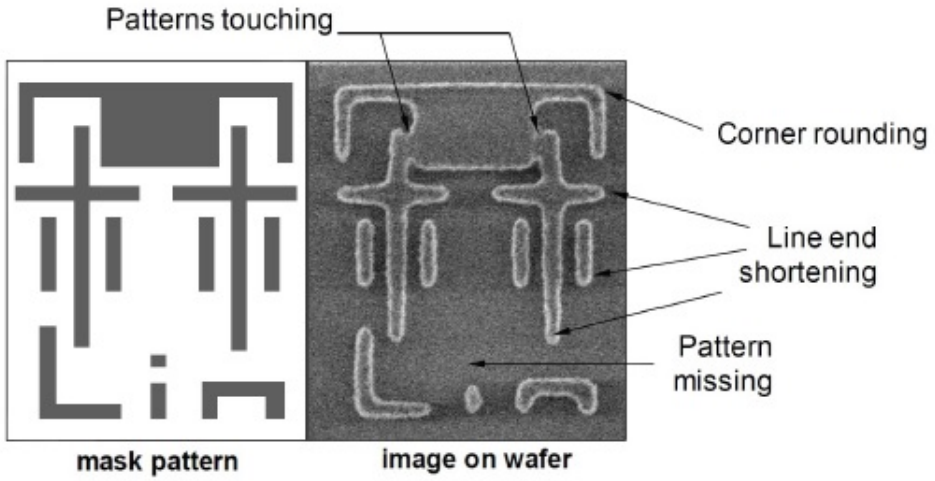

Figure 3.4: 2D and other proximity defects due to diffraction and process effects [4].

Rule Based OPC: Correction rules are introduced by characterizing the structure with its CD and surrounding proximity. To come up with these rules, the OPC engineer tries to characterize the structures based on CD and space. Then gather real wafer SEM measurements to do the characterization. Finally calculate the amount of compensation required based on the collected SEM measurements.

Rule based OPC started to be required when the features size dropped below 500nm until 130nm. For one dimensional structures a set of CD-through-pitch curves are experimentally measured for a given process. From these data, a one-dimensional rules table is created by interpolating from these data as shown in Figure 3.5. This table lists the required correction for a certain CD across different pitches to maintain that the CD prints as drawn by the designer.

For the two dimensional structures, Optimum line-end treatments and corner serif sizes are also empirically determined for the given process. These correction rules apply on real designs to compensate for the proximity effects for the two dimensional structures.

The rule based OPC approach is simple in implementation once the right set of rules with the correct parameters are found. But as the feature size starts to shrink down to 130nm the rules started to be more complex and less accurate. To

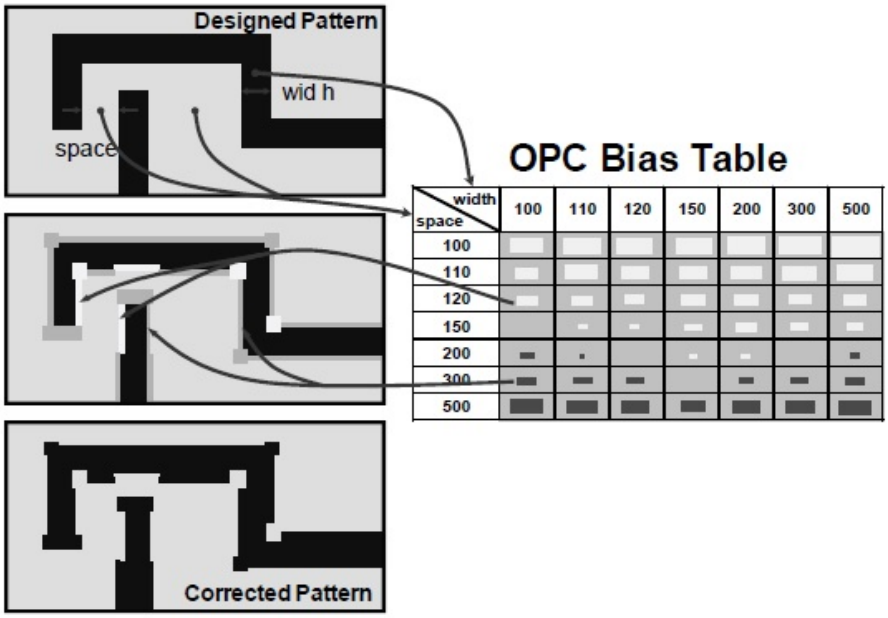

Figure 3.5: Rule-based OPC from a lookup table [4].

gain a better accuracy the complexity increased. A minor increase in the OPC accuracy led to a very large increase in the correction rules count. Also with the minimum feature reduction the complexity increased by another factor which is the variability in geometry of the structures and the close proximity to each other. The rules complexity led most of the semiconductor manufacturers to consider the model based OPC a good candidate for the OPC for the 90nm technology nodes and below.

Model Based OPC, correction is done based on the simulation of the printed image for a given mask. The simulated printed image is used to generate the mask shape by applying a correction algorithm. A correction algorithm aims to minimize the difference between the simulated image and the desired image on wafer such that the mask shapes are changing to generate the desired feature. A flow chart of the model based OPC is shown in Figure 3.6.

As discussed in chapter 2, the final image on wafer is based on the optical system and resist. The model based OPC needs models. The model based OPC is limited by the models accuracy. The Optical and resist responses are the two systems that are needed to be modeled to perform model based OPC. Model based OPC reduces the complexity of the rule based approach although it introduced two new major

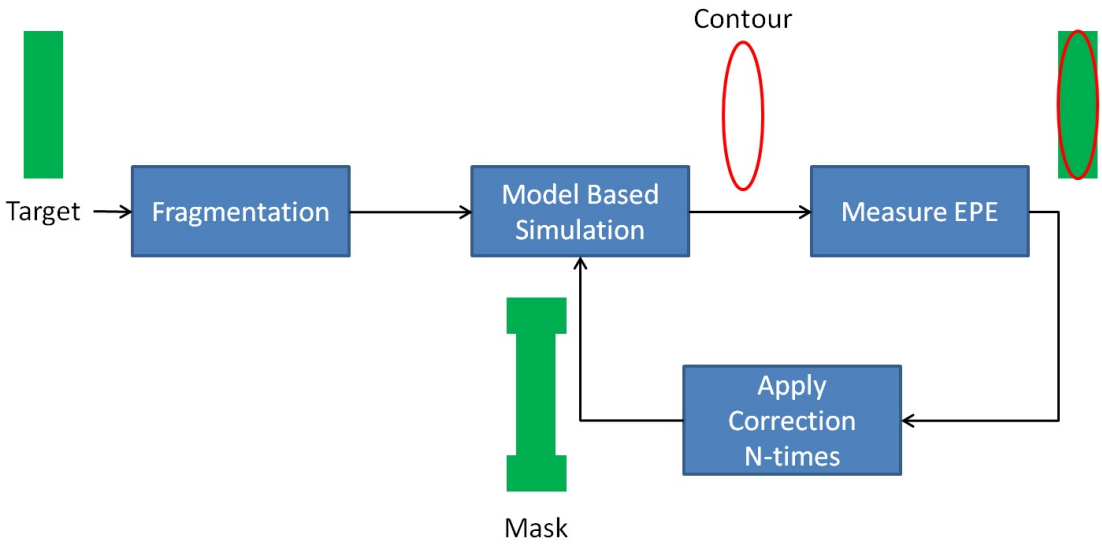

Figure 3.6: Model based OPC Flow Chart

challenges. Firstly the models accuracy, since model based OPC requires to have process models, a considerable effort is needed for calibration of the lithography model that predicts each design pattern response. Secondly the runtime, since correction has to be done on the full chip, the simulation time of the model has to be very fast [19].

Physical models predict the printed image accurately on the wafer, therefore, the accuracy challenge is eliminated. But physical models fail to achieve an acceptable runtime to simulate a fullchip level, therefore, a compromise is required. Physical resist models are required to solve the non linear behaviour of the resist due to light absorption described by the two Equation 2.12 and 2.13 plus the need to model the development process as well. Hybrid physical/emperical models are capable to achieve both acceptable accuracy and runtime. Hybrid models simulate the image within acceptable error of the minimum design and simulate full chip with an acceptable runtime. Hybrid models are sometimes referred to as compact models.

The hybrid process models combine a reasonably accurate and physically correct aerial imaging model with a resist model. For the aerial image calculation, Sum of Coherent Sources (SOCS), an approximate solution to the Hopkins imaging equations, gives extremely fast computation times by pre-computing a small number of coherent convolution kernels for a given source and lens pupil [20]. Diffusion effects

induced in the resist such as the PEB diffusion are usually approximated by allowing the aerial image to diffuse. Diffusion effect can be conveniently calculated using a Gaussian diffusion kernel in the SOCS formulation. Resist development effects are described by a variable threshold model shown in [21] and [22]. Variable threshold models are giving a good accuracy with an acceptable runtime. However, as the models are empirical models they need extensive model calibration.

The model based OPC flow is described in Figure 3.6, Firstly, to perform the simulation the edges are divided into small sections called Fragments. Each fragment moves individually during the correction. Each fragment has a simulation points called control site. Sites are placed ideally orthogonal to the expected printed contour. Sites are the locations where the The image is simulated with the hybrid model to predict the image in the resist. The differences between the simulated image and the desired image is calculated Edge Placement Error (EPE). Finally based on the EPE the correction movement of each segment is calculated so that the remaining EPE becomes zero. This process is iteratively done until the final EPE per fragment is zero or below a certain limit. The final geometries are the final mask.

As shown in Figure 3.7, Model based OPC is used to generate a mask shape that produces an acceptable resist shape for a given lithography process that is assumed to be operating at its nominal conditions. Thus it increases the resolution. as those features initially were not being able to print with high quality after applying OPC the image is meeting the target.

- **Sub-Resolution Assist Features "SRAF"**

OPC manages to make the features print as drawn by the designer which increases the resolution limit, however the OPC can not change the response of the feature to the process deviation encountered in dose and focus deviations. Taking the examples of isolated line and dense array responses to dose and focus variations shown in Figure 3.8. For each graph the x-axis represents the focus deviation, the y-axis represents the CD, and each curve is drawn for a given dose value. For a given dose condition the focus effect on the dense structures line width deviation

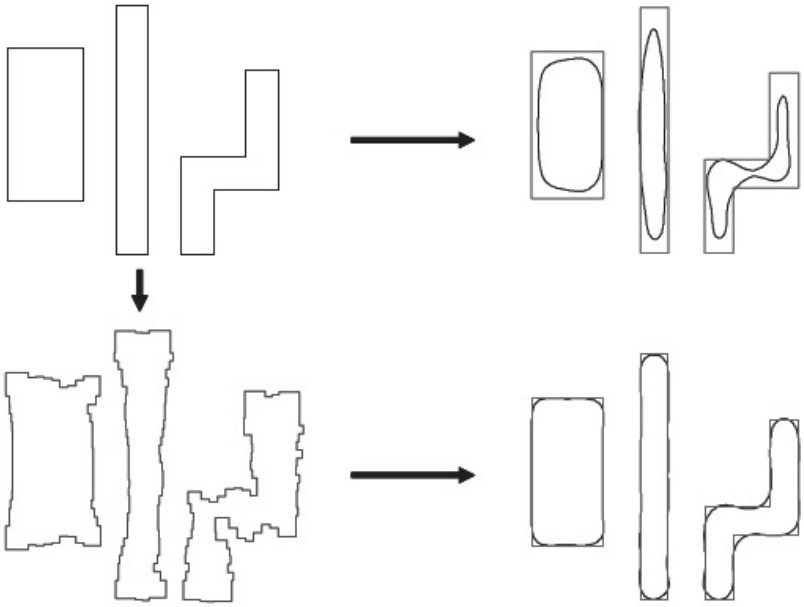

Figure 3.7: Example of model-based OPC: the original design (upper left) prints very poorly (upper right). After model-based OPC, the resulting design (lower left) prints very close to the desired shape (lower right) [1].

can be considered negligible if compared to the deviation in the isolated structure for the same defocus deviation. This makes the isolated feature line width across the full chip hard to control. Aggressive line width variation across the full chip impacts the electrical behaviour of the designed circuits.

Sub-Resolution Assist Features (SRAF), also called, Scatter Bars (SBAR) are placed to reduce the difference in the response of the focus and dose variation on the isolated and dense structures. SRAFs are narrow lines or spaces placed adjacent to a primary feature in order to make a relatively isolated line (large pitch) or semi-isolated line (medium pitch) behave lithographically more like a dense line (small pitch) [23]. These narrow lines are sub resolution lines that are not designed to print across the different dose and focus variations of the process. As shown in Figure 3.9 an isolated contact with/with out SRAFs under the same defocus variation, with focus changes the left handside shows large deviation in the line width compared to the right hand side figure.

SRAF insertion looks simple for the isolated structures, however, the implemen-

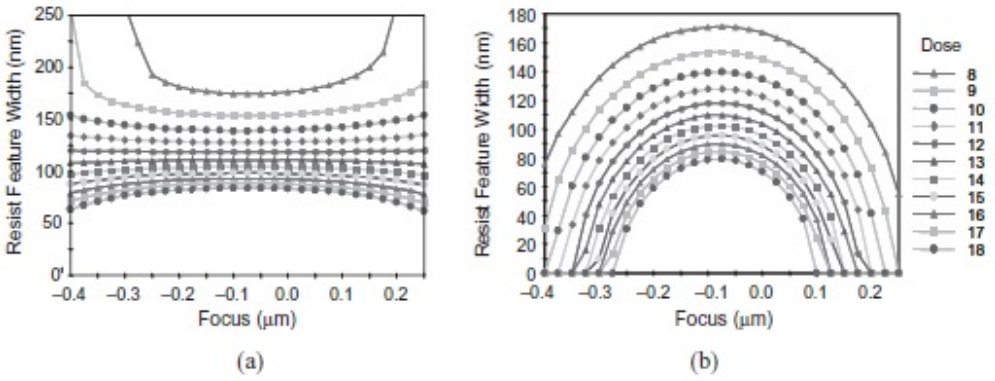

Figure 3.8: Focusexposure matrices (Bossung curves) for (a) dense and (b) isolated 130-nm features (isolated lines biased to give the proper linewidth at the best focus and exposure of the dense lines, λ 248 nm, NA = 0.85, quadrupole illumination optimized for a 260-nm pitch)

tation is far from being simple. Unlike the ideal case of isolated and dense structures SRAF insertion is a complex problem. SRAF insertion techniques during the past 20 years have gone from low complexity level to extremely complex with the reduction in the feature dimension [24]. The major two techniques are rule based SRAF and model based SRAF. Rule based is quite complicated when it comes to 2D structures. Complex 2D structures with varying dimensions exists on full chip. With the change in the 2D structures dimensions and proximity the optimal SRAF varies in both location and size. On the other hand the model based shows promising results when it comes to SRAF insertion. As the insertion is model based so accurate models with reasonable runtime are required.

SRAFs helped in having a uniform feature dimension across the full chip especially for nodes below 28nm as the fullchip geomteries gets more complex and the allowed deviation in the line width gets smaller.

3.3 Technology Node Development Cycle

In the previous section, the resolution enhancement techniques are introduced. In this section the use of RET is described. The mask generation process is a major

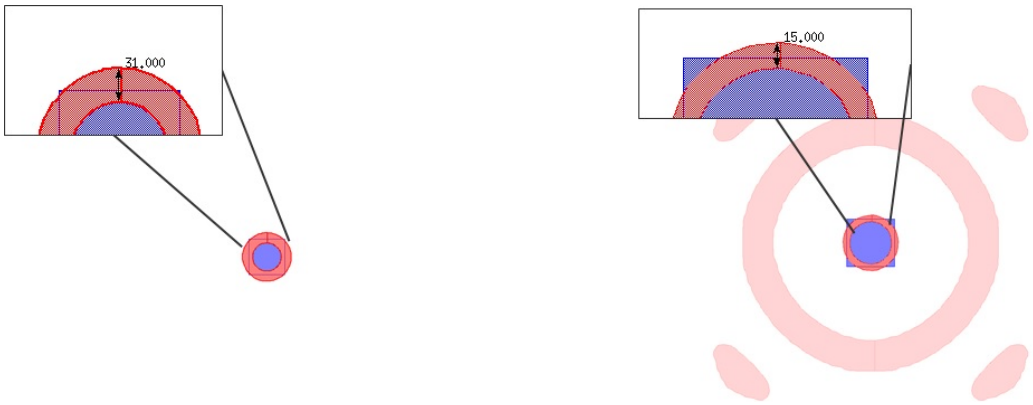

Figure 3.9: Impact of inserting SRAF for isolated contact across where the left hand side is the line width deviation of the contour without SRAFs and the right hand side is the response for with SRAFs. Left hand side shows CD [1].

step involving several tasks. To generate a mask multiple enhancement techniques are used. Each of which is done to achieve a specific purpose and all the techniques need to be considered at the early stages of the technology node development. RET affects each other like the insertion of SRAFs requires the regeneration of the OPC layer since SRAFs change the diffraction orders of the main feature.

A schematic in Figure 3.10 shows the basic steps for mask generation. This flow is considered one of the basic flow. For advanced technology nodes from the 22nm and below, this flow is becoming more complex. As an example, the illumination sources are no longer a standard illumination source (dipole, annular, standard, etc) but they are pixelated sources. The pixelated sources are generated with an optimization process to achieve a source that meets the specific focus and dose deviations for the most critical structures [25].

3.3.1 Process Modelling Test Pattern Mask Generation

After the process parameters are defined, such as the illumination type, type of the resist used and scanner configuration, a test pattern mask with several thousands of structures is generated. This test mask is exposed and printed. This test mask contains thousands of patterns that are used in process models calibration and the study of the of the etching process. This test pattern mask is used to collect the SEM measurements that will be used to calibrate the empirical process models.

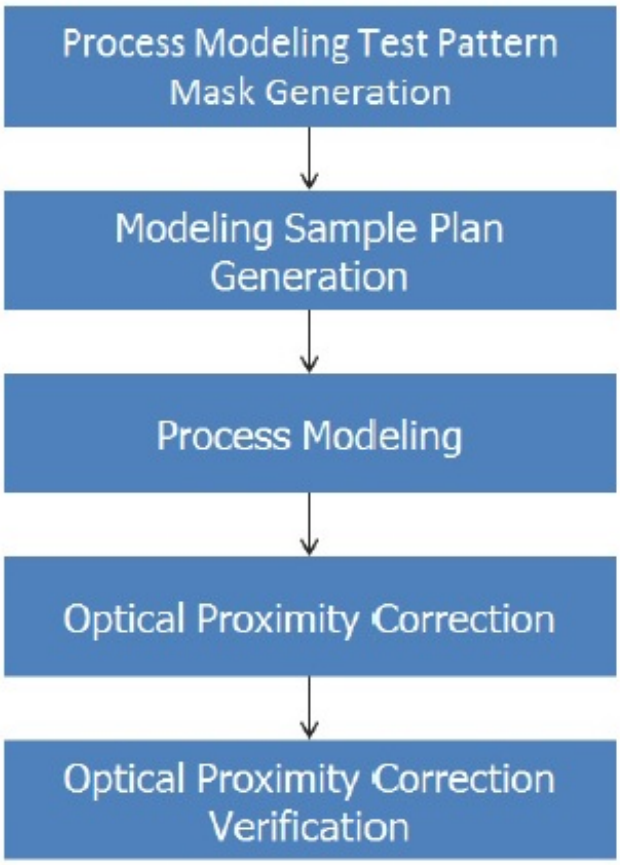

Figure 3.10: Steps to generate the mask for a certain design

Special considerations need to be taken into account to avoid wasting of the mask and maintaining the measurements fidelity to be used for process modeling. This section will be discussed in more detail in chapter 4 emphasising on building a modeling test mask.

3.3.2 Sample Plan Creation

Since the models used to describe the process are physical/emperical models. Empirical models are based on fitting the physically based parameters using a training SEM measurements. Sample plan is the group of the training structures to be measured from the test mask that are use for the model calibration. Several aspects are considered to define the sample plan. Firstly, this set needs to be a representative

set of data where the most critical structures are represented in the plan such as the minimum feature. Secondly, this set of measurements is required to be measured with accuracy. Thirdly, the sample plan need to be of a reasonable size as the modeling turn around time is directly proportional to the sample plan size. The larger the sample plan size the more time is consumed to collect the SEM measurements. Each structure in the sample plan is required to be measured more than one time from different locations on wafer and from different wafers as well. The methods that are used in selecting the sample plan will be discussed later in this chapter.

3.3.3 Modelling

The SEM measurements are ready for model calibration after data filtering to remove the failed SEM measurements. Failed SEM measurements have a huge impact on the final model accuracy. The OPC models developed are generated using a technique of decoupling the optical and resist model effects in order to achieve better model accuracy, specifically through focus as studied in [26].

Usually the Optical models are calibrated in a separate calibration step. The optical models that are typically used in this flow are based on the sum-of-coherent systems (SOCS) approximation described in [19]. The sum-of-coherent systems (SOCS) approximation currently represents the base of the fast image computation. This SOCS uses singular value decomposition to decompose the optical system response function in the Hopkins imaging equation into a sum of products of its kernels. Since the system is partially-coherent optical imaging system then it can be represented as a sum of images formed by coherently illuminated optical systems with transfer functions corresponding to the kernels of the optical system response.

Then the resist model is calibrated. The most widely used resist models in the industry are compact models. One of the compact models is the variable threshold model. Variable threshold models are based on the data fitting approach of the measurement data. In [21] the variable threshold models was tested over 14 different semiconductor company processes experimental setups totaling 3000 CD measurements to prove the accuracy of the prediction of the variable threshold model. Also

In [21] the variable threshold basics are discussed. Variable threshold models are based on the resist development simulation discussed in Section 2.4.1.3.

A variable threshold model states that for each mask pattern edge there is an image intensity T at which this edge is printed. For a given structure to predict the printability of the CD, the threshold equation is calculated at the edge to determine the printing threshold. The printing threshold is proven in [21] to be a function of image parameters. This model is based on the definition on a simplified form of Dill's equation done in [27] and [28]. VT-5 models places a group of control points, called site, normal to each edge as shown in Figure: 4.1 (a). An image profile is calculated at each control point along the site as shown in Figure: 4.1 (b). Two more control points are inserted tangential to the edge to detect the curvature of the feature. The threshold polynomial T can be represented by,
T = f (Imin, Imax, Slope, Factor, Density),
• I_{min}/I_{min}: The minimum/maximum intensity value found within window of width equal to 2*search range (0.5*lambda/NA).
• Slope: The first derivative of the intensity profile calculated along the site at the reference threshold.
• Factor: The second derivative of the intensity profile calculated along the edge at reference threshold.

The process model simulates the calibration data set with accuracy such that the difference between the simulated contours and the SEM measurements provided is within the process acceptable limits. The acceptable difference between the measurement and simulation is usually determined based on the mean error in the measurements. Yet those models need to predict other structures which are not used in calibration with the smaller or equal error to the calibration set so that the OPC is safe. These process models are used to predict the simulation contour for any structures during the OPC. This introduces a new concept of model predictability and model stability. Model stability is defined as the model response doesn't change radically due to a change in the input data slightly different from the calibration set. The model predictability is related to the maximum error of the predicted full chip contour with respect to the wafer image. Many techniques are

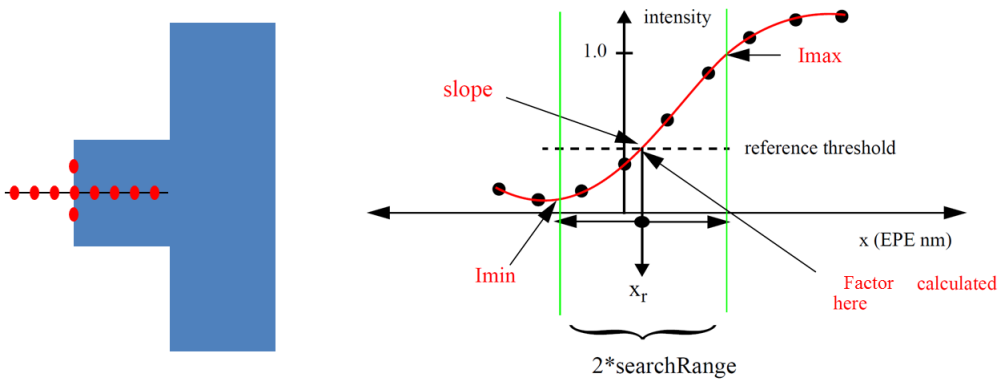

Figure 3.11: (a) showing the site placement along the edge of the fragment, (b) showing the aerial image profile on the site location

used to test the model stability and predictability the most basic and widely used one is the testing over verification data set as stated in [21].

3.3.4 Optical Proximity Correction Flow

Using the process models, the OPC flow is performed. The OPC flow is not as simple as described in 3.2.2.2, since it contains several preparation steps that need to be done ahead. The input of this flow are the process models, special treatment to the design known as pre-OPC which will be discussed later on, and finally an input design to be printed on wafer that is compliant to design rules of the fabrication facility rules.

1. Pre-OPC implementation:

   The output layer of the pre-OPC is the final on-wafer litho target. This step starts from the initially drawn design geometries, modifying the geometries to accommodate for the etch effects depending on the process models used, and if there is special device compensation to meet certain electrical characteristics is required. Pre-OPC may contains global bias, selective device compensation, etch compensation and Clean-up code (nub cutting, notch filling, jog smoothing)

2. SRAF Insertion Flow:

   SRAF is inserted based on the geometrical distribution to make the weak features less vulnerable to dose and focus variation. Several methodologies has been used to insert the SRAFs. These methodologies aim to maximize the process window of the weak structures and avoid the printability of the SRAF if the process drifted of the nominal conditions of dose and focus. The major two techniques for SRAF insertion is the rule based, or the model based, or a hybrid technique between the two techniques.

3. OPC

   OPC uses the lithography target and the SRAF to generate the final mask shape. The latent image of the litho target and the SRAF is simulated and a correction algorithm is applied to make the final contour meet the target. Latent image simulation is considered the backbone of the correction since without accurate simulation the correction will not be optimum. A suboptimal correction is not desired as it will degrade the whole process yield.

   During the OPC step the SRAF may be optimized further to reduce the variation due to focus and dose variations as studied in [29]. This flow has proven to add value to the metal layer at 32nm node.

3.3.5 Optical Proximity Correction Verification

Optical Proximity Correction Verification also known as Optical Rule Checking (ORC) is a method of verifying the post OPC mask data by simulating the printed image and performing geometrical checks to spot critical failures such as pinching or bridging. It is done as part of the mask preparation step that applies the desired RET (SRAFs and OPC). After the mask shapes are generated, a final simulation is performed using a calibrated process model to generate a simulated contour. This contour is verified using geometrical checks to look for minimum line width locations (pinching) and minimum space locations (bridging) also look for additional layer-specific checks such as line-end pullback, contact coverage, or sraf printing. ORC relies on having an accurate model that predicts failure to perform the corrective

actions needed.

3.4 Problem Definition

Looking at the previous framework, the dependency of the final mask for a given design on the process models is discussed. Process models with weak predictability or stability will have a large impact on the quality of the wafer contours. Also many resources will be wasted to generate non-functional chips such as cost (represented in labour cost, mask cost, SEM tool to collect the measurement) and will increase the time to market of a product.

Empirical models have many dependences that may degrade the model performance. With the shrinkage of minimum feature the allowed residual errors are getting smaller and smaller in order to achieve accurate models. In [30] sources of the errors affecting the model accuracy are reviewed. These sources of errors affect directly the model accuracy such as the photomask errors, optical system errors, film stack errors and finally the metrology errors. These source of errors are considered when building a model to reduce the fitting over high error process SEM measurements.

Since the resist models are empirical models they are calibrated based on experimental data contained in the sample plan. Empirical model quality is a function of the sample plan measurement accuracy and the geometrical diversity. Having poor accuracy or limited geometrical diversity will negatively impact the model predictability and accuracy.

Several studies show that a better sample plan used for model calibration improves the models. Sample plan selection takes the measurement accuracy and the geometrical diversity into consideration.

Regarding the accuracy studied in [31], [32], and [33] the sources of measurements errors and analysis of the of variance of the wafer measurements is done.

These studies categorize the sources of errors and determine whether they are systematic errors or random and determine the confidence of measurements to determine how many times each structure needs to be measured with the SEM to reduce the measurement error.

The geometrical diversity of the structures is very important. There are mainly two approaches in the industry for the test pattern selection. The first approach is a heuristic selection of the test patterns from the test pattern mask. The heuristic sample plan is based on the semiconductor manufacturer experience, and the type of structures this technology supports. Another variation of the heuristic sample plan generation is introduced in [34]. In [34], sample plan is selected from a test pattern mask based the image parameters. They used a reduction algorithm to reduce the test pattern mask into unique set of structures based on the image parameters. For each group of similar test patterns only one is chosen to be in the sample plan.

The second approach presented in [35]. In [35] real full chip clips are used in the sample plan. Full chip analysis is done based on the image parameters. Full chip uncovered locations in the image parameters space are used as an extension to the calibration set to be used for calibration to encounter the full chip geometrical diversity compared to the heuristic sample plan.

The heuristic sample plan approach contains test pattern structures that are easily measured with single gauge, also, maximizes the coverage of the sample plan to the test pattern mask. However, assumes that the test pattern mask is covering any full chip, and the selection is done in uniform basis ignoring the real full chip image parameters distribution. Those selected test patterns may lead to models with insufficient prediction. Real full chip prediction issues cause critical failure on mask since models does not predict a pattern failure on wafer. These problems introduced the second approach.

For the second approach, complex structures are captured with SEM by applying multiple gauges on a given structure. This approach suffers from high complexity in measurement compared to the single gauge measurement performed for the heuris-

tic test patterns. Since ArF resist is sensitive the SEM e-beam. Resist exposure to the e-beam leads to resist shrinkage. This shrinkage requires special handling of the extracted gauges to accurately represent the on-wafer contour. This approach can not be adopted easily as it requires special CD-SEM measurement handling. Also each structure has several gauges which increases the calibration time compared to regular model calibration with single gauge per structure.

In this work, new methodology is introduced that selects regular test patterns based on full chip patterns characterized image parameters. A regular modelling test pattern that can be easily measured is used. For every single fragment on the full chip, the image parameters are calculated and used to select test patterns close to these image parameters characterizing the full chip fragments. This approach Maintains the feasibility and simplicity of the regular test patterns selection and improves the prediction of the real product full chip by choosing the closest test patterns in the image parameters space.

Chapter 4

Full Chip Image Parameters Analysis and Sample Plan Creation

4.1 Introduction

In this chapter, a new methodology of creation of a sample plan to enhance the coverage of a process model is presented and discussed. A full chip image parameters analysis is presented. A uniform data reduction algorithm is developed to reduce the plan to several thousands to represent the full chip design. Secondly, a heuristic modelling test pattern mask is created. For each pattern the image parameter are analysed considering manufacturing constrains. Finally, the modelling structures (the sample plan) are selected from the test pattern mask based on the distance within the image parameters space to the reduced full chip data set.

4.2 Full Chip Image Parameter Coverage

4.2.1 Objective

Evaluation of the image parameter space for a full chip after OPC is used for the selection of the heuristic test patterns. The selected test patterns have a similar set of four image parameters compared to the full chip patterns such that similar

image parameters structures are used for calibration of models. This methodology improves the predictability of the models and improves the quality of the OPC.

The output of this flow is a set of four image parameters values and the x, y coordinates on the full chip where this pattern is located. The image parameters are referring to optical image response of the mask for a given illumination source as shown below Figure 4.1. The first three image parameters are quantifiers to the image profile resulting from the optical system I_{min}, I_{min}, and slope. The fourth parameter is the factor. The factor is a quantifier to the pattern geometry being 1D or 2D.

• I_{min}/I_{min}: The minimum/maximum intensity value found within window of width equal to 2*search range (0.5*lambda/NA).

• Slope: The first derivative of the intensity profile calculated along the site at the reference threshold.

• Factor: The second derivative of the intensity profile calculated along the edge at reference threshold.

Calibre®Image Parameters Space Explorer (IPSE) is used for the display of the set of image parameters data since the computer programs are written to generate a compatible format of the resulting files.

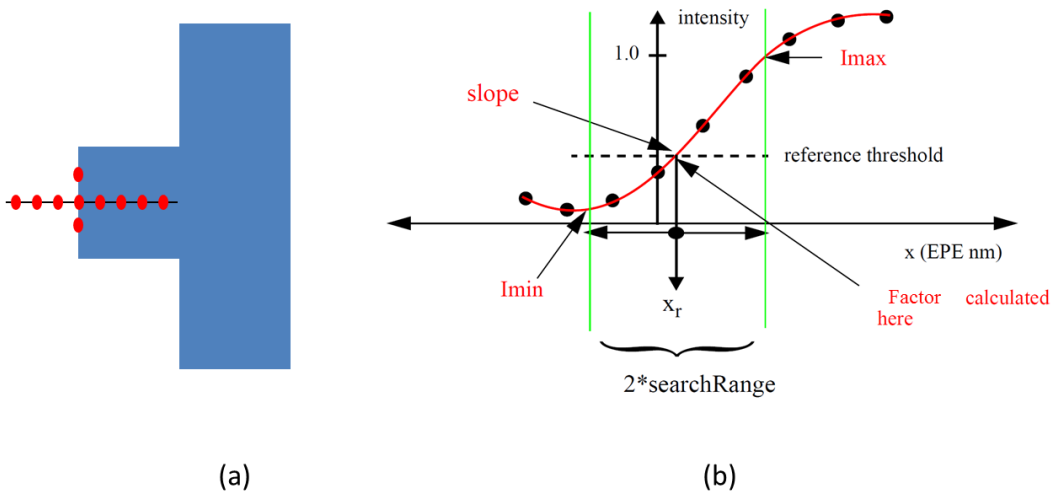

Figure 4.1: (a) The site placement along the edge of the pattern fragment, (b) The image profile at the site location [36]

4.2.2 Flow Details

As shown in the Figure 4.2 the flow consists of 5 main steps to complete the full chip image parameter analysis. Firstly, the inputs to the flow are prepared. Secondly, optical proximity correction using heuristic optical model based on the nominal scanner settings and the illumination source is applied to correct polygons as close as possible to the fully corrected mask using process models (optical model and resist model). Thirdly, the image parameter calculation step utilizes Calibre®Lithography Application Interface (LAPI) code. The Calibre®LAPI allows full control over the simulation and correction algorithm when invoked within Calibre®OPCpro^{TM}. LAPI allows the creation of fully customized RET recipes that suit your advanced process schemes [37]. Fourthly, the calculated image parameter sets are reduced by application of newly developed the C++ code to receive a unique representative for each set. The formatting of the file is compatible to the IPSE display. Finally, the Calibre®IPSE tool is used to analyse the coverage of the reduced set compared to the calibration image parameter space. IPSE provided a utility showing the image parameter distribution using a checker board like representation.

Step 1: Flow Requirements, Initial Optical Model, this model contains the basic source information such as the illumination source map (Annular, Quaser, Standard, etc.) and the resist film stack. A full chip layout contains critical design features.

Step 2: Optical Proximity Correction, due to proximity effects the initial target at the design level does not represent the final mask data as shown in Figure 3.6. Since our aim is to find representative set of patterns that are as close as possible to the final mask patterns in the image parameter space, therefore as explained in Section 3.3.4 the OPC step contains other treatments such as pre-OPC step, SRAF insertion step and OPC step. Those steps are implemented to achieve a mask as close as possible to fully corrected mask using process models.

Step 3: Image Parameter Calculation Code is utilizing Calibre®OPCpro^{TM} simulation engine to calculate the image parameter for each pattern in a full chip post

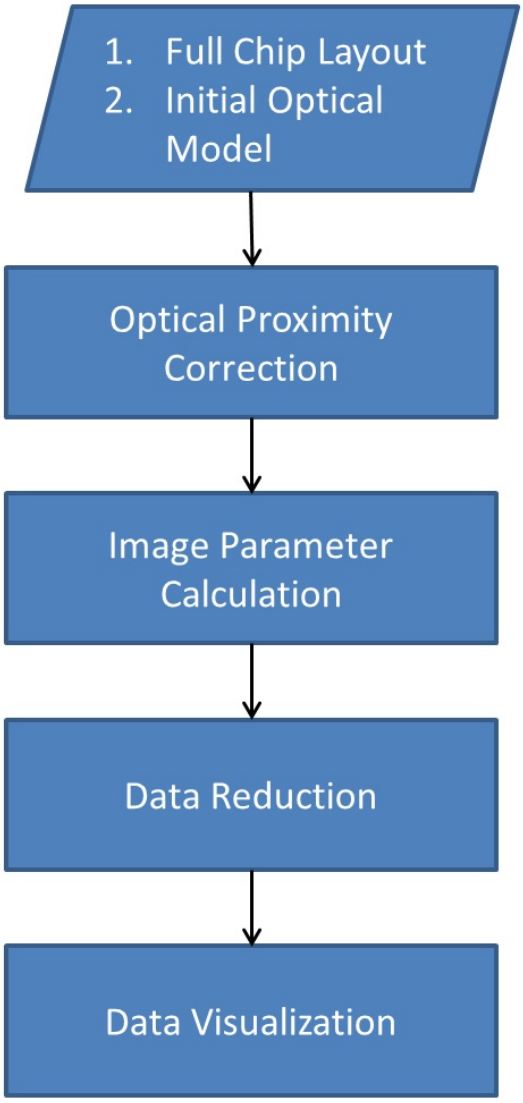

Figure 4.2: Full Chip Image Parameter Coverage Analysis Flow

OPC. For each pattern edges are divided into smaller fragments. Each fragment holds a line of simulation points (site). A single site is located per fragment in this work. At each site the four image parameters are calculated.

This work is using C-Lapi. The purpose of the C-LAPI code is to write out the simulation sites' image parameters into a file. The C-LAPI code is invoked from the OPCpro engine. The exact site location is determined by the fragmentation scheme provided in the setup file. The information written in the log file are in the following order, I_{min}, I_{max}, Slope, Factor, site coordinates, and finally Cell name.

Simulation artefacts occur at corners and jogs, because the simulated contour is not orthogonal to the simulated site. A jog is a smaller convex concave edge relative to adjacent edges. Sites on jogs are not orthogonal to the image. Sites on jogs will report articulately increased I_{min} and reduced I_{max} values. Sites must be placed orthogonal to the simulated contour. Sites too close to the corners also provide misleading image parameters and are eliminated from the final image parameter set. Corners are very sensitive to the site location such that I_{min} and I_{max} vary due to site placement, hence they are eliminated as well.

Symmetric Line ends and space ends are considered important structures. They have sites in the middle of the line end and space end, therefore, their sites are placed normal to the image, and hence correct image parameter sets are extracted.

Step 4: Data reduction or image parameter reduction binning code reduces the output from the C-LAPI calculation from millions of fragments to smaller set of unique fragments. The code selects one unique set of image parameter per bin. Each selected set of image parameter is linked to the corresponding fragment on the full chip. All the full chip fragments are classified based on the four parameters I_{min}, I_{max}, Slope, Factor. The generated information uses the IPSE format.

The code spans over each parameter for all the full chip fragments. The range of each image parameter minimum and maximum is determined. Then each parameter in the set is divided into equal bins of total count δ such that the final bin size is fully defined by following set of equations,

$$\begin{aligned}
\Delta I_{min} &= \frac{Max(I_{min}) - Min(I_{min})}{\delta} \\
\Delta I_{max} &= \frac{Max(I_{max}) - Min(I_{max})}{\delta} \\
\Delta Slope &= \frac{Max(Slope) - Min(Slope)}{\delta} \\
\Delta Factor &= \frac{Max(Factor) - Min(Factor)}{\delta}
\end{aligned}$$

Step 5: Data Visualization, Finally the reduced sets of image parameters are loaded for visualization using a checker board. Since each fragment is represented by a set of four image parameters a checker board is used to visualize the 4D sets. Sample checker board is shown in Figure 4.3. The major red x, y axis of the checker

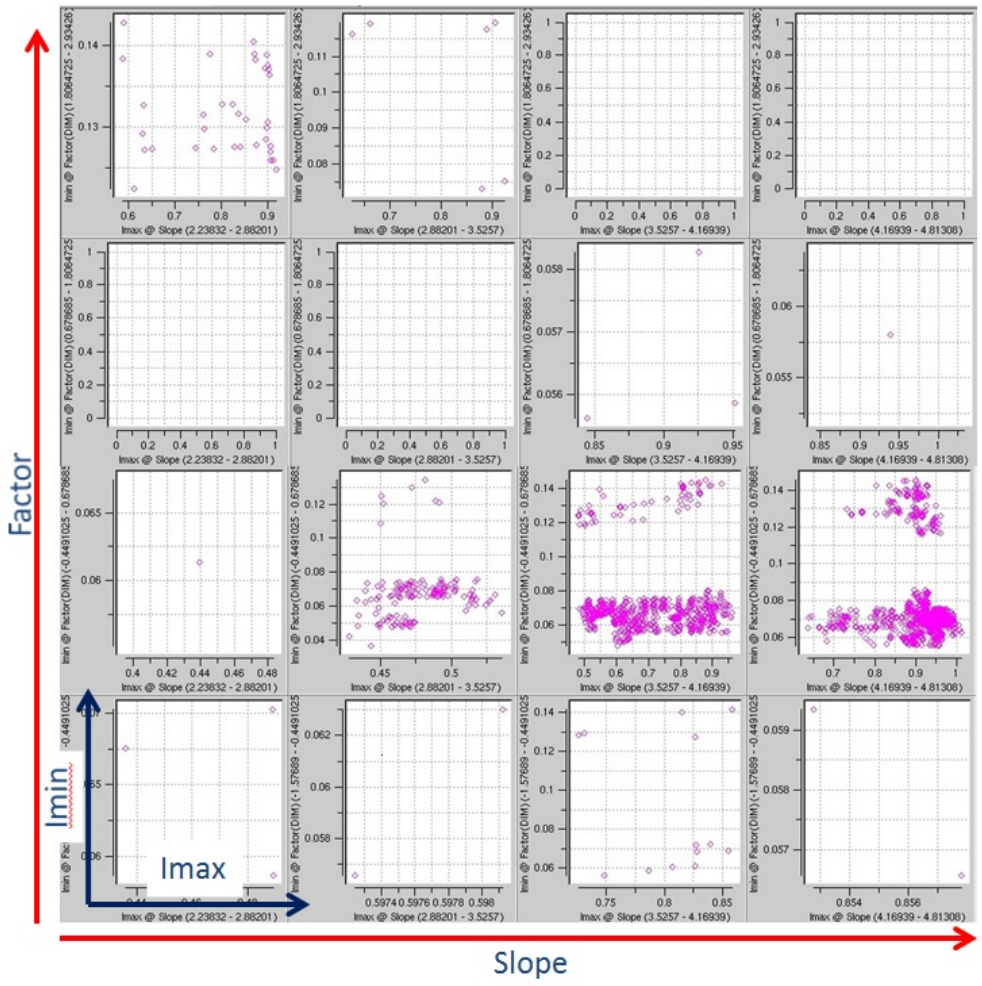

Figure 4.3: IPSE Checker Board

board represents the slope and factor, respectively, whereas the minor blue x, y axis of the checker board represents the I_{max} and I_{min}, respectively. The main benefit of the review process is to visualize the range of each of the parameters.

4.3 Process Modelling Test Pattern Mask Generation Flow

4.3.1 Objective

The motives to build a process modelling test mask:

1. Collect a better image parameter coverage sample plan.

2. Achieve enhanced process models coverage.

3. Improve process models predictability.

The expected output of this step is a layout containing all test pattern structures.

4.3.2 Flow Details

Test pattern generation is described in Figure 4.4. The flow consists of five steps the first of which is collecting the mask requirements, the second is the test patterns definition and the ranges evaluation of the critical dimensions and spaces, the third is the compilation of the test patterns which translate the test patterns from definition to layout format, and the fourth is the placement of the patterns to form the test pattern mask, finally fifth is the mask review and image parameter comparison.

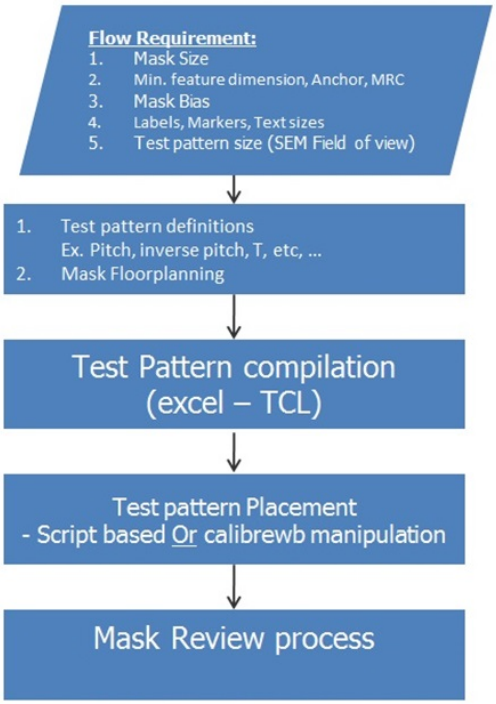

Figure 4.4: Modelling Test Pattern Mask Flow

Step1: Flow requirements,

1. Mask size: allocated mask area for the test patterns mask
2. Minimum feature size: minimum allowed feature size and critical dimension for width and space.
3. Anchor feature: this is the most critical feature used by the process engineer to anchor the process.
4. Mask bias: what is the mask bias to achieve a certain feature dimension on the wafer.
5. Field Of View (FOV): the scanning electron microscopy (SEM) final magnification field of view in order to recognize the structure properly with the SEM tool.
6. Labels, Markers sizes: to ensure it is being properly placed in the field of view.

Step 2: Define the test patterns, depending on the layer under development usually Line and Space layers (Poly, metal) share the same set of structures. Structures are being classified as 1D and 2D. Examples of the most important 1D structures are: Pitch, Inverse Pitch, Iso Pad, and Iso. Examples of the 2D structures are: broken H, H, Lineend, Inverse Lineend, Dense Lineend, and Inverse Dense Lineend.

Step 3: Test Pattern generation: A Tcl based utility is used to generate the desired golden mask patterns defined in step 2. For each structure used different dimensions are placed on the mask. Dimensions variation plan is defined, label sizes, and marker shapes (SEM Marker – used to focus the SEM tool during the measurements), and finally the area allocated for each structure is being calculated.

Step 4: Placement Step, structures are collected all together in the final layout. Placement could be done with a Calibre®Workbench Tcl script. Manipulation of the layout is needed to maximize the utilization of the mask area. Several methods is used to manipulate the structures placement In our methodology Calibre®workbench Tcl scripts is used.

Pattern placement avoids wasted area on the mask. Step 3 is revisited to optimize the area utilization. for example, if the allocated test pattern mask area is

1mm x 1mm and the total area utilized by all the patterns is 1.1mm x 1mm so the test patterns structures allocated area may need to be revisited to reduce the 0.1mm to fit in the mask area properly.

Step 5: Mask Review Process, upon finishing the mask, a final review step is required, by running design rule checks for the minimum dimension checking.

4.3.3 Additional Considerations

The following points should be considered during building a test pattern mask to avoid problems with the selected structures during the sample plan creation and ensure the mask area utilization,

• 1D structures are characterized by higher fidelity in the measurements, hence it is recommended to have a smaller step size around the smaller features. The step size should be greater then the mask shop expected CD uniformity error.

• The Optical diameter typically 1 to 2 microns. It is recommended to have each test pattern structure dimension from end to end to be 3 to 5 microns. These dimensions are parameters for some of the test patterns and could be adjusted to the fit the space of the test mask.

• Labels and text are placed at a distance (more than the optical diameter) in order to avoid any optical effects on the patterns and reduce the risk of jeopardizing the image fidelity of the test patterns wasting the whole mask.

• Mask should be exposed at the same conditions that will be used for production, and deviation from the nominal conditions during exposure should be reported.

• During building the mask, some space should be spared for real design verification clips to be used in the process model verification using SEM image overlay method. The verification clips are logic structures and SRAM cells. Those verification clips are used to check the SEM contour matching versus the simulated

contours.

4.4 Modelling Sample Plan Generation

4.4.1 Objective

The modelling sample plan generation selects the calibration data set from the heuristic test patterns, generated in the previous section. A first version of the methodology of the modelling test pattern generation is shown in [36]. Sampling of the test pattern mask is done taking into account the metrology confidence of the test patterns ensuring to maximize the test pattern mask full coverage without reducing the SEM measurements quality. A second version of the test pattern selection was developed to take into account the full chip fragments image parameter analysis. By minimizing the image parameters distance between the selected test pattern image parameter and the full chip fragment image parameter. The closer the test pattern structure image parameters' to the full chip fragment image parameters' the more priority is addressed to the structure compared to other structures in the test pattern mask. After the test patterns selection is complete, locations that could not find a closer structure are reviewed and iteratively corrected to minimize the distance between the full chip structure and the nearest heuristic test pattern.

The output constitutes a sample plan containing the structures with image parameters that are covering the full chip data domain and at the same time located closest to the full chip fragments image parameters. Points in the full chip that could not find a close point in the defined grid are reported for further treatment and manual review.

4.4.2 Flow Details

As shown in the Figure 4.5, the flow mainly consists of 3 steps. Firstly, the full chip and the golden mask image parameters are quantized using the same grid which is based on the full chip data. For each grid unit the distance between the full chip

and the test pattern mask structures is evaluated. The test pattern structure closest to the full chip data within each grid unit is selected and reported as a candidate to be inserted into the sample plan. Finally the selected test patterns are reviewed in the data visualization and those on the full chip data that could not find a proper match are reviewed for corrective action.

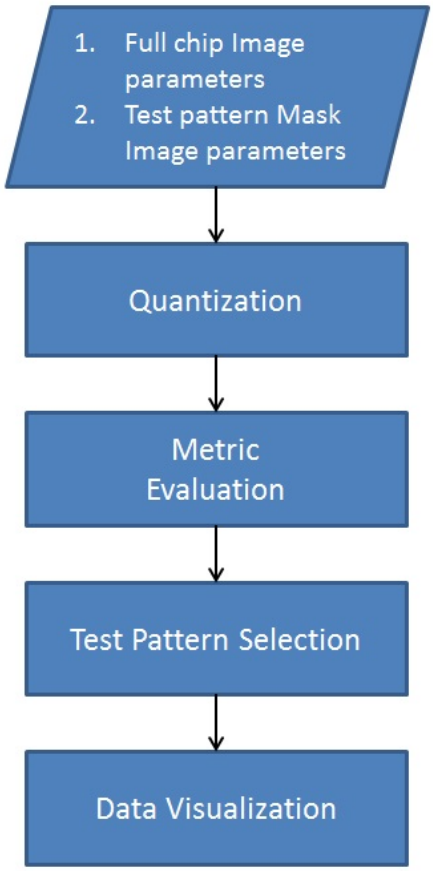

Figure 4.5: Sample Plan Generation Flow

Step 1: Flow Requirements:

1. Reduced full chip sets of image parameters.

2. Test pattern mask image parameters data.

Step 2: Quantizations:

The full chip reduced sets of image parameter are quantized based on a user defined grid such that each element in the full chip data gets an ID that consists of four integers. The same approach is applied to the mask test patterns using the same

grid as defined for the full chip.

Step 3: Metric Evaluation:
Test patterns and full chip points falling into the same bin are eligible for metric evaluation. The distance between the points in the image parameter space is the used metric.

The Metric equation is defined as follows:

$$DistanceMetric^2 = (Imin_{fc} - Imin_{tp})^2 + (Imax_{fc} - Imax_{tp})^2 + (slope_{fc} - slope_{tp})^2 + (factor_{fc} - factor_{tp})^2 \quad (4.1)$$

Step 4: Test Pattern Selection:
After the metric evaluation in step 3. Each bin contains 1 set of image parameter of the full chip data and more than 1 set of image parameter of the test patterns. Metric is the basis of comparison. Test patterns with set of image parameters closest to the full chip point is chosen to be in the sample plan.

Step 5: Data Visualization:
Calibre®IPSE is used as visualization tool of the 4D sets of image parameters. The two sets of image parameters are overlaid to compare the image parameters of both the test patterns and full chip. Also the density distribution of the test patterns relative to the full chip is reviewed.

4.4.3 Additional Considerations

This flow is iterative. In each iteration, the euclidean distance is used as the metric to find the closest test pattern in the image parameter space to the full chip, therefore a fixed quantization step size is used in every iteration to make the metric act as a proper differentiator between two test patterns structures. The quantization step size consists of set of four grid sizes. Each grid size corresponds to an image parameter. The grid size for each of the four image parameters is determined depending on this image parameter range of that parameter in the full chip image parameter space. For a given iteration, I_{min} has a grid size that may be different

in value from the I_{max} grid size depending on the range distribution of the two parameters for the full chip. Quantization defines the search boxes in the 4D space by normalizing the image parameter value to a non-uniform grid size. This non-uniform grid depending on the distribution each of the four image parameters in the space. A study of the image parameter distribution of the four image parameters is needed before running this flow to properly select the quantization step size.

At a given iteration, each of the test patterns and the full chip set image parameter is quantized to the quantization step size. After quantization a single full chip set of image parameter is selected within each grid step. The distance between the full chip set of image parameter and the test patterns sets of image parameters within each bin is calculated. The nearest test pattern is selected. If a set of image parameter in the full chip after quantization is not finding a match, it is a candidate for the next iteration.

In the next iteration, a larger grid size is calculated. The input to the next iteration are those full chip sets of image parameters that did not find a match in the previous iteration. These are quantized with the larger grid size and hence the allowed distance metric is changed to find a close the nearest test pattern set of image parameter.

The iterations scheme starts with a fine step size. The small step ensures that the first quantization step of the full chip does not lose any pattern due to coarse quantization process since only one full chip set of image parameter per bin is selected. As the iterations count increase the grid size increases and the search box and the allowed metric distance increases, hence, more matching points on the full chip fragments are found.

Chapter 5

Results

5.1 Introduction

This chapter will be divided into three sections. The first section is showing the image parameters analysis for a full chip layout, and the mask building process is started to select the sample plan which covers the full chip image parameters space. Finally, models are calibrated using the image parameter generated sample plan and compared to models calibrated with a heuristic sample plan.

5.2 Full Chip Image Parameter Coverage

5.2.1 Testcase Conditions

A sample design is exposed with the following illumination conditions: annular source (outer radius: 0.7/ inner radius: 0.4), wavelength: 248nm, NA: 0.68. The design layout size is about 2mm x 2mm. A single layer (line and space layer) is used in this designs.

5.2.2 Flow Implementation

Recalling the discussed methodology at Section 4.2 shown in the Figure 4.2, An initial optical model is constructed for the illumination condition stated above. The threshold of the optical model is anchored to be 0.28 such that when the tightest pitch image formed by the optical model is evaluated at this intensity the resulting

contour image is equal to expected on-wafer measurement. The optical model acts as an approximation for the real exposure process. This optical model is used in performing simulation for the OPC step.

Second, optical proximity keyword is built as explained in Chapter 3. Recalling the three main steps in the keyword, the pre-OPC then SRAF insertion finally performing OPC. Global biasing is applied, but no SRAF are inserted and then OPC is applied. OPC is using 10 iteration of model based correction using the initial optical model. A constant feedback is used to ensure the stability of the correction.

After the completion of the OPC image parameters are evaluated for each fragment using C-LAPI developed code. Artefacts are removed as explained in Chapter 4. Finally, image parameter sets are reduced by uniform sampling and viewed using Calibre IPSE for display as explained in Chapter 4. The full chip image parameters post OPC are shown in Figure 5.1.

Each green triangle on the graph represents an image parameter set for a fragment on the full chip. The major axes represent the slope and the factor. The major x-axis represents the slope value and the major y-axis represents the factor value. For each small graph the minor axes represent I_{min} and I_{max}. The minor x-axis represents the I_{max} value and the minor y-axis represents the I_{min} value. The factor spans the range from -1.67 to 3.02. The slope spans the range from 2.16 to 4.83. The I_{min} spans the range from 0.031 to 0.14. The I_{max} spans the range from 0.43 to 1.002. The I_{min} does not be exceed 0.28 and I_{max} must not be less than 0.28 which is the threshold for printing. We can see that the majority of the fragments are located in the third row from the top of the graph particularly in the third and fourth columns where the factor value is between -0.497 to 0.677 and the slope is between 3.496 to 4.83. The distribution is less dense in other charts. This graph represents the full chip fragments without artefact.

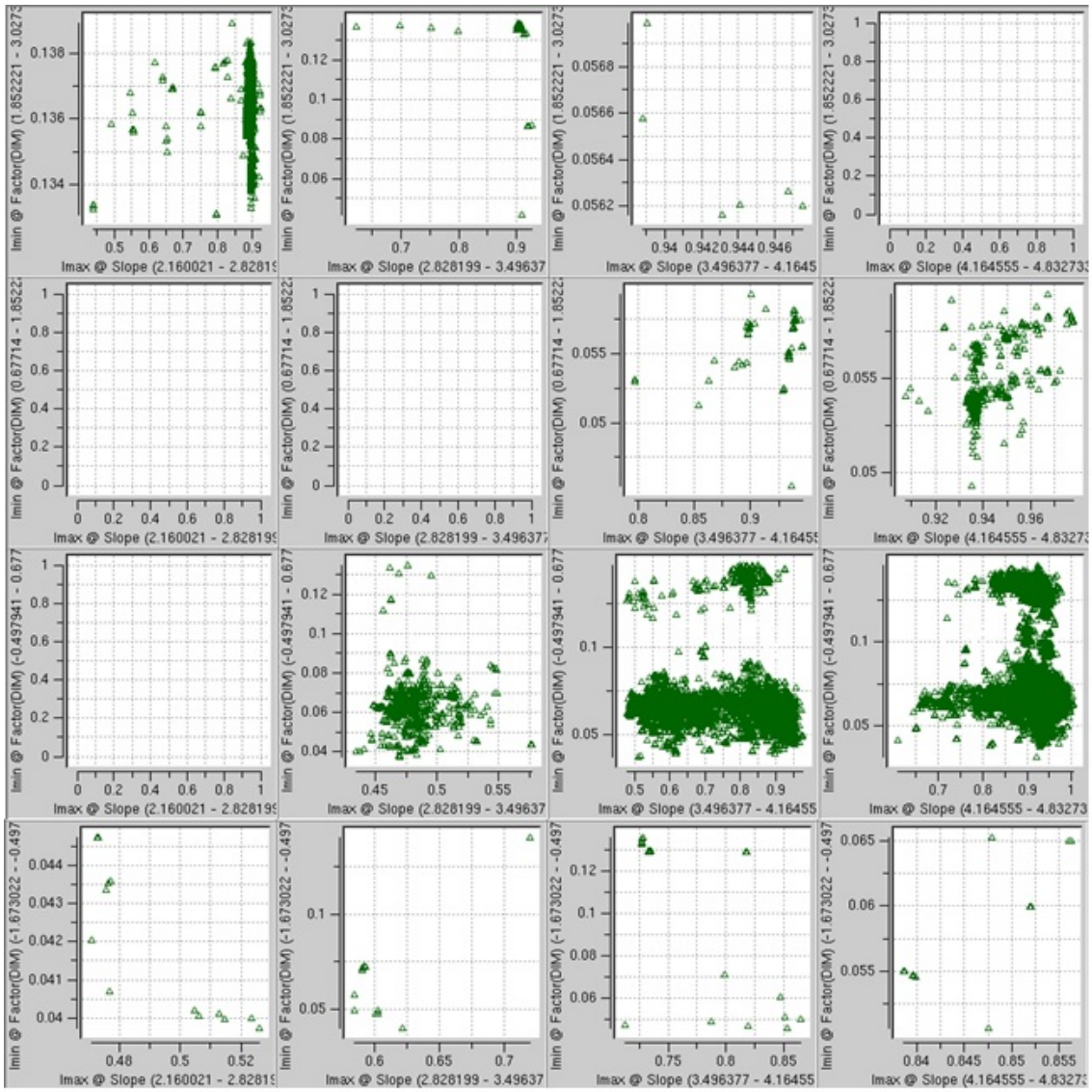

Figure 5.1: Full Chip Image Parameter Coverage Analysis Checker Board without Artefacts

5.2.2.1 Discussion

After applying OPC, the maximum I_{min} is less than the threshold which means there are no bridging structures in the full chip. Also the minimum I_{max} is greater than the threshold which means there are no pinching structures in the full chip.

At the high density location in the checker board, fragments are located with factor between -0.497 and 0.677 and the slope is between 3.496 and 4.83. Having a factor value close to zero represents that the curvature at the control points tangential to the edge is equal to zero. This means it is a 1D structure or close to the 1D

structure. For a line/space layer after applying OPC, majority of the patterns on real design are 1D patterns compared to the 2D patterns low density representation in other factor ranges.

In the Figure 5.2, the same full chip was analysed with out the removal of the artefacts. Each of the pink diamonds on the graph represents a fragment on the full chip and also included artefact. Figure 5.3 shows the overlap between the two graphs.

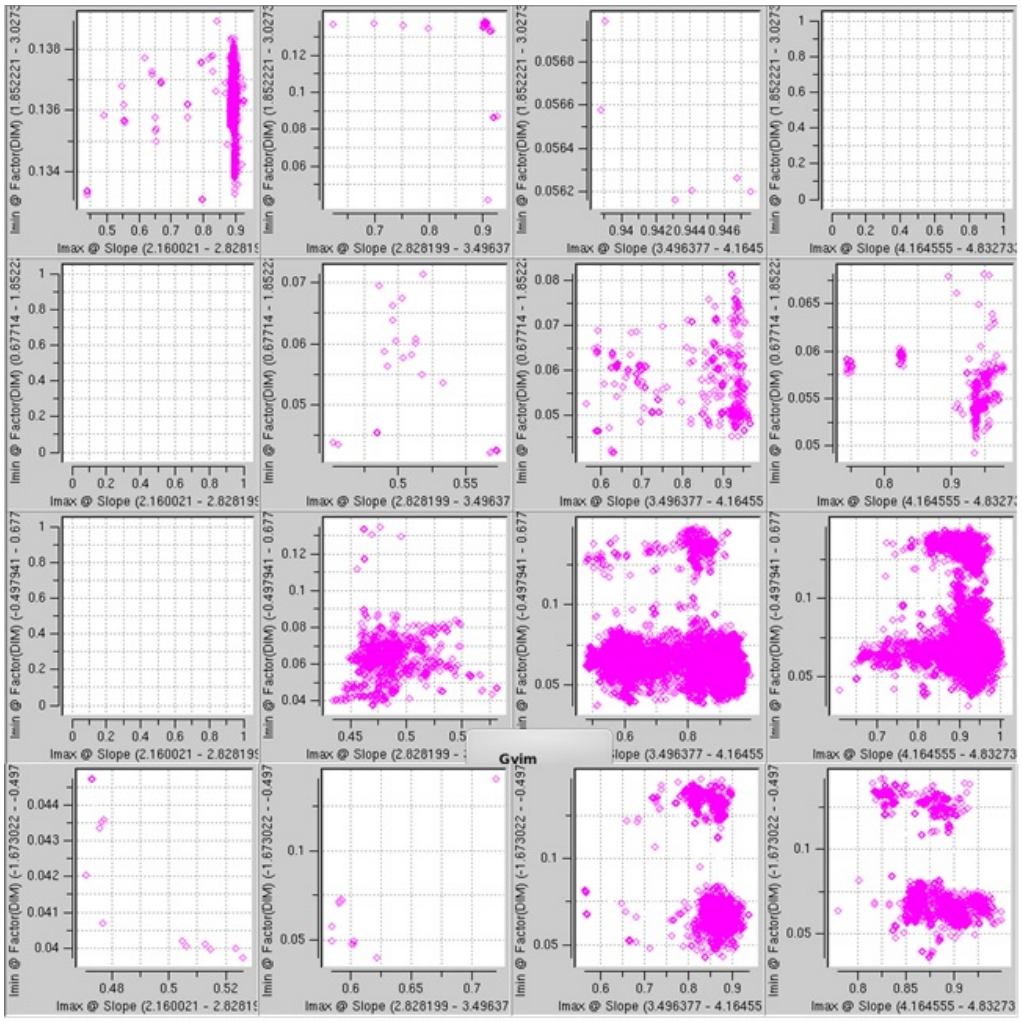

Figure 5.2: Full Chip Image Parameter Coverage Analysis Checker Board with Artefacts Included

Each of the pink diamonds represents set of the image parameters of a fragment on the full chip. The total count of the pink diamonds in Figure 5.2 is larger the

green triangles in Figure 5.1. For the full chip image parameter analysis with the artefact fragments included, the factor spans the range -1.673022 to 3.027302. The slope spans the range 2.16 to 4.83. The I_{min} spans the range 0.031988 to 0.147573. The I_{max} spans the range 0.433939 to 1.002772. The majority of the fragments are located in the third and fourth row from the top of the graph particularly in the third and fourth columns.

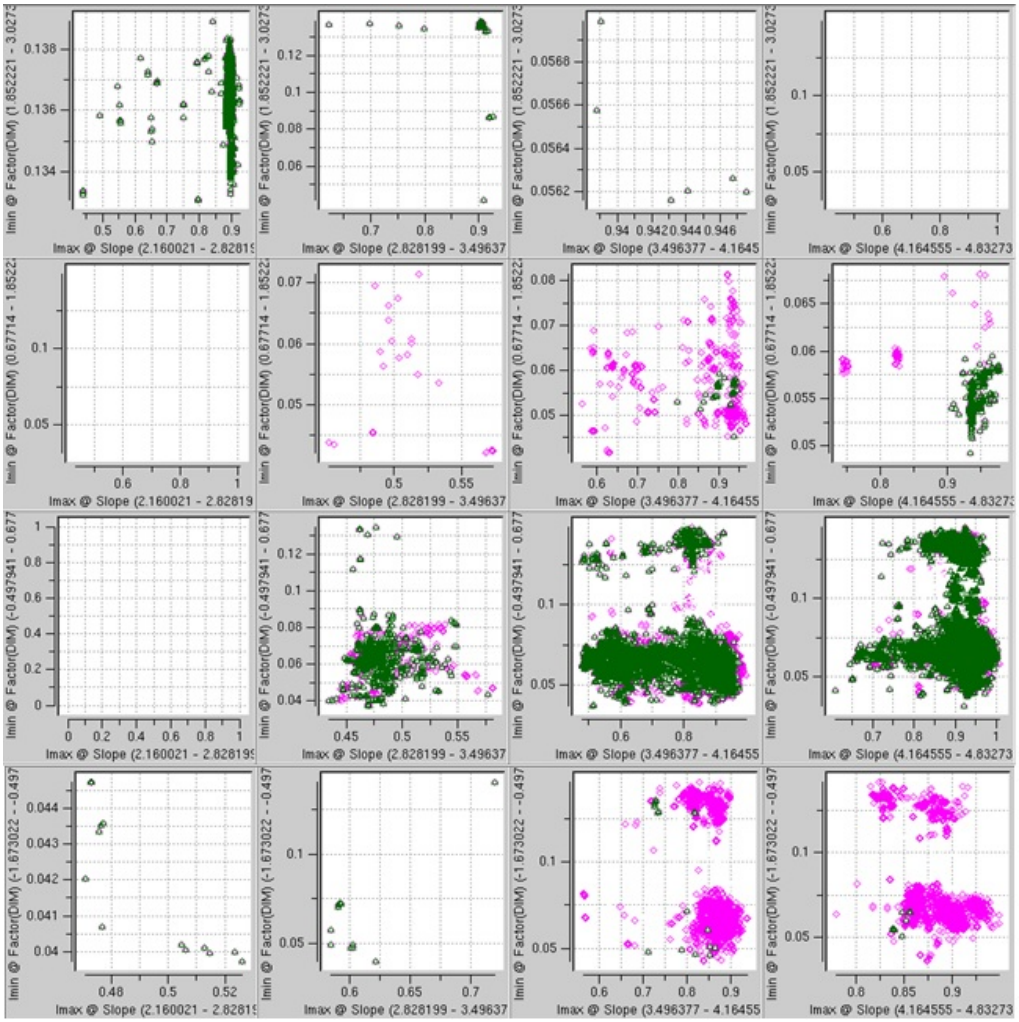

Figure 5.3: Full Chip Image Parameter Coverage Analysis Checker Board without and with the artefacts removal

In Figure 5.3, The overlay between the two graphs is presented. The green triangles represent the full chip without artefacts and the pink diamonds represent the full chip with the artefacts. Differences in the distribution for the fourth row where the factor varies from -1.67 to -0.47 and the slope varies from 3.496 to 4.832

is evident.

By examining the different locations where the distribution differs as shown in Figure 5.4, the feature drawn in blue is the target pre-OPC and the red contour is the simulated contour post OPC, and the black line is the site where the image is evaluated. The site is not normal to the image profile. This means that slope, I_{min}, I_{max} and factor evaluated for this site are dependent on the angle of the site to the contour. In our sample plan selection, artefacts are discarded.

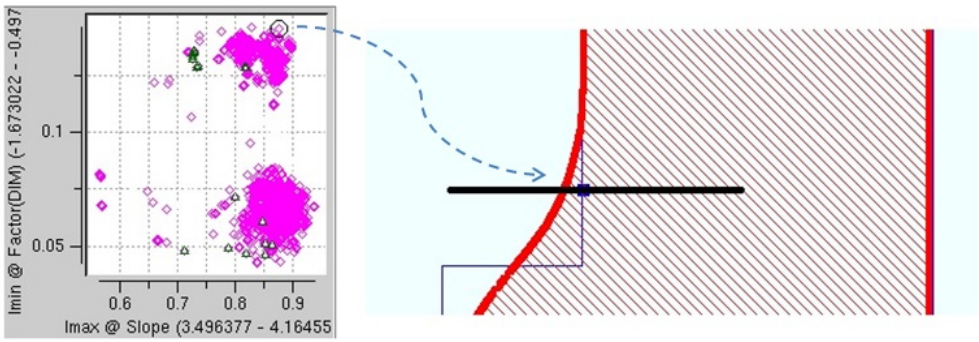

Figure 5.4: A concave corner Fragment, where the feature in blue is the target pre-OPC and the red is the simulated contour post OPC, and the black line refers to the site where the image is evaluated.

In Figure 5.3, the difference are located in the fourth row the last two graphs where the factor varies from -1.67 to -0.47 and the slope varies from 3.496 to 4.832. These fragments belong mainly to corners and jogs. The C-LAPI developed code manages the removal of those corners and jogs (artefacts) and keeps other important 2D structures such as line ends and space ends.

5.3 Test pattern Mask Generation

The test pattern generation flow Section 4.3 shown in Figure 4.4 is implemented. The major steps are explained in the coming sections.

5.3.1 Flow Requirements

Firstly, the flow requirements are identified as follows, the allocated mask area is around 2mm x 2mm ($4mm^2$). Minimum pitch is 300nm. Label sizes and markers dimension and distance to the feature to measure is determined. The feature size start to end is about 7 microns, and the distance to the next structure is about 7 microns.

5.3.2 Patterns Definition

This step is used to determine the patterns that are used in the test pattern mask. The patterns are determined based on two main factors. Firstly, structures are characterized as measurable patterns using a SEM tool, and widely adopted by the industry as modelling test patterns. Secondly, ensures that the test patterns are covering the full chip image parameter space.

200 seed structures are used as a probe for the test pattern definition. Seed patterns that cover the full chip image parameter space are determined. The seed test patterns contain the following basic structures as listed in Table 5.1.

To determine the required seed structures to use, seed structures sets of image parameters is calculated. Seed structures sets of image parameters are overlapped with full chip sets of image parameters as depicted in Figure 5.5. The green triangles represent the full chip image parameters, and the red circles represent the image parameters of the seed test patterns used.

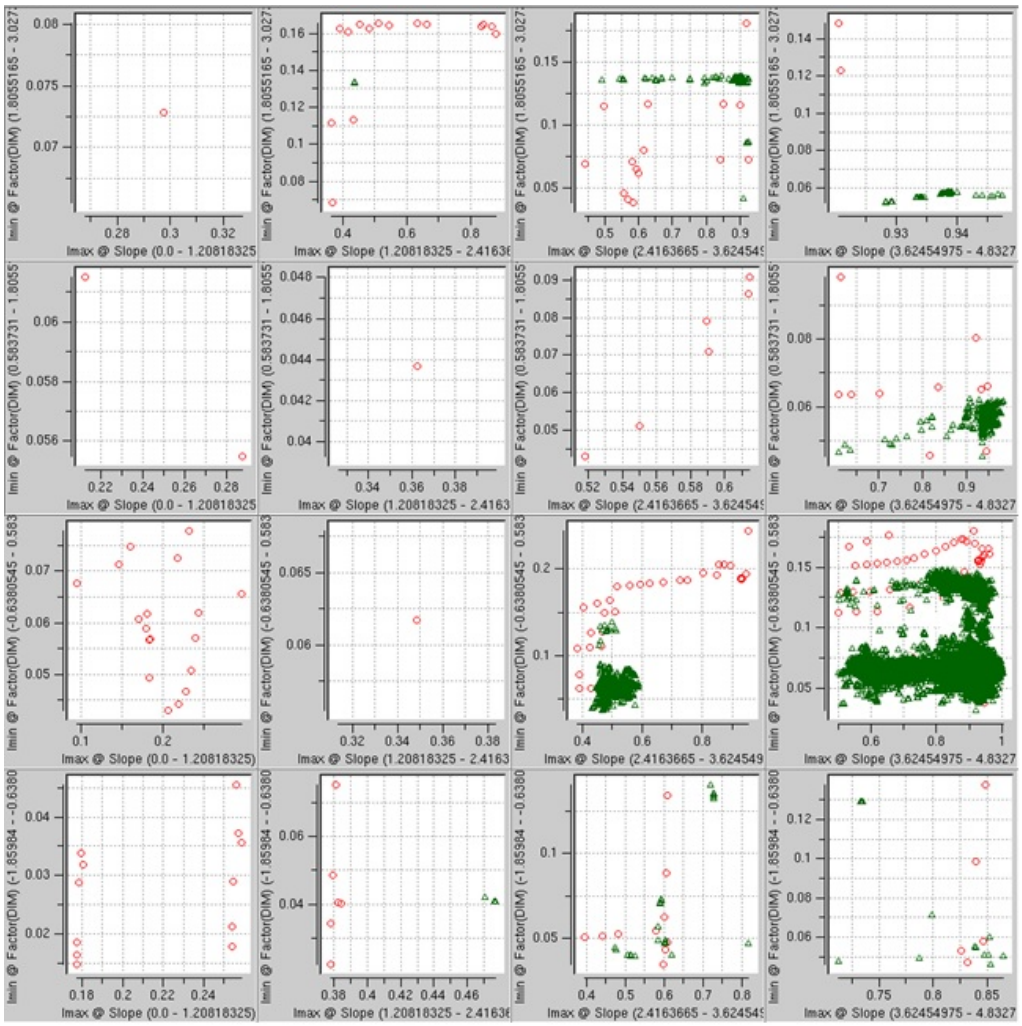

Figure 5.5: Seed test patterns image parameters overlay with the full chip image parameter space

Seed patterns image parameters are far from the full chip fragments image parameters, however, seed patterns sets of image parameter are covering a larger extent of the full chip image parameters space. Although those patterns represent the basic patterns that could be measured easily and used widely in modelling they are not close to most of the full chip image parameters fragments.

Table 5.1: List of Seed Structures

Pitch
Inverse pitch
Isolated line
Inverse isolated line
Isolated line between pads
T Structure
Line end
Inverse line end
Inverse dense line end
Dense line end
Broken H
H
Pitch line end
Rectangle
Inverse Rectangle

To define the set of seed test patterns needed, the graph in Figure 5.5 is re-drawn after classifying the space into three main regions as shown in Figure 5.6. Each of these three regions is defined based on their image parameters and the presence of full chip sets of image parameters in those regions.

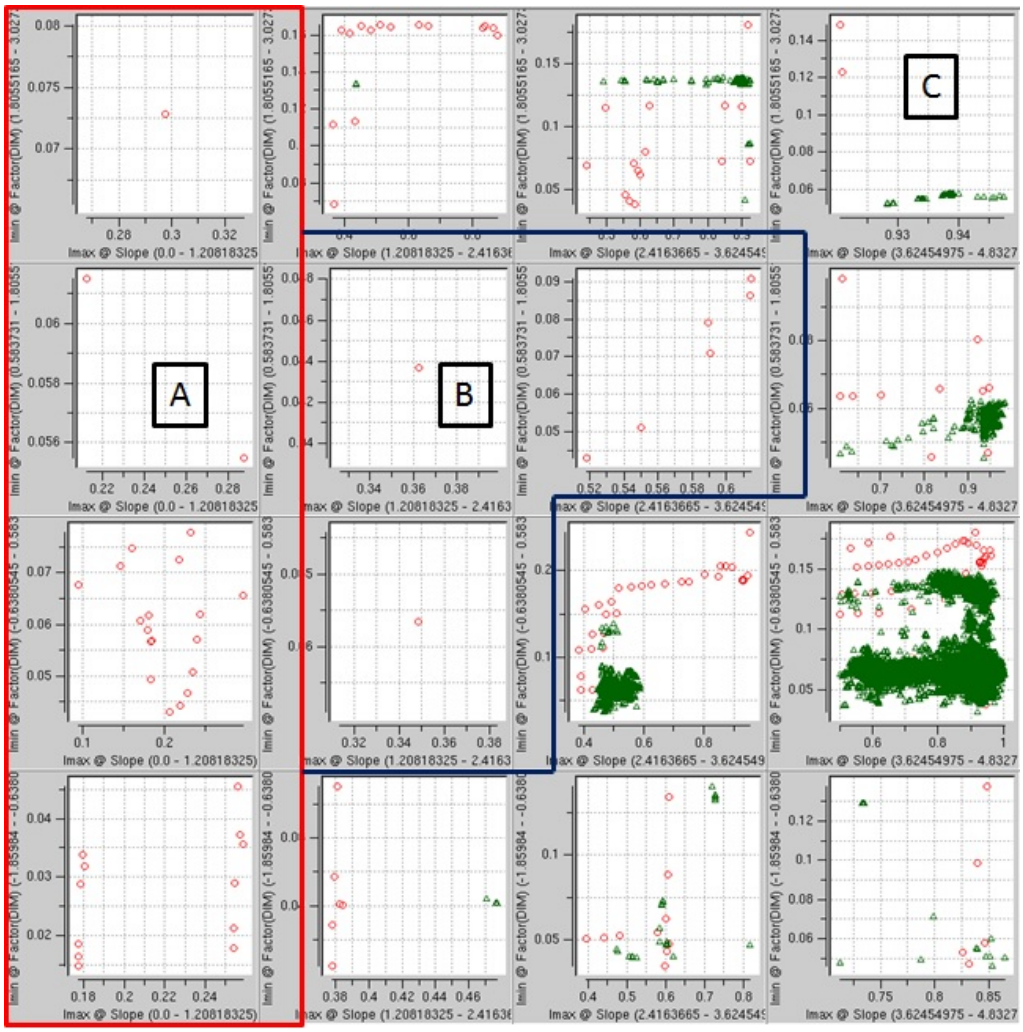

Figure 5.6: Classified Seed Test Patterns Image Parameters Overlay with the Full Chip Image Parameters Space

a) Region A

Region A is characterized by slope ranging from zero to 1.208 and factor from -1.85 to 3.027. This region only contains seed test patterns and no full chip fragments are located in that area. Also I_{max} in this region is less than the model threshold.

b) Region B

Region B is does not show any common overlap with the full chip fragments image parameters and the seed test patterns image parameters. No valuable information is found in that region.

c) Region C

A large count of seed test patterns and full chip fragments in that region. Analysis of each row in region C is done to find the basic seed patterns.

In row 4 factor between -1.859 and -0.638, and slope varying from 1.208 to 2.416. Examining the seed structures in that region it was found that the H type structure is the closest in the image parameter domain to the full chip sets of image parameter as shown in the Figure 5.7. Each checker board box shown in Figure 5.7 has a corresponding H structure below. The below H structure is the closest structure found in the seed patterns to the full chip image parameter in that checker board box. For each H structure there is a red gauge locating where the image parameters are evaluated. As the slope increases, moving from the left to the right, the main difference in the H structures is the dimensions of the H structures as shown in Figure 5.8.

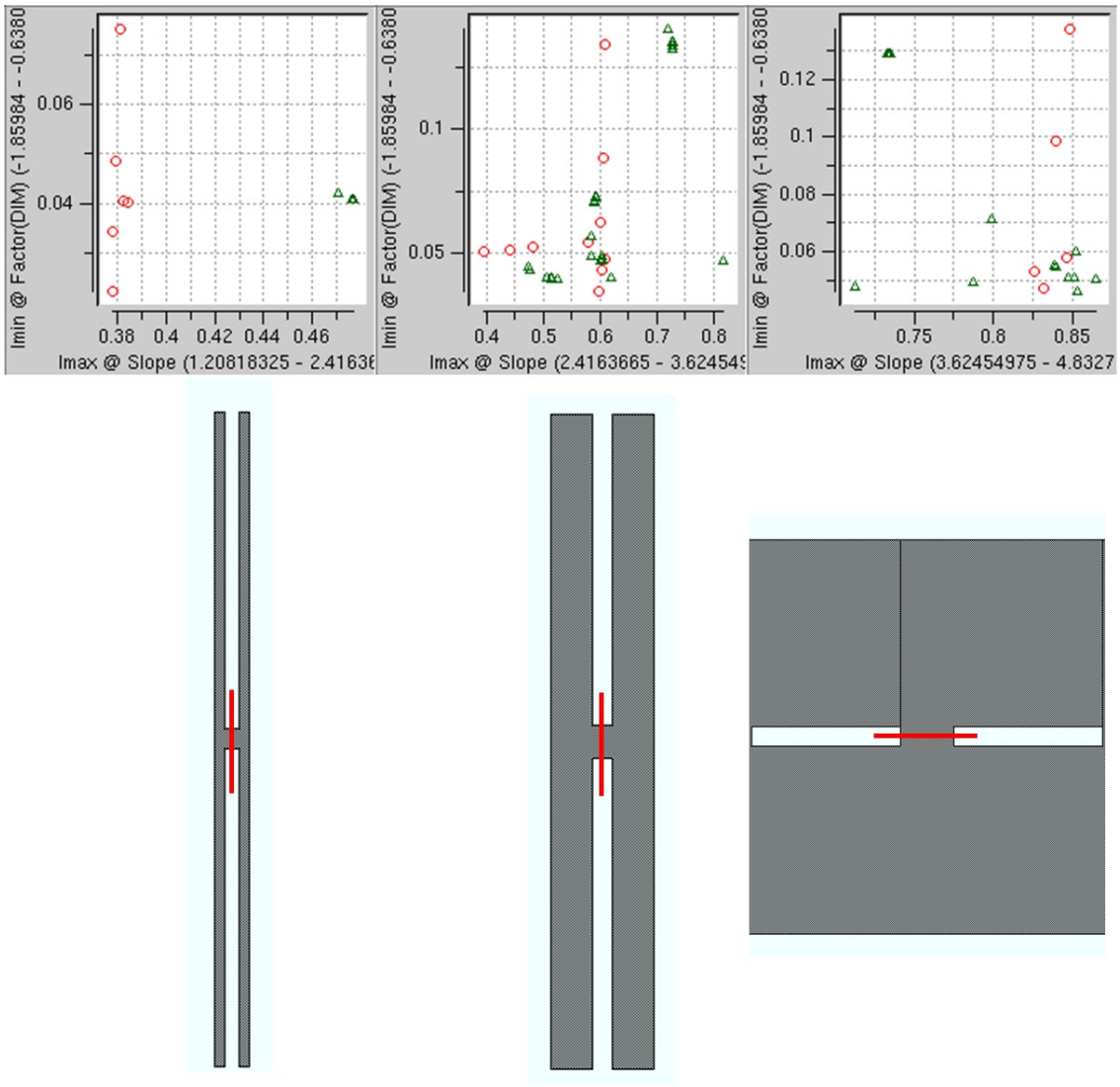

Figure 5.7: Row 4, seed test pattern versus full chip fragments image parameter analysis. The green triangles are the full chip fragments and the red circles are the seed test patterns. The closest seed test patterns structure to the full chip in the image parameters space is the H shape shown below the checker board box. The red gauge represents where the image parameters are evaluated and where the SEM measurements is performed.

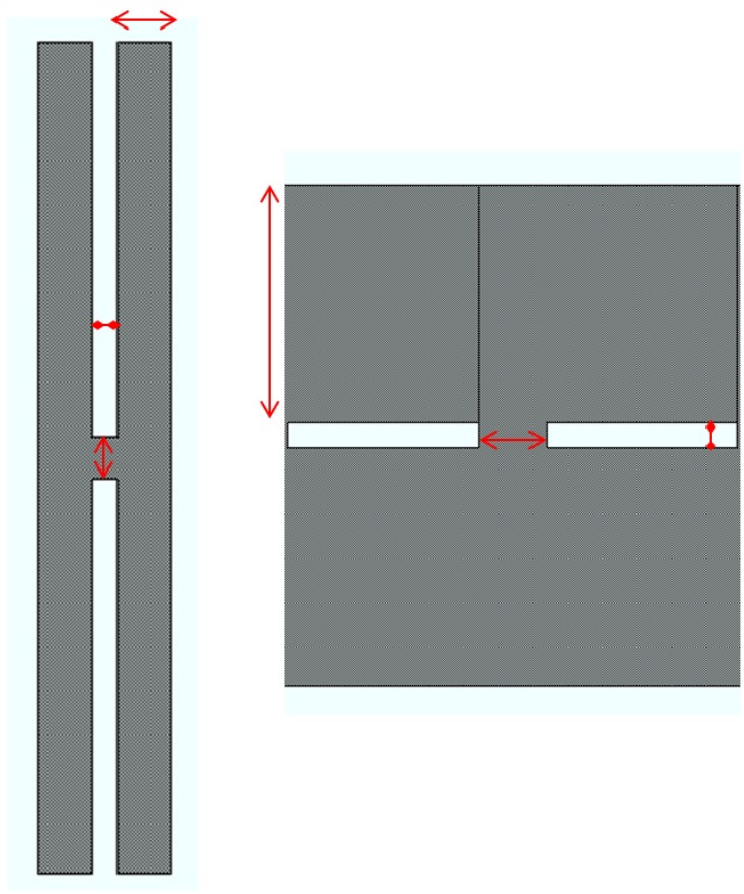

Figure 5.8: H Structure Geometrical Difference, with the variation in H structure dimensions the image parameters evaluated for the seed patterns varies.

Row 3 is characterized by a factor ranging from -0.638 to 0.583 and slope varying from 2.416 to 4.8327. Examining the seed structure in that region, it is found that a large set of structures is located in that region including the isolated line, pitch, inverse isolated line, line end for large width lines, wide broken H structures, wide H structures, and finally T structures as shown in Figure 5.9. Wide structures refer to any edge with length more than 600nm.

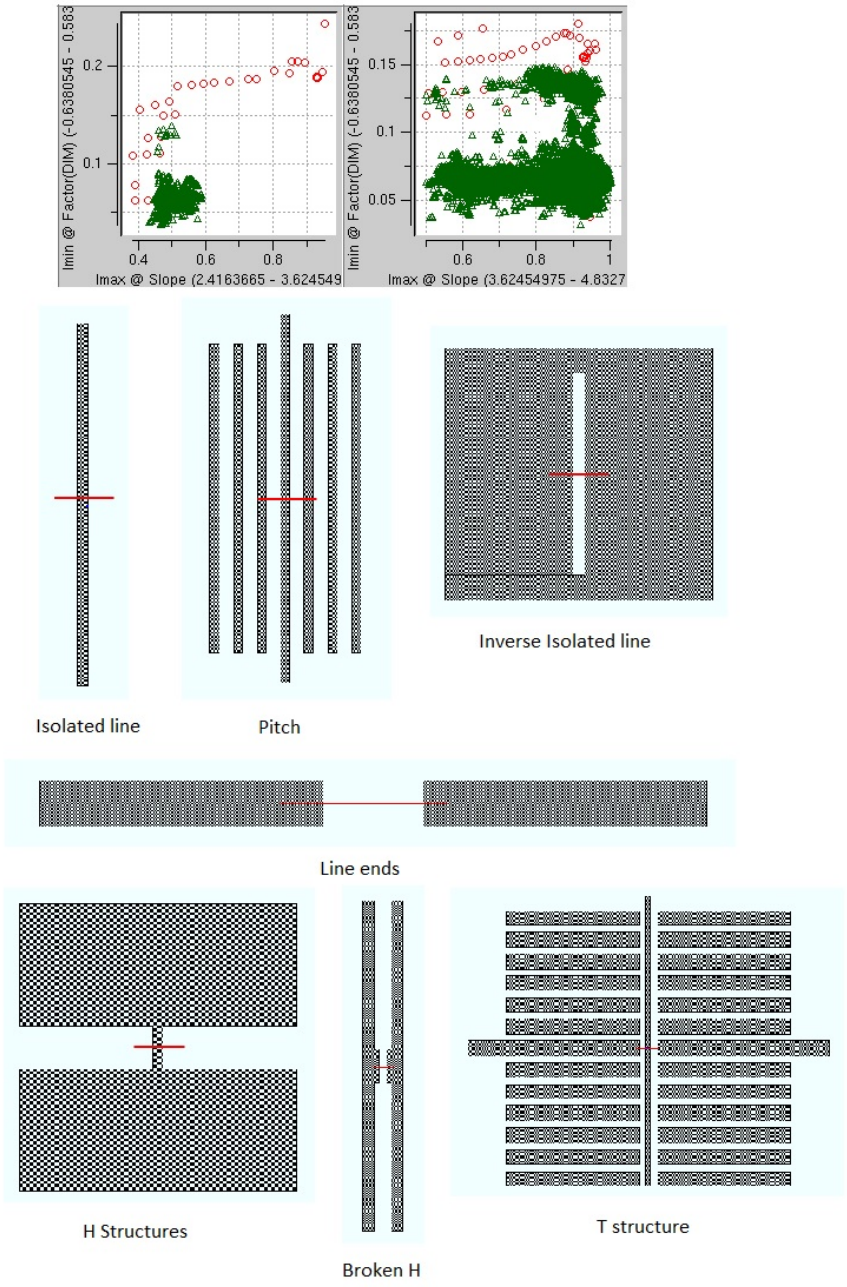

Figure 5.9: Row 3, Seed test pattern versus full chip fragments image parameters analysis, where the green triangles are the full chip fragments and the red circles are the seed test patterns. The closest seed patterns to the full chip in the image parameters space is the shown below the checker board boxes. The red gauge represents where the image parameters are evaluated and the measurements will be collected. The closest structures are isolated line, pitch, inverse isolated line, wide line ends, wide H structures, Broken H, and T structures.

Moving up in Figure 5.6, region C row 2 is characterized by factor ranging from 0.583 to 1.805 and slope varying from 3.62 to 4.8327. By examination of the seed structure in that region line ends are found. The isolated line end is present in that region as shown in Figure 5.10.

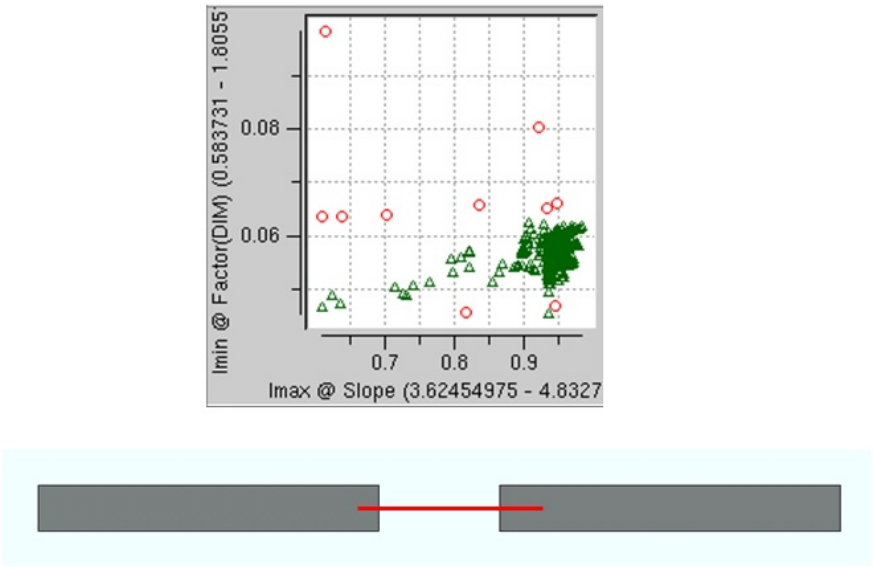

Figure 5.10: Row 2, Seed test pattern versus full chip fragments image parameters analysis, where the green triangles are the full chip fragments and the red circles are the seed test patterns. The closest seed patterns to the full chip in the image parameters space is the shown below the checker board boxes which is isolated line ends. The red gauge represents where the image parameters are evaluated and the measurements will be collected.

Moving to the last row at the top of Figure 5.6, row 1 is characterized by factor ranging from 1.805 to 3.027 and slope varying from 1.208 to 4.8327. Examining the seed structure in that region it was found that mainly it can be represented by line ends, pitch line ends, dense line ends as shown in Figure 5.11.

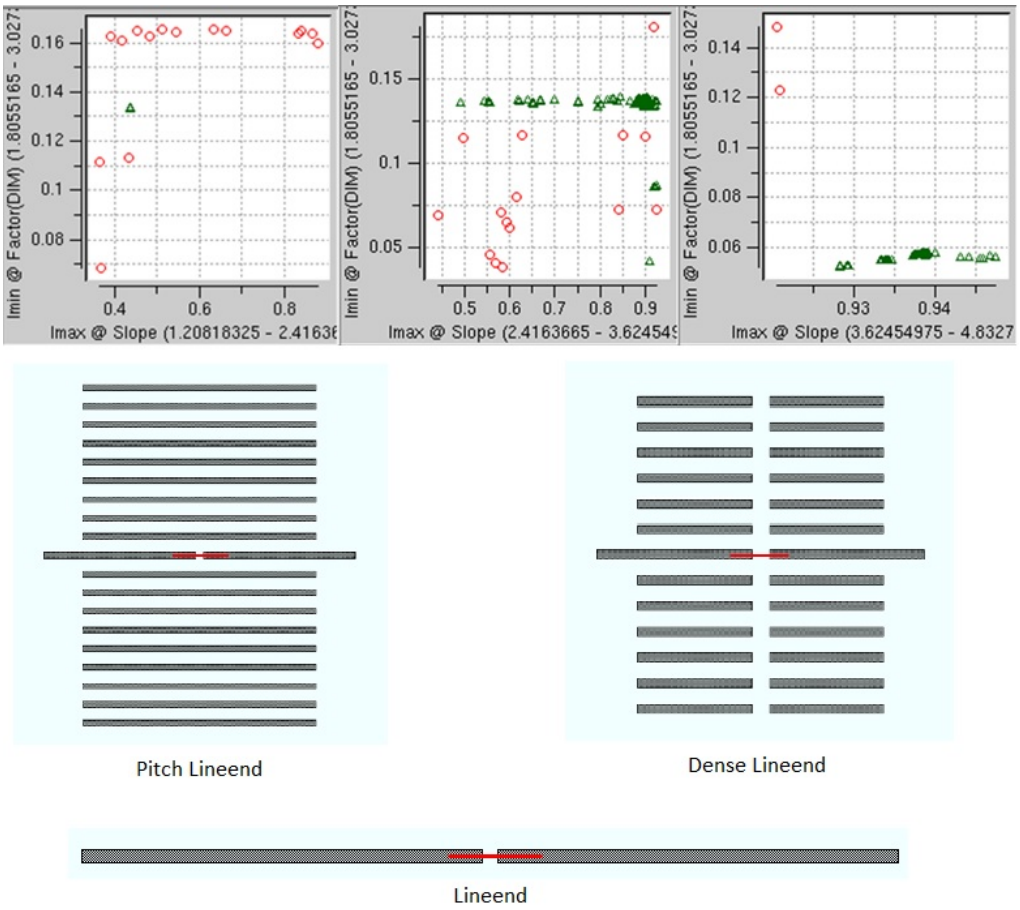

Figure 5.11: Row 1, Seed test pattern Vs full chip fragments image parameters analysis, where the green triangles are the full chip fragments and the red circles are the seed test patterns.The closest seed patterns to the full chip in the image parameters space is the shown below the checker board boxes. The red gauge represents where the image parameters are evaluated and the measurements will be collected. This figure contains the closest structure to the full chip fragments which are line ends, pitch line ends, and dense line ends.

The seed structures are identified. These seed structures will be placed on the mask varying the dimension of the feature, spacing between the features, count of the features for a given structure, with and without OPC. Mask floor-planning is done. In this step each structure is allocated certain area of the total area of the mask as explained in Section 4.3.

5.3.2.1 Discussion

Region A seed test patterns are structures that are below the resolution limit. I_{max} less than the threshold means that these structures fail to print. These structures are expected to fail to print on wafer as well. If these structures failed to print on wafer, no SEM measurements are available and they can not be used in model calibration. However these structures are useful in model verification to make sure that the model does not simulate those structures as printing structures.

In Figure 5.7, the orientation of the H structure differ by 90 degree. This illumination is annular source which has symmetry in X and Y direction and has symmetry in diagonal hence no differences is expected in the image parameters due to the orientation change as well. In case of asymmetric source orientation need to be considered. For example dipole sources.

Variation in the dimensions of each of the seed structures changes the image parameters evaluated at the SEM measurement location. Large span of variations improves the full chip image parameter coverage by the modelling test patterns. Variation in the seed test patterns helps in avoiding the need for complex test patterns for model calibration.

5.3.3 Test Pattern Compilation

A Tcl utility that compiles each group of structures are generated into a layout. These layouts are placed easily into a combined file.

5.3.4 Test Pattern Placement

Calibre®Workbench is used as a layout editor combining each of the generated layouts. Each layout is placed into its planned location in the final mask.

5.3.5 Mask Review Process

After approximately 17000 test structures are placed on the mask area, the mask is ready for tape-out. The final review is done. The final review stage is the calculation of the image parameters of the 17000 test pattern structures, Then the evaluated test pattern mask is overlapped with the full chip fragments image parameters.

As shown in Figure 5.12, The test pattern mask extents a larger domain compared to the full chip fragments image parameters. The green triangles represent the test pattern structures and the pink diamonds under represent the full chip fragments image parameters. Ranges of each of the image parameter is shown in Table 5.2.

Table 5.2: Image Parameter Coverage Range Comparison Between Full Chip and Test Patterns Mask

	Factor		I_{min}		I_{max}		Slope	
	max	min	max	min	max	min	max	min
Full Chip	3.027	-1.673	0.148	0.032	1.003	0.434	4.83	2.16
Test Patterns	3.264	-1.982	0.517	0.021	1.026	0.080	4.852	0

5.3.5.1 Discussion

The ranges are not sufficient to properly compare the four dimensional arrays. Each point on the charts is represented by four image parameters, so that the checker board in Figure 5.12 is useful. Looking at the first row at the second column in the chart and the fourth row at the third column some locations on full chip are not covered by the heuristic test pattern mask. Those locations are placed in the next test pattern mask.

Also there are discontinuities in the test patterns image parameter space. Some parameters combinations are forbidden. Examples of the forbidden locations in the space, locations where I_{min} is greater than the I_{max} with any slope and factor com-

binations. Also, for printing wide lines slope is characterized to be low. Yet this structure is printing on wafer. Therefore, it is expected that I_{min} and I_{max} are close to each other.

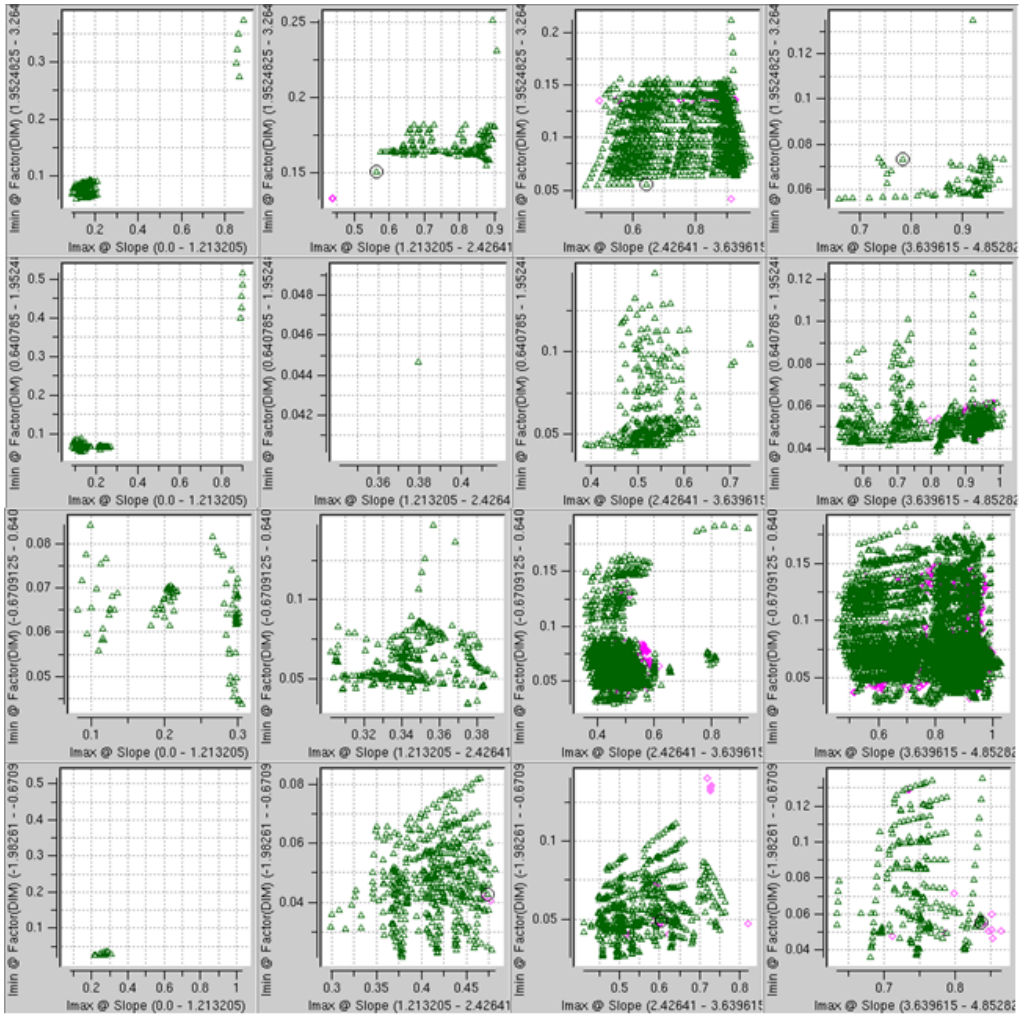

Figure 5.12: Overlay between the full chip and the test pattern mask. The green triangles represent the test pattern mask image parameters and the pink diamonds represent the full chip fragments image parameters.

5.4 Modelling Sample Plan Generation

Recalling the objectives for the sample plan selection in Section 4.4 and shown in Figure 4.5,

1. Selection of the test patterns that covers the full chip fragments post OPC

image parameters domain.

2. Selection of the closest structure to the full chip fragments in the image parameters domain.

3. Generation of a sample plan distribution following the same distribution of the full chip post OPC fragments image parameters.

The flow is performed iteratively to fully cover the image parameter space of the full chip. From the previous sections, Section 5.2 and Section 5.3, the inputs to the flow are ready. In the coming section, 4 iterations are described. New test patterns are added in every iteration to our sample plan to improve the final sample image parameter space coverage.

In Table 5.3, the progress of the coverage of the image parameters ranges is shown. The first row contains the four image parameter ranges for the full chip image parameters space. For the iteration from 1 to 3 of the flow an intermediate sample plan is generated. For each iteration the generated intermediate sample plan is amended to the previous iteration sample plan except the first iteration sample plan. For each generated sample plan the sets of image parameter is calculated. The calculated image parameter range for each intermediate sample plan is represented in Table 5.3 from rows 2 to 4. The last row in Table 5.3 represents the final sample plan image parameter ranges.

Table 5.3: Progress of the Image Parameter Ranges for Each Iteration of the Flow

	Factor		I_{min}		I_{max}		Slope	
	max	min	max	min	max	min	max	min
Full Chip	3.027	-1.673	0.148	0.032	1.003	0.434	4.83	2.16
1st Iteration Sample Plan	2.789	-1.490	0.152	0.038	1.008	0.443	4.665	2.584
2nd Iteration Sample Plan	2.789	-1.543	0.155	0.035	1.008	0.419	4.665	2.584
3rd Iteration Sample Plan	2.789	-1.543	0.155	0.030	1.008	0.419	4.795	2.559
4th Iteration Final Sample Plan	2.793	-1.543	0.155	0.030	1.008	0.419	4.795	2.559

In Table 5.3 ranges are shown. However, the checker board contains more information regarding the selection data density. In Figure 5.13, the blue circles represent that full chip fragments post OPC image parameters and the green triangles represent the image parameters of the selected test patterns for the first iteration. Figures 5.14, 5.15, and 5.16 represent the sample plan image parameter space for each of the second, third, and fourth iteration, respectively. In each graph, The blue circles represent that full chip fragments post OPC image parameters and the green triangles and pink diamonds represent the image parameters of the selected test patterns from this iteration. The green triangles represent the previous iteration sample plan image parameter, and the pink diamonds represent the added test patterns structures to the sample plan image parameter for this iteration.

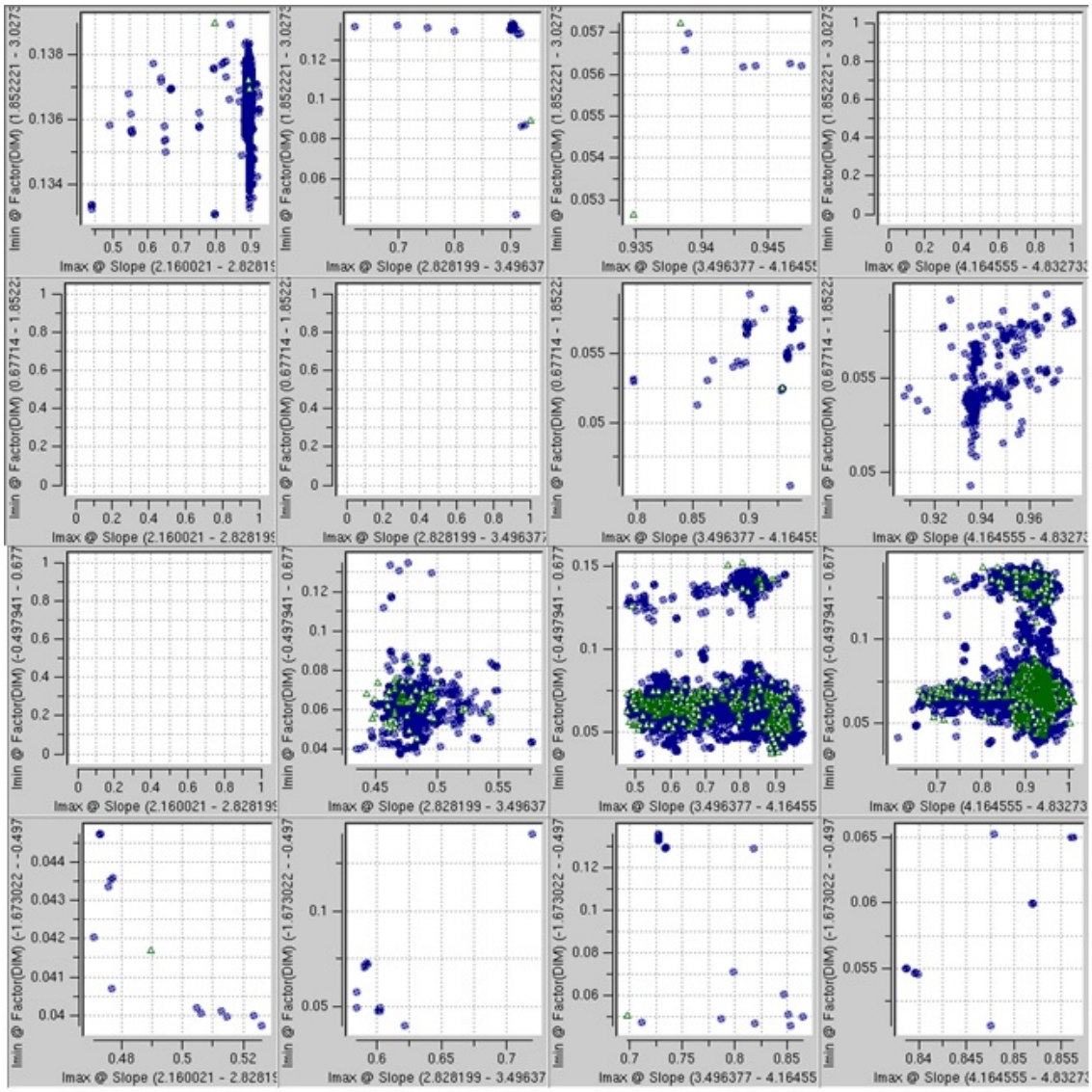

Figure 5.13: First iteration over lap between the selected sample plan and the full chip. The blue circles represent the full chip and the green triangles represent the test patterns image parameter.

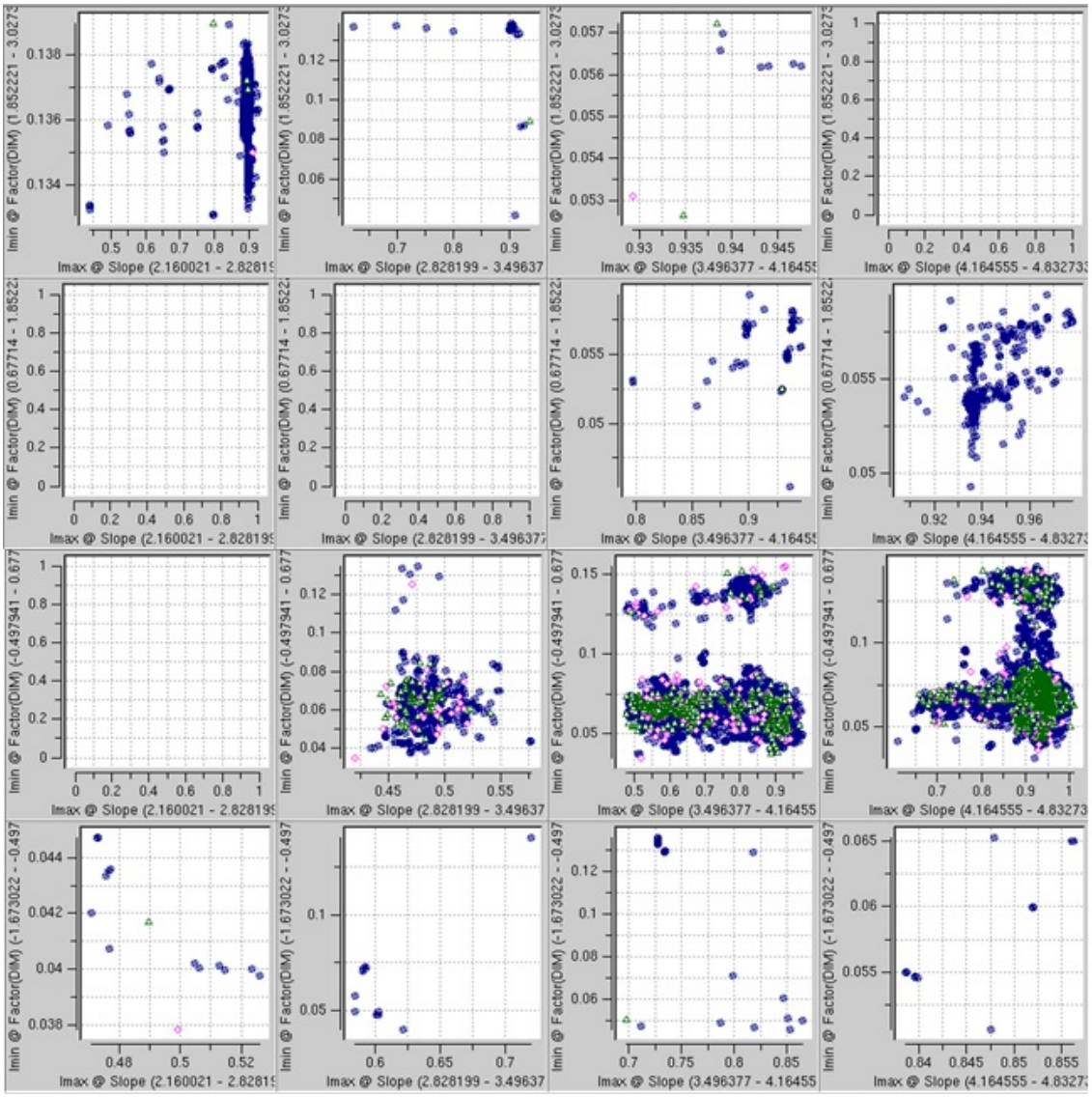

Figure 5.14: Second iteration overlap between the selected sample plan and the full chip. The blue circles represent the full chip and the green triangles represent the first test patterns image parameters. The pink diamonds represent the added structures from the second iteration test patterns image parameter.

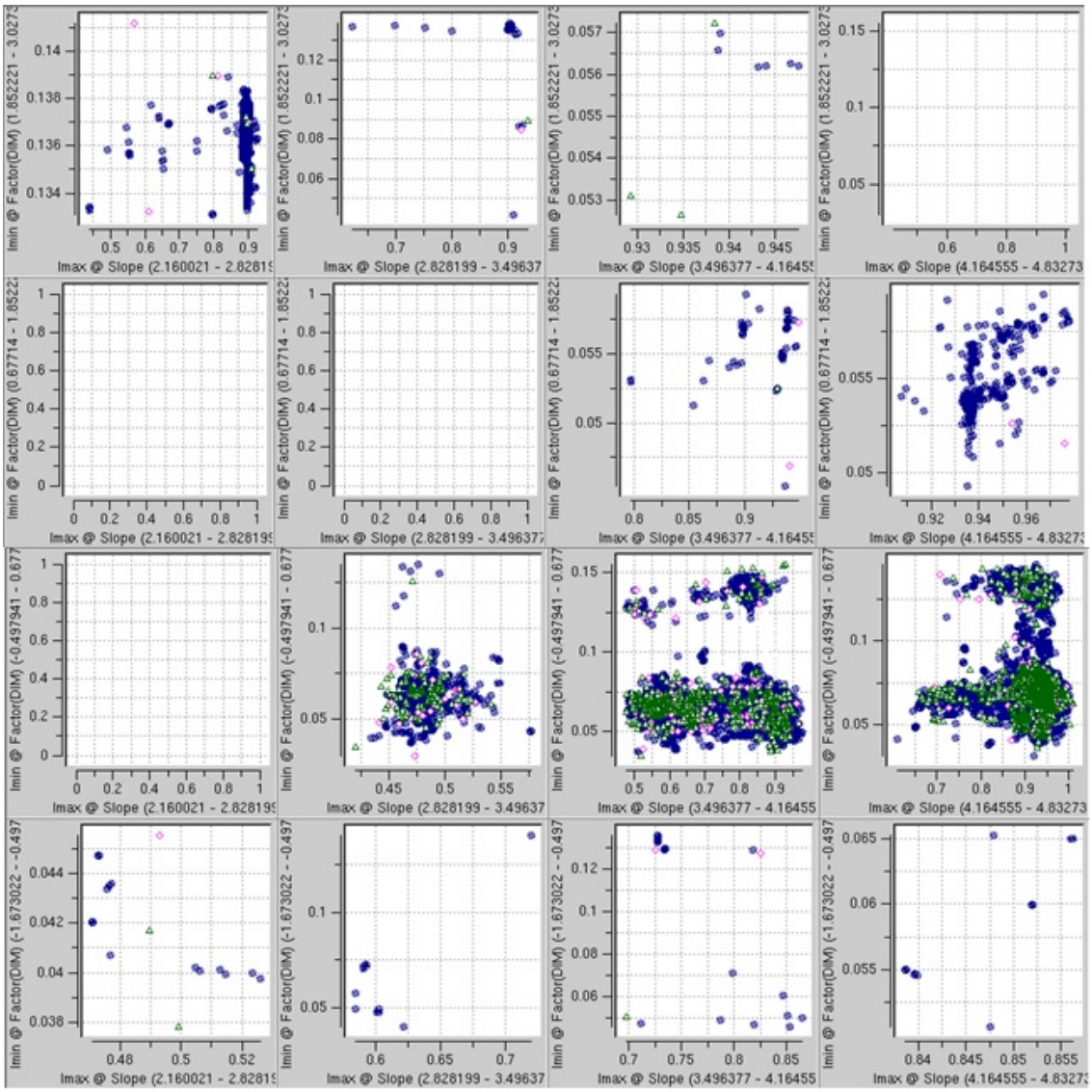

Figure 5.15: Third iteration overlap between the selected sample plan and the full chip. The blue circles represent the full chip and the green triangles represent the first and second iteration selected test patterns image parameter. The pink diamonds represent the added structures from the third iteration test patterns image parameter.

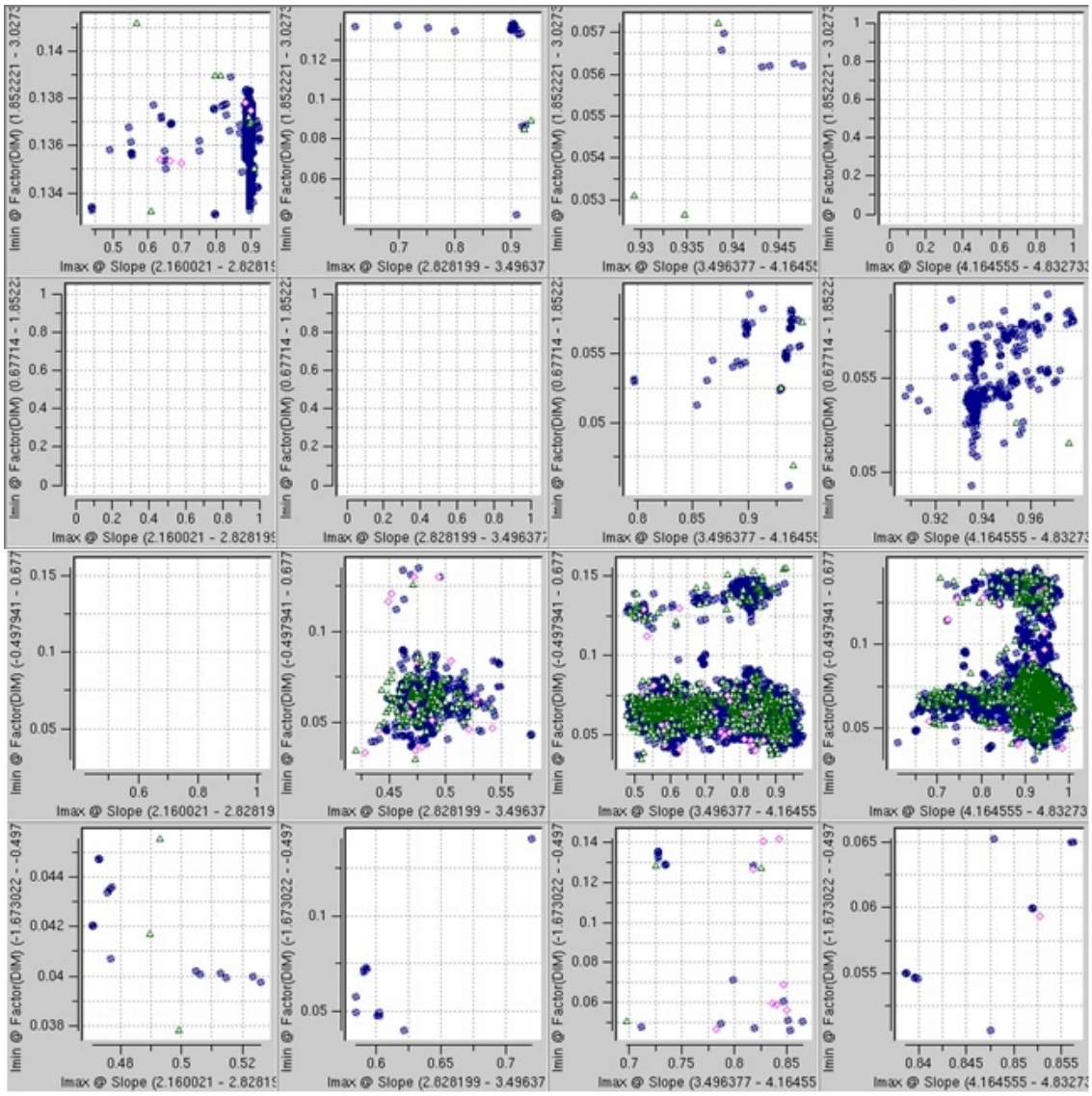

Figure 5.16: Fourth iteration over lap between the selected sample plan and the full chip. The blue circles represent the full chip and the green triangles represent the first, second and third iteration selected test patterns image parameter. The pink diamonds represent the added structures from the fourth iteration test patterns image parameter

The distance metric is the maximum space distance between the full chip and the test pattern in the image parameters space. The distance metric is expected to be small at the first iteration and increases as we move to the final iteration to increase the search range for the location on the full chip. This increase in the distance metric helps in improving the full chip coverage. The maximum allowed distance metric for the first iteration is 0.047002. For the second, third, and fourth

iterations, the maximum allowed distance metric is 0.077514, 0.14562, and 0.289015, respectively.

In Tables 5.4 types and count of the selected structures is shown. In the second column the first iteration intermediate sample plan count is shown. The total count of the selected test patterns from the first iteration is 824 test patterns. After the second iteration the total count of the selected structures from the first and second iteration is 1150 test pattern structures. The second iteration adds 326 test patterns. For the third iteration, the total count of the selected structures from the first three iterations is 1363 test patterns. The third iteration adds 213 test patterns. Finally, After the fourth iterations the total size of the sample plan is 1499. The fourth iteration adds 136 test patterns.

5.4.1 Discussion

In Figure 5.13, the selected test patterns are following the full chip density in the image parameter space. In the first iteration majority of the selected test patterns are located between factor values of -0.497 and 0.677, and slope values of 2.82 and 3.496. This region corresponds to the high density region of the full chip image parameter space. Majority of the selected test patterns are wide (edge length ¿ 600nm) structures that resembles a 1D pattern. This corresponds nature of the full chip since this layer is a line/space layer, it is expected that the majority of the full chip fragments are 1D.

In Figures 5.14,5.15, and 5.16, in each of these figures the pink diamonds represents the added test patterns to the sample plan. The pink diamonds scatter across the graph. The added test patterns image parameters are following the full chip density. The selection of the test patterns is guided by the density of the full chip image parameter space density. Test patterns close to the full chip in the image parameter space has higher priority to be in the sample plan. This priority improves the model prediction of the real full chip patterns in production.

In Table 5.3, the fourth row range is almost covering the full chip image param-

Table 5.4: List of the Types of the Structures in the Final Sample plan. Each Iteration added test Patterns is Listed.

	1^{st} Iteration	2^{nd} Iteration	3^{rd} Iteration	4^{th} Iteration	Sample Plan
Pitch	150	65	50	15	280
Inverse Pitch	53	22	12	8	95
Isolated Line	12	0	1	0	13
Inverse Isolated Line	19	4	1	1	25
Isolated Line Pads	51	25	9	1	86
T Structure	169	81	41	26	317
Line End	101	43	35	23	202
Inverse Line End	11	5	3	6	25
Inverse Dense Line End	20	5	4	12	41
Dense Line End	57	15	13	11	96
Broken H	96	35	21	11	163
H Structure	17	7	8	11	43
Pitch Line End	49	15	13	9	86
Rectangle	19	4	2	2	27
Inverse Rectange	0	0	0	0	0
Total	824	326	213	136	1499

eter space. The deficiency in the coverage of the sample plan is coming from two reasons. Firstly, the selection is based on the distance metric some locations could not find a close test pattern in the maximum allowed distance metric. This can be resolved by having an extra iterations to find the closest match. This will increase the sample plan size to gain more accuracy for the model. Secondly, the test pattern mask shortage at image parameter space explained in test pattern mask generation. Those patterns are required to be added in the next test pattern mask.

To show the progress of the selection of the test patterns between I_{min} and I_{max} relationship between the selected test patterns and the full chip post OPC fragments is shown in the rotated Figure 5.17. Each of these graphs represents the I_{min} on the y-axis and the I_{max} on the x-axis. The blue dots represent the full chip post OPC fragments image parameters values for the I_{min} and I_{max}. For the first graph the green triangles represent the test patterns selected in the first iteration. In the second graph the green triangles represent the selected test patterns image parameters I_{min} and I_{max} from the previous iteration, and the pink diamonds represent the added test patterns from the second iteration. As we proceed to the third and fourth graph the green triangles represent the previous iteration selected test patterns image parameters and the pink diamonds represent the added test patterns from this iteration.

Figure 5.18 showing the progress for the test pattern selection. For each of the graphs the blue dots represent the full chip data, the x-axis represents the I_{max} and the y-axis represents the slope. The graphs are following the same legend as the previous figure.

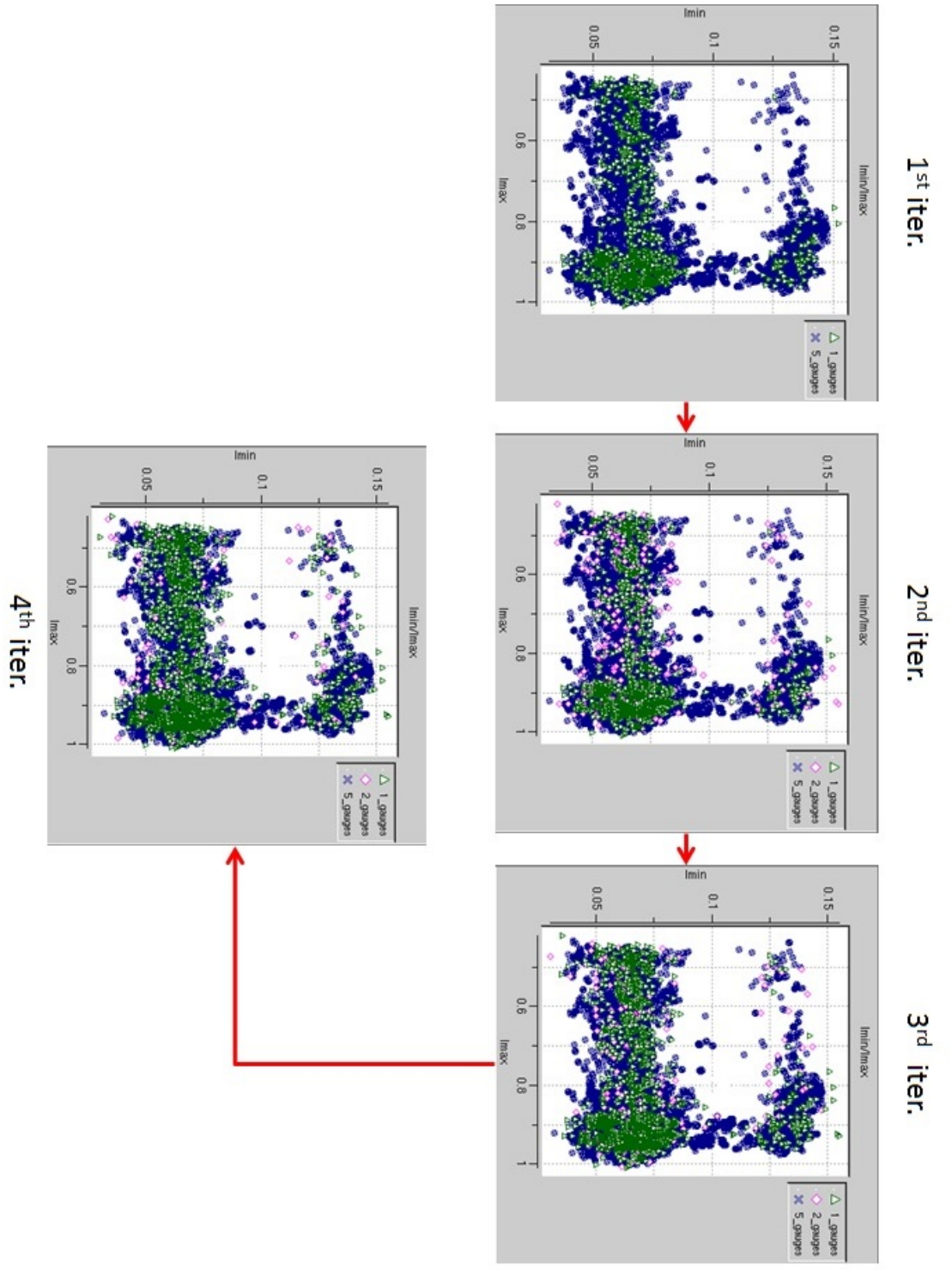

Figure 5.17: The process of test pattern selection. For the first graph the blue dots represent the full chip patterns and the green triangles represent the selected test patterns for the first iteration I_{min} versus I_{max}. The vertical axis represents the I_{min} and the horizontal axis represents the I_{max}. As we proceed to the second iteration the green triangles represent the previous iteration selection and the pink diamonds represent the second iteration added test patterns and so for the third and fourth iteration graph.

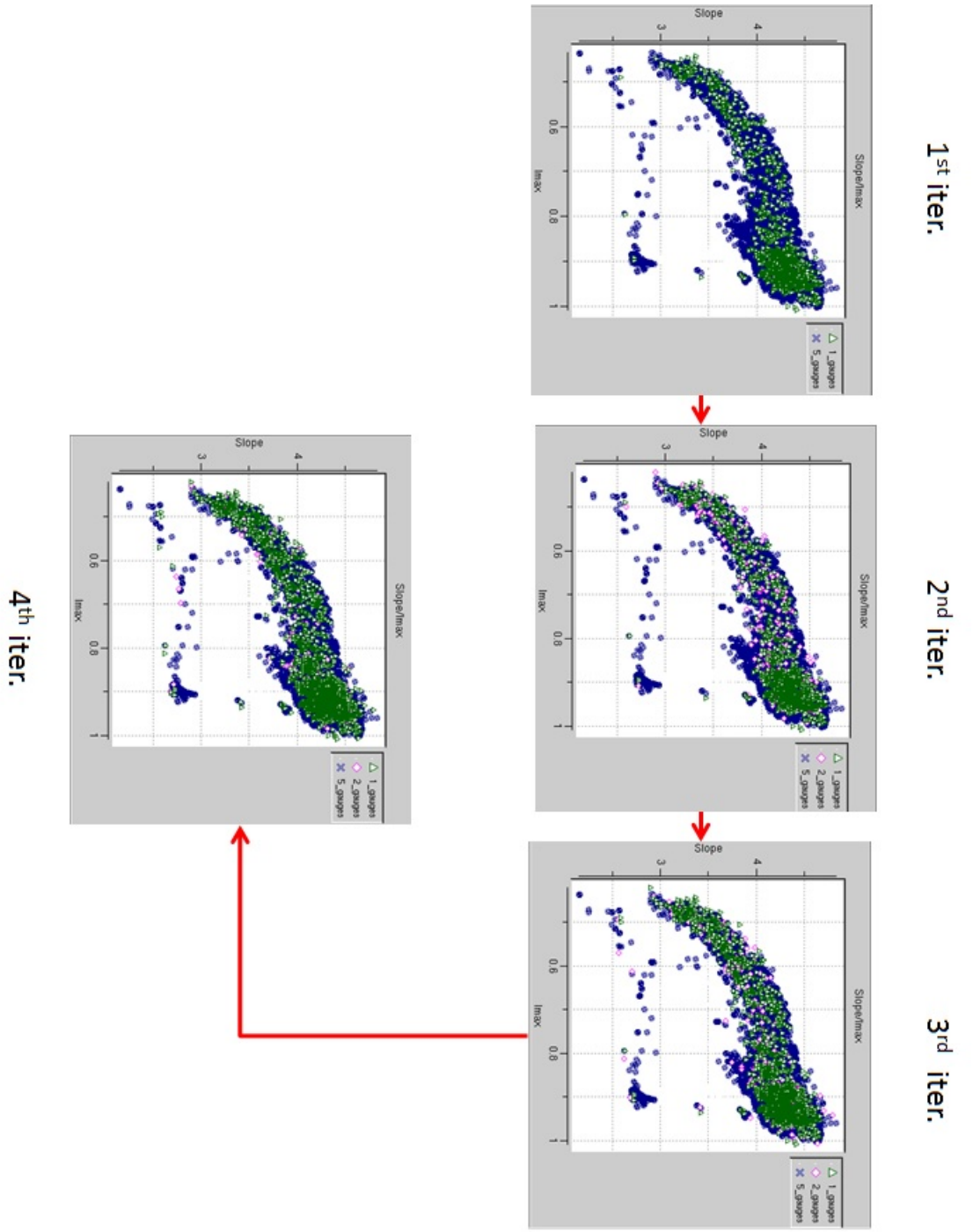

Figure 5.18: Iteration based test patterns structures selection process. For the first graph the blue dots represent the full chip patterns and the green triangles represent the selected test patterns for the first iteration Slope Vs I_{max}. The vertical axis represents the slope and the horizontal axis represents the I_{max}. As we proceed to the second iteration the green triangles represent the previous iteration selection and the pink diamonds represent the second iteration added test patterns and so for the third and fourth graph.

Two observations are made in this discussion, Firstly, the patterns increases progressively to cover the whole full chip image parameter space. The sample plan is selected to enhance the image parameter space coverage of the full chip design. Secondly, the density of the selected test patterns is following the full chip density for both I_{min} versus I_{max} graphs as well as for the slope versus I_{max} graphs, this ensures a good modelling prediction for the critical structures.

This concludes the test pattern selection criteria, by having the final outcome of this step which is a sample plan consisting of 1499 test patterns that fully cover the post OPC full chip fragments. This sample plan is ready to be measured after exposure of the wafer.

5.5 Verification and Comparison

In this section the sample plan is compared to a heuristic sample plan. The verification flow is shown in Figure 5.19. The flow is divided into two branches. Each branch applies to one of the sample plans. Resist model is calibrated using the two calibration sets defined in Table 5.5. Two verification methodologies are used. The first is measurement fitting using the verification set for each sample plan. Also, we added the fitting over the other sample plan as a good model predication criteria. Secondly, Calibre®OPCVerify^{TM}is used to simulate the contours using the two calibrated models. The same full chip mask is used in that stage. The differences in the contour are reported.

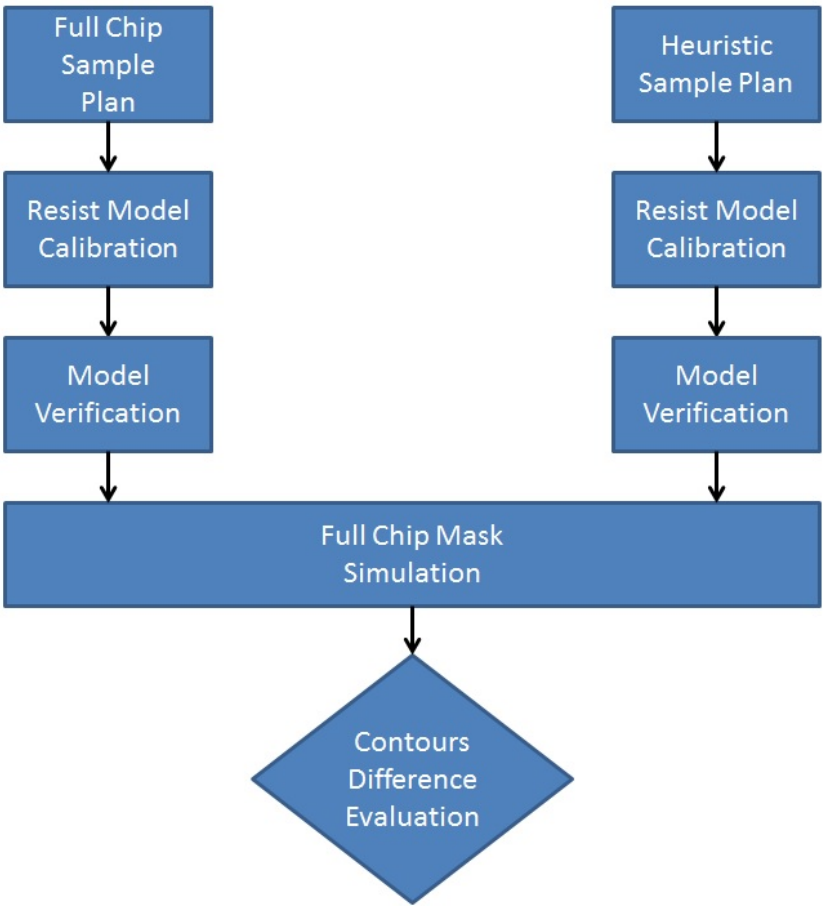

Figure 5.19: Comparison Flow of Models Generated Using the Full Chip Sample Plan and the Heuristic Sample Plan.

For the full chip sample plan, the patterns are divided based on the image parameters into two sets used for calibration and verification following methodology introduced in [36]. The verification set is defined to cover the image parameter domain of the sample plan and surrounded by the calibration point, therefore, maximizing the calibration set points image parameters coverage and optimizing the prediction of the model.

The heuristic data set is divided a calibration and a verification heuristically based on the geometric resemblance of the patterns such that both sets contain the same type of structures. Table 5.5 shows both sample plans sizes, also shows the calibration set and verification sets structure count.

Table 5.5: Table Showing the Count of the Structures for Each Sample Plan

Sample Plan	Calibration count	Verification count	Total Count
Full Chip Sample Plan	900	599	1499
Heuristic Sample Plan	907	620	1527

5.5.1 Stage 1: Model Verification

For the full chip sample plan the model was calibrated using 900 structures and verified using the 599 structures. For the heuristic sample plan the model was calibrated using 907 structures and verified using 620 structures.

Calibre®Workbench™is used as a calibration engine. Models accuracy is measured by the EPE error weighted root mean square which is defined as:

$$errRrms = \sqrt{\frac{\sum W_i (EPE_{sim} - EPE_{meas})^2}{\sum W_i}}$$

where, EPE_{sim} is the simulated EPE to the drawn mask shape, EPE_{meas} is the measured EPE to the drawn mask shape, and W_i is the weight given to each structure during the verification. The weights W_i are set to 1. The smaller the value of the errRrms the better the model predicts the measurements for this sample plan.

Each of the two models are calibrated with the corresponding sample plan. The model calibrated with the full chip Sample plan is verified using the full chip sample plan verification set and the heuristic sample plan as well. The model calibrated with the heuristic sample plan calibration set is verified using the heuristic sample plan verification set and the full chip sample plan as well.

Each of the two models are simulated using both sets. The simulation result is transformed into a normalized errRrms where the 1 is the calibration set errRrms. If the models are good, it is expected that after the normalization that the predicted errRrms is less than or equal to the calibration set errRrms. Otherwise there would be a problem at the model prediction with the higher errRrms. The errRrms is normalized to the errRrms to the calibration set, as the calibration errRrms is the

best achievable errRrms that complies with the specifications.

Table 5.6: Table showing the normalized EPE error weighted root mean square both the model calibrated with the full chip sample plan and the model calibrated with the heuristic sample plan using the full chip sample plan. All the numbers are normalized to the full chip calibration set errRrms to the full chip model

Measurement Set Name	Full Chip Model	Heuristic Model
Full Chip Calibration Set	1	1.125
Full Chip Verification Set	0.8927	0.9627

Table 5.7: Table showing the normalized EPE error weighted root mean square both the model calibrated with the full chip sample plan and the model calibrated with the heuristic sample plan using the full chip sample plan. All the numbers are normalized to the full chip calibration set errRrms to the full chip model

Measurement Set Name	Full Chip Model	Heuristic Model
Heuristic Calibration Set	1.04	1
Heuristic Verification Set	1.076	1.1138

5.5.1.1 Discussion

In Table 5.6, the prediction of the model calibrated with the heuristic sample plan has worse prediction on both the calibration and verification set (extracted form the full chip sample plan) compared to the model calibrated with the full chip sample plan. The model calibrated with the heuristic sample plan has a lower prediction capability when applied to other measurement not used during calibration. The model calibrated with the full chip sample plan shows a good prediction when verified with the verification set extracted from the full chip sample plan.

In Table 5.7, shows that the heuristic model is degraded with respect to the verification set extracted from the heuristic sample plan. Second the model calibrated with the full chip sample plan is showing a good predication over the heuristic sample plan. The model generated using full chip sample plan shows improved model

prediction over structures that are not used in model calibration.

5.5.2 Stage 2: Full Chip Verification

Simulated contours are compared for both models. Simulations are performed using Calibre®OPCVerify™to extract the contours generated by both the resist and the optical models. The same mask shapes are used for both simulations. The used mask is a full chip. The euclidean distance between the contours is calculated. Contour differences is measured at locations separated by 15nm.

The edges are classified into 1D structures and 2D structures. For each type of edges the maximum difference between the contours is classified into buckets. Each of these buckets are represented in a histogram format shown in the next section.

5.5.2.1 Long lines 1D

In Figure 5.20, a histogram shows the contour differences for the 1D edges. The x-axis represents difference values at the contour in um. The y-axis represents the count of the differences in each bucket. The total count is 1872665 differences between 1nm and 3nm. The differences distribution is centred around 2nm value and decreases as we go to the 3nm differences.

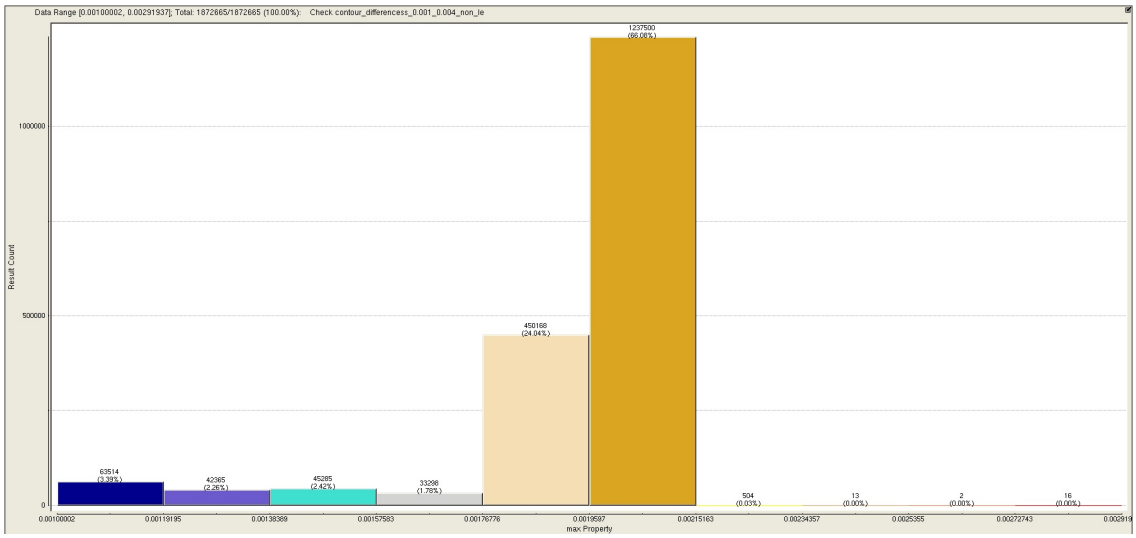

Figure 5.20: A histogram showing the difference between the two contours generated by the two models calibrated for the 1D structures. The x-axis represents the difference between the contour edges at the long lines of the target contour in um. The y-axis represents the count of the differences in each bucket. The differences between the contours is between 1nm to 3nm.

5.5.2.2 Line Ends and Space Ends

For the line ends and space ends, errors are classified them into two categories. Warning level is the differences between 1nm to 4nm. Error level is the differences between 4nm to 8nm. In Figure 5.21 we can see a histogram showing the contour differences at line ends and space ends edges. The x-axis represents difference values at the contour in um. The y-axis represents the count of the differences in each bucket. The total count is 41958 differences between 1 nm and 4 nm.

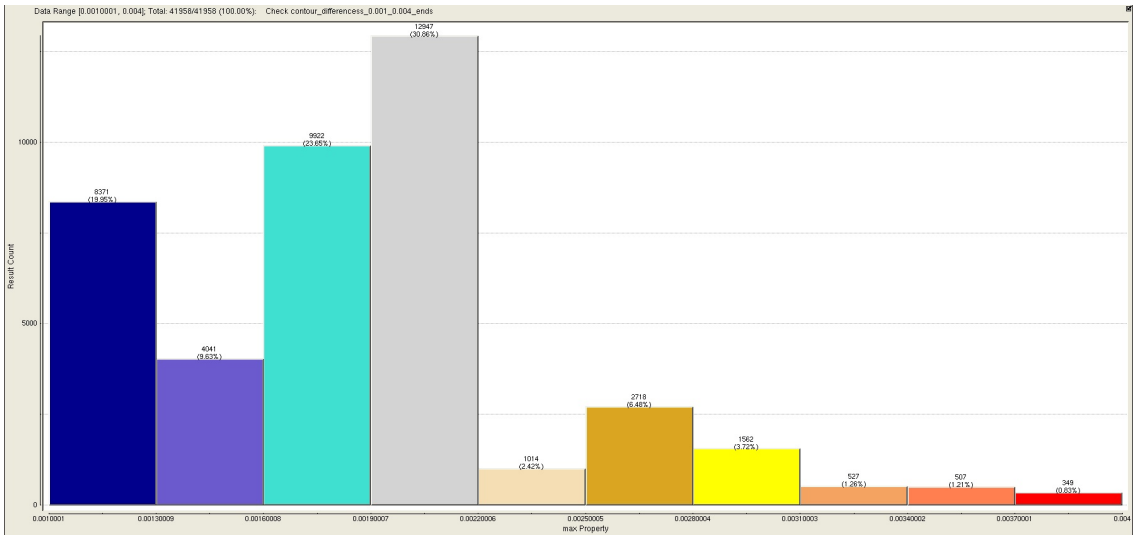

Figure 5.21: A histogram showing the warning level differences between the two contours generated by the two models calibrated for the 2D structures. The x-axis represents the difference between the contour edges at the long lines of the target contour in um. The y-axis represents the count of the differences in each bucket. The differences between the contours is between 1nm to 4nm.

In Figure 5.22, a histogram shows the two models contour differences at line ends and space ends edges. The x-axis represents difference values at the contour in um. The y-axis represents the count of the differences in each bucket. The total count is 183 differences between 4 nm and 6 nm.

5.5.2.3 Discussion

As we move toward the 3 nm those locations can be considered as warning locations and decrease the acceptable error budget of the process. The critical pitch is 300nm. The pitch is equally divided between CD and space (150 nm) each. The allowed process deviation is typically 10%. The allowed on process deviation is translated to be 15 nm per CD. Based on Figure 5.20, the contour differences between the two models is equal to 3 nm per edge which is 6 nm per CD which is almost 40% of the allowed process margin. This can is mainly due to uncertainty in the model.

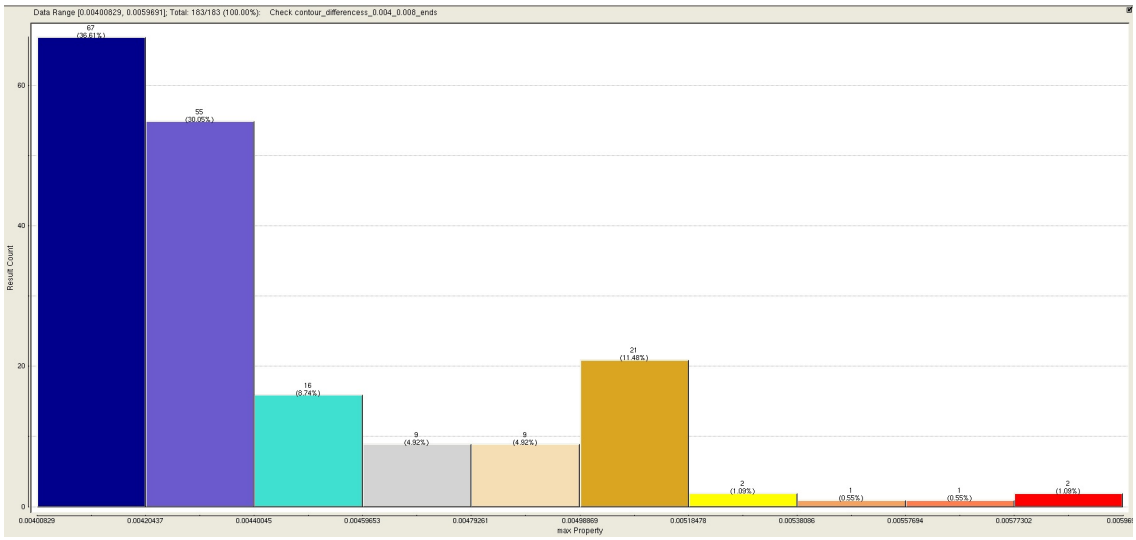

Figure 5.22: A histogram showing the difference between the two contours. The x-axis represents the difference between the contour edges at the long lines of the target contour in um. The y-axis represents the count of the differences in each bucket. The differences between the contours is between 1nm to 4nm.

As we go further into advanced technology nodes the error budget decreases, therefore, the required model uncertainty also need to decrease by adopting better sample plan that reduces the final full chip simulation uncertainties.

For a line and space layer the line ends and space ends are critical as typically those layers are connected to other layers above and below using contacts or vias. Those vias and contacts have a minimum enclosure to line and space layer. The uncertainties at the contour level found in this simulation signifies that models can introduce undetected errors which may affect the error budget allowed to this process.

Chapter 6

Summary and Future Work

6.1 Summary

A methodology for generation of a resist model with improved predictability for optical proximity correction is presented. The enhanced predictability model is achieved by having a guided sample plan selection based on full chip date image parameters. The model calibrated with full chip sample plan is compared to model calibrated with the heuristic sample plan.

Given the limited error budget for advanced technology nodes, instead of calibrating a process model with heuristic sample plan and being at risk of having a final model coverage and accuracy issues. A sample plan out of several thousands of heuristic data based on a real design image parameters is selected. The selected sample plan maintains the simplicity measurement process avoiding complexity in the test patterns and ensure the similar image parameter coverage as the full chip. Also the generated sample plan is following the same image parameter density as the full chip. The density resemblance between the full chip and the sample plan increases the presence of the test patterns at high density location and maintains the coverage as we move to low density locations. This ensures enhanced prediction for the high density locations in full chip image parameter space and minimized model errors at critical full chip locations without degrading low density locations prediction as they are included in the sample plan. Comparing the model generated with our sample plan to the heuristic sample plan model differences at the contour level were found. Differences that may degrade the allowed technology node error budget.

To achieve the full chip based image parameter sample plan, optical image parameters for millions of fragments on a full chip are evaluated to determine the image parameters space of the full chip. C-LAPI code was developed to extract optical image parameters per fragment on the full chip and filtering out artefact fragments. Thousands of test pattern structures are generated covering the full chip image parameters. Studying the image parameters of regular seed structures relative to the full chip image parameters domain helped in coving the full chip image parameters domain. Sample plan of around 1500 test patterns was selected from the thousands of test patterns structures by minimizing the distance in the image parameter space. The distance is measured between the full chip fragments image parameters and the thousands of test patterns. Test patterns closer to the full chip fragments in the image parameter space are selected. The final sample plan is formed of regular test patterns that can be measured following the heuristic sample plan measurement procedures. The final sample plan followed the same distribution in the image parameters domain as the full chip fragments in the image parameters domain. Comparison between the resist models calibrated with our sample plan and a heuristic sample plan was performed. our sample plan model showed better prediction on variety of verification sets. Contour differences were found between the two models for the same full chip mask.

6.2 Future Work

In this work, the main concern was the closeness of the selected test patterns to all the full chip fragments in the image parameter space. The evaluation of the image parameters for all the fragments on the full chip is a heavy computational process, that requires both runtime and large memory consumption. Pre-processing of full chip might help in the reduction of the required resources of complete the full chip image parameter analysis. Runtime and memory needed is a function of the total count of the fragments on the full chip. Full chip pattern classification of the full chip patterns before the evaluation of the image parameters of the full chip might enhance the flow runtime. The full chip pattern classification aims to reduce the total count of the fragments to analyse. Pattern matching algorithms might be

a candidate for pattern classification. Also the reduction of the full chip to set of unique patterns will enable running this flow on several full chips with an affordable runtime.

+

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الملخص

ان الدافع وراء صناعة أشباه الموصلات هو الحاجة إلى المزيد من الاجهزة على شريحة واحدة وتوفير معالجات أسرع، ذاكرة أكبر. كل عملية في عمليات تصنيع الدوائر المتكاملة تحتاج إلى أن تكون الأمثل و الأفضل لتلبية الطلب في السوق و تحقيق الأرباح المستدامة. عملية الطباعة الضوئية أصبحت من العمليات الحاسمة التي شهدت تحسينات هائلة خلال السنوات ال٣٠ الماضية. ان العقد التكنولوجيا المتقدمة ٣٢نانومتر و أقل تعانى من زيادة تكلفة التصنيع. تحقيق انتاجية عالية أصبح تحديا بالنسبة لمعظم الشركات المصنعة. ساعدت برامج المحاكاة لعملية التصنيع في خفض التكاليف والسماح لكمية واسعة من التجارب للوصول إلى الظروف المثلى لتحقيق انتاجية أعلى. الهدف من هذه الدراسة هو تطوير منهجية جديدة لنمذجة نماذج دقيقة لمحاكاة عملية الطباعة الضوئية. أن نماذج عملية الطباعة الضوئية تستخدم لتصحيح القرب الضوئى لتوليد أنماط قناع الصحيحة. أنماط القناع صحيحة تساعد في خفض تكلفة التصنيع وتجنب الاخفاقات غير المتوقعة. أيضا النماذج الدقيقة لعملية الطباعة الضوئية سوف تساعد في التنبؤ بالمناطق الساخنة خلال عملية تصميم الرقاقة الكاملة من خلال اختبارات التوافق مع الطباعة الضوئية.

لقد أجريت هذه الدراسة من خلال فهم خطوات عملية الطباعة الضوئية بدءا برقاقة مسطحة حتى يتم تشكيل نمط على السيليكون. أولا، تحدد العلاقة بين صورة المقاوم الضوئى و معلمات الصورة الهوائية. ثانيا، تدرس تبعية تقنيات تعزيز الدقة على نماذج عملية الطباعة الضوئية. أخيرا، تدرس الأطروحة استخدام معاملات الصورة كمؤهل لتعزيز تغطية النموذج استنادا إلى أحد النماذج الصناعية، تحسب معاملات الصورة لرقاقة كاملة، يصمم قناع من من الأنماط الأختبارية بحيث يحتوى على المعاملات الضوئية للرقاقة الكاملة. يتم اختيار أنماط خطة العينات اعتمادا" على مدى قرب المعاملات الضوئية لكل من أنماط الأختبار و الرقاقة الكاملة فى فراغ المعاملات الضوئية ذو الاربع ابعاد. و يتم مقارنة خطة العينات المعتمده على الرقاقة الكاملة مع خطة العينات تجريبيه عن طريق نمذجة نماذج للمقاوم و التحقق من كلا النموذجين.

نتائج هذه الدراسة هو إنشاء العينات اعتمادا على معاملات الصورة لتوفير نماذج عملية دقيقة تنبؤية لتصحيح القرب البصرى وغيرها من تقنيات تعزيز الدقة، علاوة على ذلك يقلل من خطر فشل النموذج غير المتوقع. و قد تم دمج المنهجية الجديدة فى عملية النمذجة و تم تقديم توصيات لخطة انشاء العينات. و يمكن ان تكون هذه المنهجية آلية.

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تاريخ الميلاد: ٢٤/ ١٢ / ١٩٨٥

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عنوان الرسالة:

خطة إنشاء العينات والتغطية لكل معاملات صورة الدائرة بهدف النمذجة لتصحيح القرب الضوئى

الكلمات الدالة:

الطباعة الضوئية؛ تقنيات تعزيز الدقة؛ تصحيح القرب الضوئى؛ نمذجه؛ محاكاه

ملخص البحث:

تستخدم الطباعة الضوئية فى صناعة الدوائر المتكاملة. مع القيود المفروضة على الطول الموجى المستخدم اصبح تحدى تصغير الأنماط يحتاج الى تقنيات تعزيز الدقة. تصحيح القرب الضوئى هو احد تقنيات تعزيز الدقة. يحتاج تصحيح القرب الضوئى الى نماذج تنبئية لعملية الطباعة الضوئية. فى هذه الدراسة، نقدم منهجية جديدة لخطة إنشاء العينات تستند الى تحليل تغطية معاملات الصورة الدائرة. تهدف خطة العينات الى توفير نماذج تنبئية للمقاوم الضوئى المستخدم فى الطباعة الضوئية.

خطة إنشاء العينات والتغطية لكل معاملات صورة الدائرة بهدف النمذجة لتصحيح القرب الضوئى

اعداد

محمد كامل عبد الفتاح كامل معوض

رسالة مقدمة إلى كلية الهندسة جامعة القاهرة
كجزء من متطلبات الحصول على درجة ماجستيرالعلوم
في
هندسة الالكترونيات و الاتصالات الكهربية

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الجيزة – جمهورية مصر العربية
٢٠١٥

خطة إنشاء العينات والتغطية لكل معاملات صورة الدائرة بهدف النمذجة لتصحيح القرب الضوئى

اعداد

محمد كامل عبد الفتاح كامل معوض

رسالة مقدمة إلى كلية الهندسة جامعة القاهرة
كجزء من متطلبات الحصول على درجة ماجستيرالعلوم
في
هندسة الالكترونيات و الاتصالات الكهربية

تحت إشراف

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و الاتصالات الكهربية
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