RESEARCH ON MEMRISTIVE- AND MEMCAPACITIVE-BASED GATE-LESS MEMORY ARRAYS

By

Ahmed Adel Mohamed Emara Kassem

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfilment of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Communications

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Title of Thesis:

Research on Memristive- and Memcapacitive-based Gate-less Memory Arrays

Key Words:
Memristor; Memcapacitor; Gate-less memory array; Sneak paths

Summary:
This work aims to explore the properties of emerging devices as memristors and memcapacitors. The use of these devices as memory cells in memory applications is investigated as well as the techniques used for information extraction. The work helps to better solve the problems of sneak paths in gate-less arrays, coupling capacitance between selection bars and non-uniformity of data distribution in the array. It also gives a guide to solving selection bar resistance effect for future work.

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Dedication

To

my parents:

Dr Adel

and

Dr Neamat,

my sister:

Ayah,

and

my brothers:

Abdel Rahman,

and

Ibrahim.

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List of Symbols and Abbreviations

Symbols	**Description**
v	Voltage.
i	Current.
q	Charge.
ϕ	Magnetic flux.
R	Resistance.
G	Conductance.
C	Capacitance.
L	Inductance.
t	Time.
M	Memristance.
W	Memductance.
R_{on}	Low resistance state.
R_{off}	High resistance state.
D	Device width.
w	Doped region width.
μ_v	Dopants mobility.
σ	Charge time integral.
ρ	Magnetic flux time integral.
α	Device voltage order.
β	Device current order.
Ξ	Device complexity metric.
Z	Impedance.
U	Potential energy.
F	Force.

z	Membrane displacement.
z_o	Membrane equilibrium position.
k	Membrane stiffness coefficient.
m	Membrane mass.
ω_o	Membrane natural frequency.
γ	Damping constant.
ζ	Damping ratio.
E	Electric field.
ϵ_o	Vaccuum permittivity.
y	Normalized membrane displacement.
Z_m	Selected impedance.
n_i	Node i.
$Z_c/Z_r/Z_a$	Impedances of cells in the selected column/ selected row/ niether selected column nor row.
Z_{ij}	Impedance measured between node i and j.
Z_t	Detected value.
Z_{th}	Threshold impedance.
C_c	Coupling capacitance.
R_l	Line resistance.
r	OFF/ON ratio.
R_{av}	Mean resistance.
p	Generalized mean parameter.
x	ON cells to total cells ratio.
R_{arr}	Array resistance.

Abbreviations	**Description**
ITRS	International Technology Roadmap for Semiconductors.
CMOS	Complementary Metal-Oxide-Semiconductor technology.
RAM	Random Access Memory.
RRAM	Resistive Random Access Memory.
MRAM	Magnetic Random Access Memory.
FRAM	Ferroelectric Random Access Memory.

CBRAM	Conductive Bridge Random Access Memory.
PCM	Phase Change Memory.
DRAM	Dynamic Random Access Memory.

List of Publications

Published:

[1] Ahmed A. Emara, Mohamed M. Aboudina, and Hossam A.H. Fahmy. "Corrected and accurate Verilog-A for linear dopant drift model of memristors". In: *2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, Aug. 2014.

[2] Ahmed A. M. Emara, Mohamed M. Aboudina, and Hossam A.H. Fahmy. "Nonvolatile low-power crossbar memcapacitor-based memory". In: *Microelectronics Journal* 64 (June 2017), pp. 39–44.

[3] Ahmed A. M. Emara, Mohamed M. Aboudina, and Hossam A.H. Fahmy. "Adaptive and optimum multiport readout of non-gated crossbar memory arrays". In: *Microelectronics Journal* 67 (Sept. 2017), pp. 162–168.

Abstract

In this work, we explore the properties of one of the relatively new devices, the memristors, which act as memory resistors and are considered the fourth fundamental circuit element along with resistors, capacitors and inductors. Memristors have resistance switching property and can preserve their state in the absence of applied signal. This makes them candidates for use in memories, logic circuits, reactance-less oscillators, neural networks and many more useful applications. We also explore the extended class of memcapacitors and meminductors which are also the memory analogues of capacitors and inductors respectively. They are part of the more general class of higher-order elements and the even wider class of fractional-order elements. We investigate the use of these devices as memory cells in gate-less crossbar memory arrays and how the goals of the International Technology Roadmap for Semiconductors (ITRS) can be achieved. The goal of the ITRS in memories is to achieve high speed, high density and low power consuming memory arrays. Researches are done on the new emerging devices, which contains the discussed memelements, to be used as a possible replacement for CMOS technology due to the prediction of its scaling limitation and the end of the distinguished Moore's law. Gate-less memory arrays are arrays that do not use selector devices, as diodes or transistors, to select the desired cell which aims to save the cost of the additional area used for selector devices to make more dense arrays. We focus on the sneak paths problem that faces the gate-less arrays and how to overcome them. Sneak paths are the undesired paths passing through the unselected devices due to the absence of selector devices that prevents current from passing through the unselected devices but can be got rid of them by using some tricky readout techniques. We analyze one of the most advantageous methods for reading data from gate-less memristive arrays that uses three measurements and doing arithmetic to extract the cell information and cancel out the sneak paths effect mathematically and show how this method can be generalized for all memelements, and edited to suppress the effect of the coupling capacitance between the bars used as selection lines. We also analyze the threshold used for detection of the binary data extracted from the array, how it can be optimized to withstand maximum deviation of the array binary data distribution among cells from the uniform distribution, and how this threshold can be made adaptive to the array cells' distribution. We last show a reading technique that uses a single-measurement to extract data without arithmetic operations as well as suppressing sneak paths which has advantage over the discussed technique in terms of speed and noise margin. Finally, we offer new theoretical approaches for future work to overcome the effect of the bar resistance on the extracted information from the array by modeling

the array as a communication channel and using communication techniques to overcome the distortion of the information sent through it.

This work is organized as follows: Chapter 1 discusses the definition of memristors, their properties, their mathematical and circuit models, some of the devices exhibiting memristive properties as well as some of the possible applications. Similarly, Chapter 2 discusses the extended class of memcapacitors and meminductors, their properties, materials that exhibit such properties as well as some further generalizations and extensions of circuit elements. Afterwards, Chapter 3 explores the use of memcapacitors as a memory cell, discusses the gate-less memory arrays and their problem of sneak paths as well as some of the possible solutions with focus on the advantageous three-readings method. The method is applied to memcapacitive arrays with modification to suppress the capacitive coupling and bar resistance effects. Then, Chapter 4 discusses the optimization of the threshold and how it can be adaptive to the information distribution among cells. Chapter 5 proposes a single-measurement method for data extraction. Finally, Chapter 6 concludes the work and offers insight to solving the line resistance effect by utilizing communication techniques to overcome the channels' effects.

Chapter 1

Memristors

1.1 Introduction about memristors

Memristors are new circuit elements which were first proposed by L. Chua in 1971 [1] as the fourth fundamental two-terminal circuit element along with resistors, capacitors and inductors. The three known fundamental circuit elements are characterized by possessing a relation between two of the four electrical quantities which are the voltage across its terminal v , the current passing through it i , the charge q and the flux-linkage φ . A resistor is characterized by possessing a relation between the voltage across its terminals and the current passing through it where the resistance is defined as the rate of change of voltage with respect to current $R = dv/di$. The conductance is defined as the multiplicative inverse of the resistance $G = 1/R$ and if the resistor is a linear resistor the resistance is simply the ratio between the voltage and the current as in Ohmic resistors. Similarly, a capacitor is characterized by the relation between the charge and voltage where the capacitance is defined as the rate of change of charge with respect to the voltage $C = dq/dv$, while an inductor is characterized by the relation between the flux-linkage and the current where the inductance is defined as the rate of change between the flux-linkage with respect to the current $L = d\varphi/di$. These elements define three of six possible combinations of the four electrical quantities characterizing circuit elements, with two combinations are already implied by definition which are: the relation between charge and current is $q = \int_{-\infty}^{t} i(t)dt$ and the relation between flux-linkage and voltage is defined by faraday's law as $\varphi = \int_{-\infty}^{t} v(t)dt$. The only remaining combination is the relation between the flux-linkage and the charge. The proposed element, the memristor, is supposed to be the missing two-terminal element characterized by the relation between the flux-linkage and the charge where the memristance is defined as the rate of change between the flux-linkage with respect to the charge as shown in eq. 1.1:

$$M = \frac{d\varphi}{dq} = \frac{d\varphi/dt}{dq/dt} = \frac{v}{i} \tag{1.1}$$

And the memductance is defined as the multiplicative inverse of the memristance $W = 1/M$. The relations of fundamental circuit elements are illustrated in Fig. 1.1.

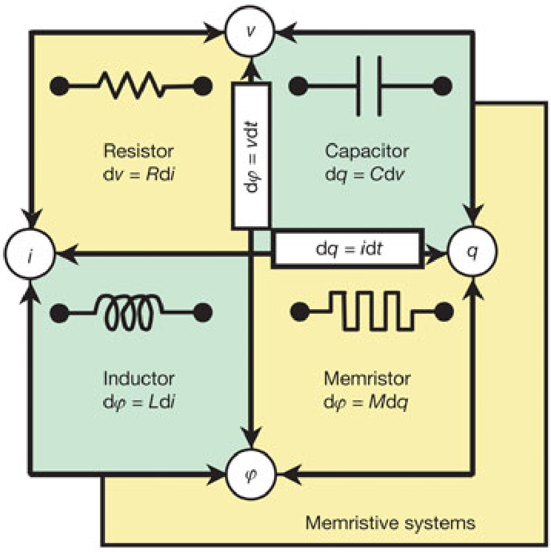


Figure 1.1: Four fundamental circuit elements [2].

It has to be noted that if the relation between flux and charge is linear, the memristance become constant and hence the memristor is reduced to a linear resistor according to eq. 1.1. So, the linear memristor does not have any contribution in the linear network theory. The memristor is called charge-controlled if the flux is an explicit function of the charge and in this case the memristance is a function of the charge $M = M(q)$, and it is called flux controlled if the charge is an explicit function of the flux and in this case the memristance is a function of the flux $M = M(\varphi)$. The general memristor is the device in which there is an implicit relation between flux-linkage and charge$f(\varphi, q) = 0$ and in this case, the memristance is a function in both flux and charge $M = M(\varphi, q)$. The name memristor is short for memory resistor due to the fact that the memristance is a function of charge and flux which are the integrals of current and voltage respectively, which means that the memristance depends on the history of the voltage or current. The memristor has a zero-crossing property in which $i = 0$ when $v = 0$ according to eq. 1.1. Under sinusoidal excitation, each voltage value is applied twice to the device but the integrals have different values which makes memristance have different values too and hence, the non-linearity and the zero-crossing property between voltage and current results in a pinched hysteresis loop (Lissajous figure) in I-V characteristics under sinusoidal excitation as shown in Fig. 1.2. The area inside the hysteresis loop decrease as the frequency of the applied signal increases and the memristor reduces to a linear resistor at very high frequencies as the effect of the integral is suppressed at high frequencies and the device cannot respond to high speed variations of the signal applied to the device.

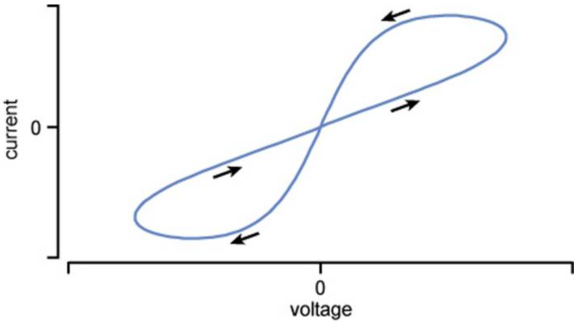


Figure 1.2: The pinched hysteresis loop in the memristor's I-V charateristics.

1.1.1 Memristive systems

In order for the definition of memristor to include practical elements, this class of elements was extended in 1976 by L. Chua and Sung Mo Kang [3] to a wider class called memristive systems which are defined by the two eq.s 1.2 and 1.3:

$$\dot{x} = f(x,i,t) \tag{1.2}$$

$$v = R(x,i,t)i \tag{1.3}$$

for current-controlled memristive system, and the eq.s 1.4 and 1.5:

$$\dot{x} = f(x,v,t) \tag{1.4}$$

$$i = G(x,v,t)v \tag{1.5}$$

for voltage-controlled memristive system, where x is the state of the system. In the special case of the ideal memristor, the state variable x is the charge: $x = q$, $\dot{x} = i$ and $v = M(x)i = M(q)i$. This broader definition means that memristive systems include devices in which the dynamics of the device's state variables are dependent on the applied voltage or current and these state variables in turn determine the resistance of the device or the relation between the voltage and the current. With this extension, the definition can then include thermistors, discharge tubes and some ionic systems. The thermistor, for example, has a state variable which is the temperature. The applied voltage and current dissipate heat in the thermistor and hence, the temperature dynamics depend on the applied electrical signals. The device's resistance in turn depends on its temperature which makes the thermistor has memristive properties.

1.2 Discovery of the memristor

The fabrication of the memristor delayed since its proposal in 1971 because search was made for a device that possesses a relation between its magnetic field flux-linkage and charge. But according to the properties of the memristor discussed above and the relations between voltage across memristor and the current passing through it, the memristor needs only non-linear relation between the integrals of voltage and current. It was not until 2008 when the first passive memristor was realized in HP labs using TiO_2 [2]. The HP TiO_2 memristor is a metal–oxide semiconductor of width D that has a heavily doped region of width w. This width changes according to the voltage applied to the device as the dopants drift to the undoped region changing the resistance of the device accordingly, so the device's resistance depends on a state, which is the width of the doped region, that depends on the history of the applied voltage or current. This device acts as an ideal memristor within a certain range of the state variable w and as a memristive system [3] within a larger range when the state variable approaches one of its two terminal states where $w\epsilon(0,D)$. The device was found to produce a pinched hysteresis loop in its I-V characteristics as predicted. Although the TiO_2 memristor was not the first memristor to be fabricated, it was the first to be recognized and modeled as memristor. TiO_2 also was known to long before exhibit resistive switching characteristics but these characteristics were first used to obtain memristor by HP in 2008.

It has to be noted that recognizing memristor as the fourth fundamental element that possesses a non-linear relation between the integral of the current and the integral of the voltage has been disputed in [4] in which the authors argued that the fourth fundamental element must be defined to possess a relation (linear or non-linear) between flux and charge without referring to the integrals of voltage or current. The HP labs did not refer to the flux in their device. Accordingly, they proposed a device in which a magneto-electric material, in which a magnetic signal stimulates electrical response, possesses the required relation between flux and charge and they named their device "transtor". However, this refutation was not cited much in the circuits and devices literature and the memristor was widely accepted as the fourth fundamental element.

1.2.1 Applying the memristive system definition to existing memory devices

In 2011, L. Chua showed that the memristive systems include all resistive switching non-volatile memory cells [5]. This means the memristor definition includes non-volatile types of RAM as: Resistive RAM (RRAM), Magnetic RAM (MRAM), Ferroelectric RAM (FRAM), Conductive Bridging RAM (CBRAM) and Phase Change Memory (PCM). RRAM is a cell, mostly made of an oxide, whose resistance changes according to the applied writing voltage and preserves its resistive state after voltage removal [2]. MRAM is a cell whose magnetization changes due to the induced magnetic field caused by the current passing through the device and this change in the magnetization changes the devices resistance [6]. FRAM is a cell in which a ferroelectric junction's polarization is changed according to the applied field's polarity which changes the resistance of the device [7]. CBRAM is a cell in which a conductive filament is either formed or dissolved due to redox reactions between two electrochemically-different electrodes placed in an electrolyte changing the device's resistance accordingly [8]. PCM is a cell that changes its phase from amorphous to crystalline or vice versa in response to the heat produced by the passage of electric current through the device and this phase change also changes the resistance of the device [9]. Some devices are bipolar in which changing the polarity of the applied voltage is required to swich the device's resistance while others are unipolar in which changing the magnitude of the applied voltage switches the resistance. In all of these devices, we see that the device has a state that changes in response to electric stimuli and the resistance of the device depends on this state and hence, it changes accordingly.

1.3 Modeling

The use of memristors in different electronic circuit applications that started since 2008 made it important for electronic circuit designers to use a realistic model for such a new device. Since the first realization of this device, several researchers proposed different SPICE and Verilog-A models to be used in simulations and applications such as memory design or logic circuits to benefit from the two terminal states of memristors. Digital applications need simple models only. Memristors can be also used in analog applications as well as mimicking neural networks. These latter applications need more accurate modeling than digital applications to be able to simulate the exact dynamics of the device to give accurate theoretical results.

1.3.1 Mathematical modeling

1.3.1.1 The linear dopant drift model

The first and simplest mathematical model for this memristor was the linear dopant drift model [2]. This model assumes that the dopants in the highly doped region are drifted with velocity that changes linearly with the voltage applied on the device changing the position of the boundary between the doped and the undoped region until the dopants reaches either of the two terminals, then it remains in this state and acts like a linear resistor till the polarity of the voltage applied is reversed. The memristor is modeled as two resistors in series: the doped region of length $w(t)$, and the undoped region of length $D-w(t)$ where D is the width of the device as shown in Fig. 1.3. The advantage of the linear dopant drift model of the memristor is that it describes the behavior of the memristor to a good degree, and very useful for the simulation speed due to the simplicity of the model and hence can be used in complex circuits. Such circuits include large digital circuits such as large memory arrays and complex digital circuits. The model is also extremely useful to proof the concept of most analog circuit techniques that are still under investigation and would require a fast simulation environment. The linear drift model's equations are shown in eq.s 1.6 and 1.7:

$$v(t) = \left(R_{on}\frac{w(t)}{D} + R_{off}\left(1-\frac{w(t)}{D}\right)\right) i(t),\ 0 \le w(t) \le D \tag{1.6}$$

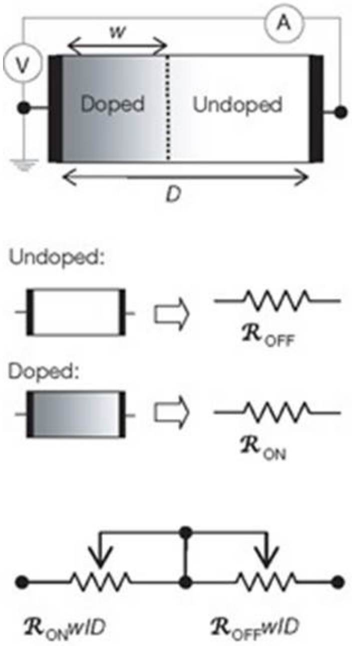


Figure 1.3: Modeling the HP labs memristor [2].

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{on}}{D} i(t) \tag{1.7}$$

Where $v(t)$ is the voltage across the memristor terminals, $i(t)$ is the current passing through the memristor, μ_v is the dopants mobility, R_{on} is the resistance of the device when $w = D$, and R_{off} is the resistance of the device when $w = 0$. The non-linear relation between voltage and current in the equation above results in pinched hysteresis loop I-V characteristics [2].

1.3.1.2 Non-linear models

There are other more complicated mathematical models for the memristor that aim to describe the device's dynamics more accurately to be used in applications that rely on the exact dynamics of the device. Modifications to the linear model include adding a window function to eq. 1.7 to limit the speed of variation of the state $w(t)$ at the boundaries [10–12]. There are also models that use non-linear drift equation instead of the linear one in eq. 1.7 [13]. Some models also try to more accurately model the physics of the device by using tunneling to model the dopants drift instead of diffusion [14, 15].

1.3.2 Verilog-A modeling

For the sake of simulation of circuits utilizing memristors, Verilog-A models were built for the memristor using the mathematical models discussed above. As we noted, the linear dopant drift model is the simplest model. Therefore, the Verilog-A models based on linear dopant drift model are very beneficial for simulations in which the exact dynamics of memristor are not important. This is the case in digital circuits in which the final states and the average switching speed of the memristor are all that matters. It can be useful for some analog circuits as well to test the function of a memristor-based circuit behaviorally. Also, it is very useful in very long simulations or circuits that contain large number of memristors such as memristor-based memory arrays.

Based on the linear drift model mathematical modeling [16, 17], a Verilog-A model was introduced in [18]. We presented a corrected model in a previous work [19] to overcome the problem of 'over-delayed switching effect' ([20]) of that model in which the integral accounts for the time the memristor stayed in its terminal state while it should act then as linear resistor. This model is shown in Appendix A. There are also models that adapts to all mathematical models and all device parameters that were developed which are the TEAM [21] and VTEAM [22] models. We showed in [19] that our model is more efficient than those two models when it comes to the linear dopant drift model as our model uses the closed-form equation to calculate the circuit variables compared to iterative methods that accumulates errors.

1.4 Conclusion

The memristor is a device first proposed in 1971 as the fourth fundamental circuit element whose resistance depends on the history of the applied voltage or current. It belongs to larger class of systems which is the memrestive systems. These systems are characterized by pinched hysteresis loop in the I-V characteristics. It was not until 2008 when the first passive memristor was discovered. The definition was then extended to include all resistive switching non-volatile memory devices. Since then, researchers are searching for applications for the memristors to benefit from their properties and several mathematical models were proposed to describe the dynamics of the device. Verilog-A models based on these mathematical models were developed to help researchers simulate the device in their proposed applications. Analogous to the memristor, memcapacitors and meminductors are defined as memory capacitors and inductors which will be discussed in the next chapter.

Chapter 2

Memcapacitors and meminductors

2.1 Introduction about memcapacitors and meminductors

Analogous to the memristor which acts as a memory resistor, another class of elements which are the memcapacitors and the meminductors are defined [23]. The memcapacitve and meminductive systems were proposed in 2009 by Massimiliano Di Ventra, Yuriy V. Pershin and Leon O. Chua to extend the notion of memristive systems where the memcapacitor acts as a capacitor with memory and the same for the meminductor which acts as an inductor with memory. The relation between the capacitor and the memcapacitor, or the inductor and the meminductor is the same as the relation between the resistor and the memristor. This relation is illustrated below in Fig. 2.1. The memcapacitor is a device that relates the integral of the voltage to the integral of the charge stored through a non-linear relation, if the relation is linear; the memcapacitor reduces to a linear capacitor. If we denote the integral of the charge as $\sigma = \int_{-\infty}^{t} q(t)dt$, the memcapacitance is defined in eq. 2.1:

$$C \;=\; \frac{d\sigma}{d\varphi} = \frac{d\sigma/dt}{d\varphi/dt} = \frac{q}{v} \tag{2.1}$$

The memcapacitor is σ-controlled if the flux is an explicit function of σ and in this case the memcapacitance is a function of the integral of the charge $C = C(\sigma)$, and flux controlled if σ is an explicit function of the flux and in this case the memcapacitance is a function of the flux $C = C(\varphi)$, while in general the memcapacitor possesses an implicit relation between σ and φ and so $C = C(\varphi, \sigma)$. The memcapacitor is therefore a capacitor whose capacitance depends on the history of the applied voltage or the charge stored. Similarly, the meminductor is a device that relates the integral of the current passing through it to the integral of the flux linked to it through a non-linear relation and also, if the relation is linear; the meminductor reduces to a linear inductor. If we denote the integral of the flux as $\rho = \int_{-\infty}^{t} \varphi(t)dt$, the meminductance is defined in eq. 2.2:

$$L \;=\; \frac{d\rho}{dq} = \frac{d\rho/dt}{dq/dt} = \frac{\varphi}{i} \tag{2.2}$$

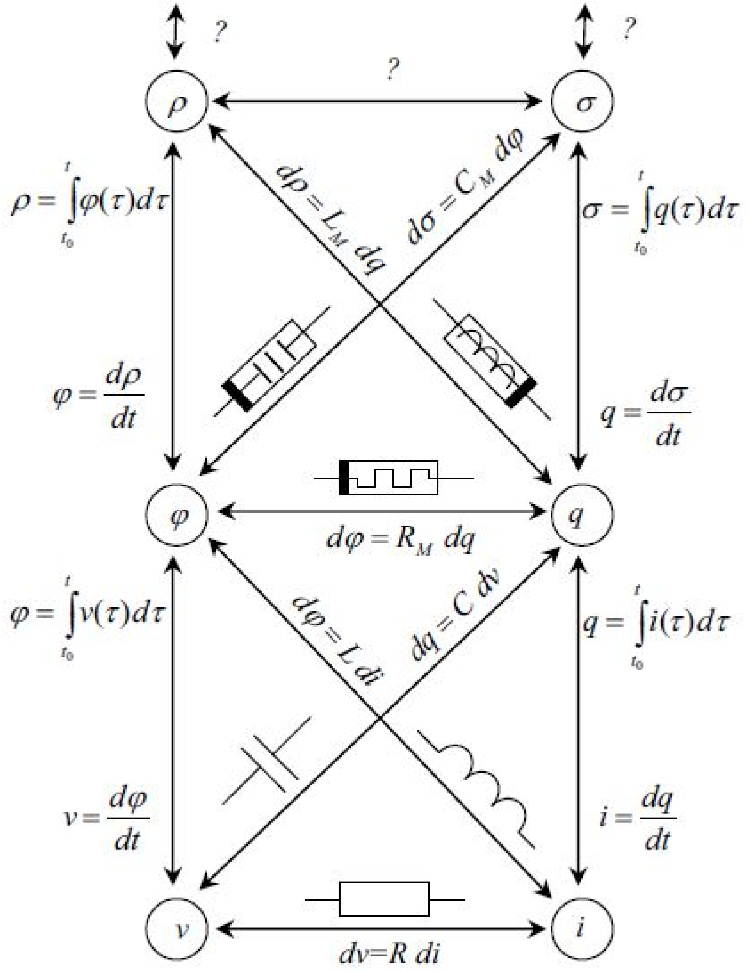


Figure 2.1: Relation between circuit variables in memelements [24].

The meminductor is called charge-controlled if ρ is an explicit function of the charge and in this case the meminductance is a function of the charge $L = L(q)$, and ρ -controlled if the charge is an explicit function of ρ and in this case the meminductance is a function of the integral of the flux $L = L(\rho)$, while in general the meminductor possesses an implicit relation between ρ and q and so $L = L(\rho, q)$. Similarly, the meminductor is an inductor whose inductance depends on the history of the current passed or the flux linked. Also, the memcapacitor or the meminductor reduces to a linear capacitor or inductor respectively at high frequencies.

As in the case of memristors and memristive systems, the memcapacitors and meminductors belong to a larger class of system which are memcapacitive and meminductive systems respectively. For a system whose input and output are $u(t)$ and $y(t)$ respectively x is the state of the system where $u(t)$ and $y(t)$ are two of the four quantities (voltage, current, flux and charge), a u -controlled memory system is defined by the two eq.s 2.3 and 2.4:

$$y(t) = g(x, u, t) u(t) \tag{2.3}$$

$$\dot{x} = f(x,u,t) \tag{2.4}$$

Where $u(t)$ and $y(t)$ are the charge and voltage for the memcapacitive system, and the flux and current for the meminductive system. These systems are characterized by a hysteresis loop in the Q-V characteristic curve in case of memcapacitive systems and in the Φ-I characteristic curve in case of meminductive systems.

2.2 Existence of memcapacitive and meminductive systems

Some capacitors were reported to have memory properties that are believed to be memcapacitive according to [23] as in [25] in which interface traps are responsible for the memory effect, and [26, 27] in which embedded nano-crystals are responsible for the memory effect. Also, there are some inductors that were reported to have memory properties that are believed to be meminductive properties as in [28] in which the core material is a ferromagnetic material exhibiting a magnetic hysteresis response to the applied magnetic field giving memory effect, and [29] in which superconducting circuits' inductance exhibits memory effects as lagging.

Also, some device structures were proposed as possible realizations for memcapacitive systems as [30] in which one of the capacitor's plate is an elastic membrane whose shape changes with time according to the applied input giving rise to memory effect, and [31] in which memory effect is due to the delayed response due to slow polarization rate of a meta-material containing parallel plates between parallel plates. The elastic membrane memcapacitor [30] will be discussed in details in Chapter 3. Memcapacitive effects were also reported to exist along with memristive effects in some solid-state devices [32, 33]. In our work, we focused on memcapacitive systems rather than meminductive systems due to the involvement of capacitors in more applications than inductors.

2.3 Higher-order non-linear circuit elements

Although their properties were not exclusively discussed and analyzed until 2009 in [23], memcapacitors and meminductors belong to an early discussed class of higher-order non-linear circuit elements. This class of elements were discussed in 1980 by L. Chua in [34] and were re-studied by him in [35]. The generalization assumes that non-linear circuit elements are characterized by the relation between a pair of signals which are: $v^{(\alpha)}(t)$ and $i^{(\beta)}(t)$, which are defined in eq.s 2.5 and 2.6:

$$v^{(\alpha)}(t) = \begin{cases} \frac{d^{\alpha}v(t)}{dt^{\alpha}} & \alpha = 1,2,\ldots,\infty \\ v(t) & \alpha = 0 \\ \int_{-\infty}^{t}\int_{-\infty}^{\tau_{|\alpha|}} \cdots \int_{-\infty}^{\tau_2} v(\tau_1)d\tau_1 d\tau_2 ... d\tau_{|\alpha|} & \alpha = -1,-2,\ldots,-\infty \end{cases} \tag{2.5}$$

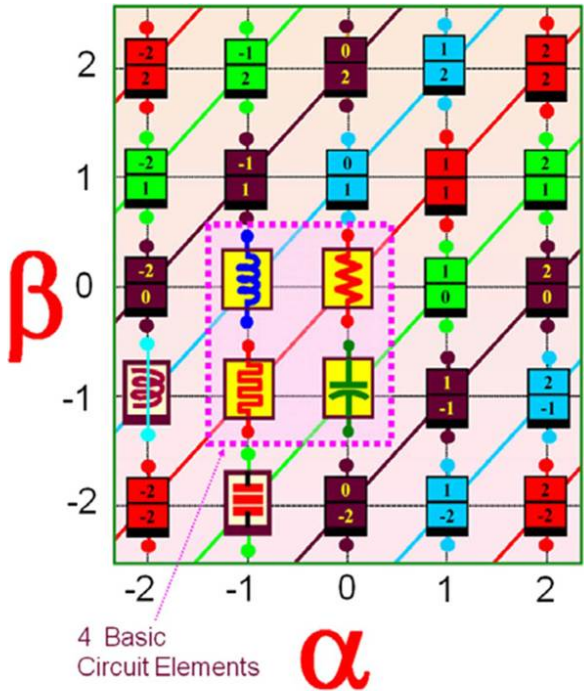


Figure 2.2: Periodic table of elements [36].

$$i^{(\beta)}(t) \quad = \quad \begin{cases} \frac{d^{\beta}i(t)}{dt^{\beta}} & \beta = 1,2,\ldots,\infty \\ i(t) & \beta = 0 \\ \int_{-\infty}^{t}\int_{-\infty}^{\tau_{|\beta|}}\ldots\int_{-\infty}^{\tau_2} i(\tau_1)d\tau_1 d\tau_2 \ldots d\tau_{|\beta|} & \beta = -1,-2,\ldots,-\infty \end{cases} \tag{2.6}$$

According to this definition, each element is defined by an ordered pair (α,β) in a so called periodic table of elements shown in Fig. 2.2. Each element has a complexity metric $\chi = |\alpha| + |\beta|$defined as the rectilinear distance from the origin in Fig. 2.2. The resistor is element (0,0), the capacitor is (0,-1) and the inductor is (-1,0). The corresponding memelements are assigned (-1,-1), (-1,-2) and (-2,-1) respectively. However, it is improbable that devices of $|\alpha| > 2$ and $|\beta| > 2$ would be used in the modeling of real devices. Also, devices of $\chi > 2$ are always active devices [36].

As with derivatives and integrals of ordinary calculus, fractional calculus was applied to circuit devices as well. Fractional calculus generalizes the differentiation operator to be applied fractional times to the mathematical function. For example, there exists the half derivative which if applied to a function twice it yields the ordinary first derivative. Fractional devices were proposed in [37] to model frequency-dependent imperfections of capacitors and other real devices leading to fractional-order capacitors (0, β) whose impedance is $Z = 1/CS^{|\beta|}$ and fractional-order inductors (α ,0) whose impedance is $Z = LS^{|\alpha|}$ where -1< α <0 and -1< β <0 . In 2009, a fractional-order memristor was proposed in [38] that applies fractional calculus to the integrals of voltage and current similar to the concepts of fractional capacitors and inductors. Afterwards, fractional calculus was applied to define fractional elements for memcapacitors and meminductors as well as all higher-order elements [39, 40] where α and β can be non-integers in eq.s 2.5 and 2.6.

2.4 Conclusion

The memcapacitors and meminductors were introduced in 2009 to extend the notion of memristor. They act as capacitors or inductors with memory. They belong to a wider class of systems which are the memcapacitive and meminductive systems. Some systems were reported to exhibit such properties. Also, some realizations for the memcapacitors were proposed to implement a solid state or NEMS memcapacitor. There is a generalization of high-order integrals or derivatives of voltage or current for non-linear elements which contains these elements. Fractional calculus generalization of the integrals and derivatives of voltage and current in memrsitor as well as other higher-order devices was proposed as well. The use of these memelements in memory arrays will be discussed in the next chapter.

Chapter 3

Memcapacitor-based array

The objective of the current research on memory technology is to minimize the cell size, minimize power consumption and maximize the speed. The current DRAM technology has cell area 7776nm^2, read and write times less than 10ns, read energy per bit 10^{-13}J and write energy per bit 4×10^{-15}J [41]. Due to expected limitations in the scaling of the CMOS technology and the end of Moore's law, search for new emergent technologies has increased.in parallel with research to scale down CMOS technology. Among these emerging devices are memory devices that depends on resistive switching as found in some oxides which are, as discussed in Chapter 1, considered memristors.

Recently, the memristors were investigated as non-volatile memory cells [42]. The memristor memory array is composed of crossbar structure which is formed of memory cells placed at intersection points between upper and lower bars where the upper bars are placed in the form of columns and the lower bars are placed in the form of rows. To select a memory cell, the corresponding row and column are selected. This structure is gate-less i.e. it does not need a switch at each cell. This increases the density of the memory cells in an array significantly as no switches are needed and lowers power consumption as no power is dissipated in the resistances of the switches. The main problem in the passive array is the sneak paths [43]. Sneak paths are the undesired paths parallel to the cell intended to be read or written to. There were some proposed techniques that solve the sneak paths problem, the simplest and most accurate one is the method presented in [44]. In this chapter, we introduce a gate-less memory array based on memcapacitors as memory cells instead of memristors that eliminates also the effect of sneak paths based on the method introduced in [44] while also enhancing this method to eliminate parasitic effects in the array as the coupling between adjacent bars and the resistances of the bars.

3.1 Memcapacitor as a memory cell

As explained in the previous chapter, the memcapacitor is a device whose memcapacitance changes according to the history of the applied voltage or the history of the stored charge. It retains its recent memcapacitance value after the applied voltage is removed.

Some device structures were proposed as possible realizations for memcapacitive systems as [30] in which the capacitor plate is an elastic membrane whose shape changes with time according to the applied input giving rise to memory effect, and [31] in which memory effect is due to the delayed response due to slow polarization rate of a meta-material between parallel plates. The memcapacitor's properties make it a candidate to be used as a memory cell. This use of the memcapacitor as a memory cell is unlike the ordinary capacitor where the value is not stored as charge on the plates of the device but as the value of the memcapacitance i.e. as an internal state of the device. This proposal has several advantages over memories that depends on charge storage as dynamic random access memories (DRAMs) as it is non-volatile and does not need refreshing. DRAMs need refreshing because the charge stored on the capacitors plates leaks away from the plates of the capacitor as time passes leading to decrease of the voltage on the capacitor which may result in an error in the reading process if the voltage decreases below the threshold value between the two binary values, so, the value stores must be read and rewritten periodically to avoid loss of information from the cell. This is not the case if the information is stored in the internal state of the device with no charge stored as in memcapacitors. The memcapacitor's internal state is held constant in the absence of external stimulus and hence retains information. The storage of the information in the form of an internal state of the device has another advantage over the storage of information in the form of stored charge as the memory array can be gate-less as no switches are needed to isolate each cell from the other which is necessary in case of ordinary capacitors to avoid charge sharing between different memory cells and loss of information. Memcapacitive effects were reported in metal oxide devices [32] where the sensing speeds and sizes are very promising. The sensing speed was reported to be less than 10ns which is similar to the DRAM sensing speed. The device has endurance of over 108 switching cycles which is less than the DRAM's endurance of 1016 cycles. The retention time for the ON and OFF state was found to be more than 105s which clearly shows the device does not need refresh as the DRAM whose retention time is only 64ms. According to ITRS 2013, the feature size F of metal oxide based memory devices has reached 40nm with cell area $4F^2$ which is comparable to the DRAM feature size F of 36nm and cell area of $6F^2$ [41].

The use of a memcapacitor as a memory cell can be as follows: Each memcapacitor possesses two voltage thresholds for each state which if exceeded, the device switches to this state. If the two thresholds have opposite polarities, the device is considered bipolar, and if they have same polarity, the device is unipolar. The reading operation is done by applying a voltage pulse on an ordinary capacitor in series with the memcapacitor and sensing the voltage on the memcapacitor which must be below the thresholds of the device. The writing operation can be done by applying the appropriate voltage pulse above the threshold that switches the state of the memcapacitor to the required state. One problem of using the memristors and memcapacitors as memory cells is sensitivity to input fluctuations and stochastic catastrophe [20] which means that the absence of energy barrier between the two limiting states of the memcapacitor can lead to loss of information due to the noise present in the circuit. The superlattice memcapacitor presented in [31] has the previous problem and so it needs refresh and its reading process is destructive and hence, data needs to be re-written after reading process. While the memcapacitor presented in [30] does not have the previous problem as it is bistable i.e. it has only two stable states.

The elastic membrane memcapacitor is a parallel plate capacitor in which one of the plates is a flexible strained membrane as shown in Fig. 3.1. The elastic membrane has only two stable positions separated by an energy barrier and a critically stable position which is the middle position. One of the two stable states, for example the upper position, is denoted as ’0’ where the device’s capacitance iswhile the other lower position is denoted as ’1’. These two stable states of the elastic membrane makes the memcapacitor has two stable capacitances. To simplify the calculations, the effective displacement of the membrane from the middle position is used to use the calculations of a parallel plate capacitor and is denoted by z . The effect of the stress on the membrane can be modeled by a double well potential $U(z)$ defined by eq. 3.1:

$$U(z) \quad \propto \quad (z^2 - z_o^2)^2 \tag{3.1}$$

The well is shown in the right panel of Fig. 3.1, where $z = \pm z_o$ are the two equilibrium positions. The constant of proportionality is assumed to be $k/4z_o^2$ such that $k = m\omega_o^2$ is a constant characteristic of the membrane, m is the mass of the membrane, and ω_o is the natural oscillating frequency. We wil use bold font in the following equations to denote vectors and the symbol $\hat{\mathbf{k}}$ for a unit vector in the positive z-axis direction. The forces acting on the membrane are: 1) The elastic force defined in eq. 3.2 as:

$$\mathbf{F}_{elastic} \quad = \quad \frac{-dU(z)}{dz} = -m\omega_o^2\mathbf{z}(\frac{|\mathbf{z}|^2}{z_o^2} - 1) \tag{3.2}$$

2) The damping force defined in eq. 3.3:

$$\mathbf{F}_{damping} \quad = \quad -\gamma m\dot{\mathbf{z}} \tag{3.3}$$

Where $\gamma = 2\zeta\omega_o$ is the damping constant and ζ is the damping ratio, and 3) The electrostatic attraction force defined in eq. 3.4:

$$\mathbf{F}_{electrostatic} \quad = \quad -q|\mathbf{E}|\hat{\mathbf{k}} \tag{3.4}$$

Which arises between the two plates due to charge stored on the plates. The negative sign is due to the fact that the force is always attractive as the two plates have opposite charge and hence, it points downwards. The electrostatic field between the two parallel plates is expressed as $E = \sigma/2\epsilon_o$, where $\sigma = q/S$ is the surface charge density of the plates, S is the area of the plates and ϵ_o is the vacuum permittivity. By using Newton’s second law, we get the equation of the elastic membrance memcapacitor dynamics in [30] as shown in eq. 3.5:

$$\ddot{y} \;=\; -\omega_o^2 y\left(\frac{y^2}{y_o^2}-1\right)-2\zeta\omega_o\dot{y}-\frac{C_0 v^2(t)}{2md^2(1+y)^2} \tag{3.5}$$

Where $y = z/d$ is the normalized displacement, d is the distance between the middle position of the membrane and the other plate, y_o is the normalized displacement corresponding to the equilibrium position z_o and $C_0 = \epsilon_o S/d$ is the capacitance at the middle position. The two stable states of the memcapacitor are: Low capacitance (high impedance):$C_{on} = C_0/(1+y_o)$ corresponding to '0' and high capacitance (low impedance): $C_{off} = C_0/(1-y_o)$ corresponding to '1'. It has to be noted that this memcapacitor is non-polarized as the voltage in the previous equation is squared. When a voltage pulse is applied on the elastic membrane memcapacitor, it results in pulling the membrane downwards during the rise edge of the pulse due the electrostatic force, then at the falling edge the membrane is released and pulled upwards by the restoring force. If the voltage pulse amplitude is very low, it will not be able to change the position of the membrane as it cannot overcome the barrier. As the voltage pulse amplitude increases, the pull of the rising edge is able to pull the membrane from its upper position to its lower one while the restoring force is not able to return it to its upper position due the attractive force between the plates, but as the pulse amplitude increases more, the membrane is released from a position more distant from the equilibrium position and so, will be able to overcome the electrostatic force and return to the upper position. So, to use the elastic membrane memcapacitor as a memory cell, reading can be performed by applying voltage pulse that has an amplitude low enough that is unable to change the position of the membrane. To write '1' we need to move the membrane to the lower position, so, we apply a pulse whose amplitude is high enough to pull the membrane from the upper position to the lower one, but low enough to make the displacement from the equilibrium low so that the restoring force cannot overcome the barrier as it is opposed by the electrostatic force between the plates. Finally, to write '0' i.e. to move the membrane to the upper position, we apply a pulse whose amplitude is high enough to make the displacement from the equilibrium low so that the restoring force can not overcome the barrier even when opposed by the electrostatic force between the plates.

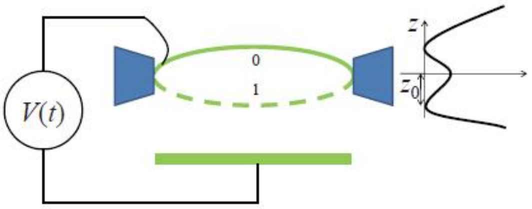


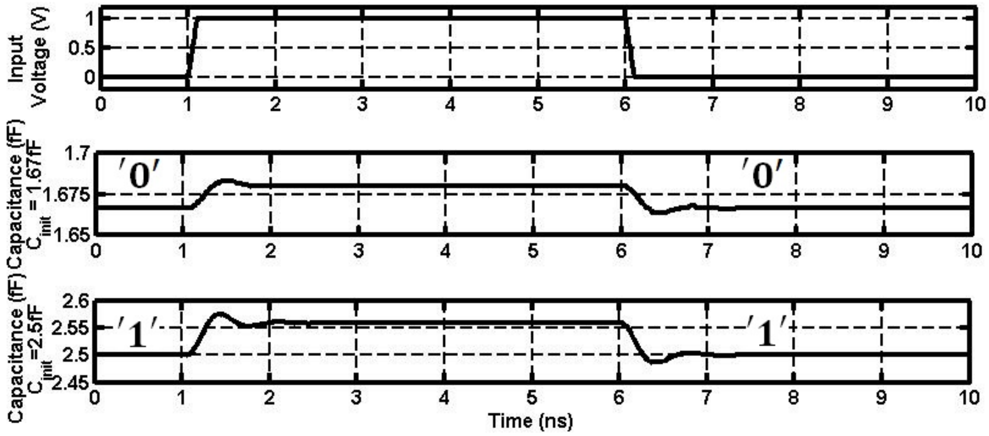
Figure 3.1: The elastic membrane memcapacitor [30].

To simulate the previous operation of the elastic membrane, we will assume that: $\omega_o = 2*\pi*1Grad/s$, $C_0 = 2fF$, $m = 1pg$ and $d = 1nm$, while we will use the same values in [30] for $y_o = 0.2$ and $\zeta = 0.7$. The two states of the device based on these parameters are

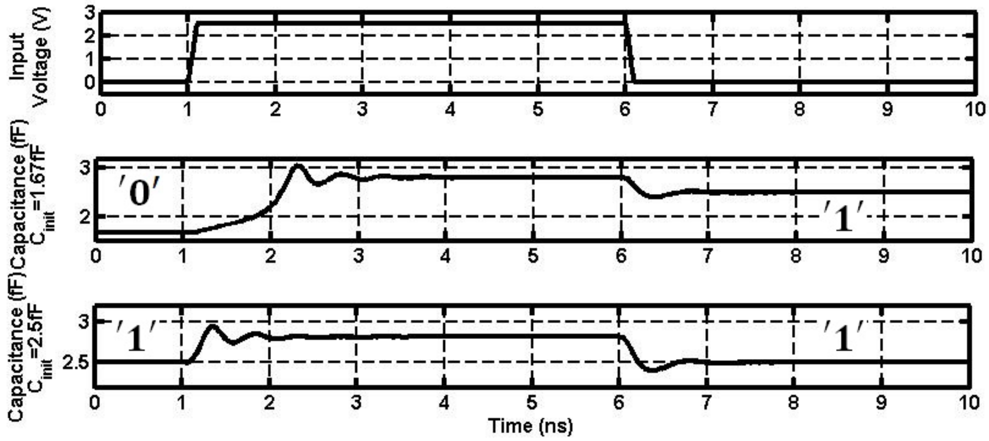
$C_{on} = 1.67fF$ and $C_{off} = 2.5fF$. Based on the previous assumptions, we developed the following Verilog-A model similar to the one used for memristors in [19]

```
‘include “constants.vams”
‘include “disciplines.vams”
nature Voltage
access = V;
units = “V”;
abstol = 1e9;
blowup = 1e100;
endnature
module memcap(p,n);
inout p, n;
electrical p, n;
parameter real y_init = 0.2;
parameter real dydt_init = 0;
parameter real q_init = 0;
parameter real w0 = 2*3.14*1G;
parameter y0 = 0.2;
parameter real z = 0.7;
parameter real C0 = 2f;
parameter real m = 1f;
parameter real d = 1n;
real y, dydt, d2ydt2, q, i;
analog begin
q = idt(I(p,n),q_init);
d2ydt2 = -pow(w0,2)*y*(pow(y,2)/pow(y0,2)-1) -2*z*w0*V(dydt)
    -C0*pow(V(p,n),2)/(2*m*pow(d*(1+y),2));
dydt = idt(V(d2ydt2),dydt_init);
y = idt(V(dydt),y_init);
V(p,n) <+ q*(1+y)/C0;
end
endmodule
```

Using this model, the circuit in Fig. 3.1 is simulated for different values of the voltage pulse of duration 5ns to test the properties of the device. It has to be noted that a small resistance of 0.1Ω is added to facilitate the calculations for the simulator. Fig. 3.2 shows the application of different magnitudes of voltage pulse and the resulting normalized displacement. Using the assumed parameters, it was found that pulse amplitude below 2V does not change the state of the memcapacitor as shown in Fig. 3.2a, amplitudes between 2V and 5V drive the memcapacitor to state ’1’ as shown in Fig. 3.2b and pulse amplitudes larger than 5V drive the memcapacitor to state ’0’ as shown in Fig. 3.2c. The memcapacitor in this case needs $4/(\zeta\omega_o) \approx 1ns$ for its value to settle.

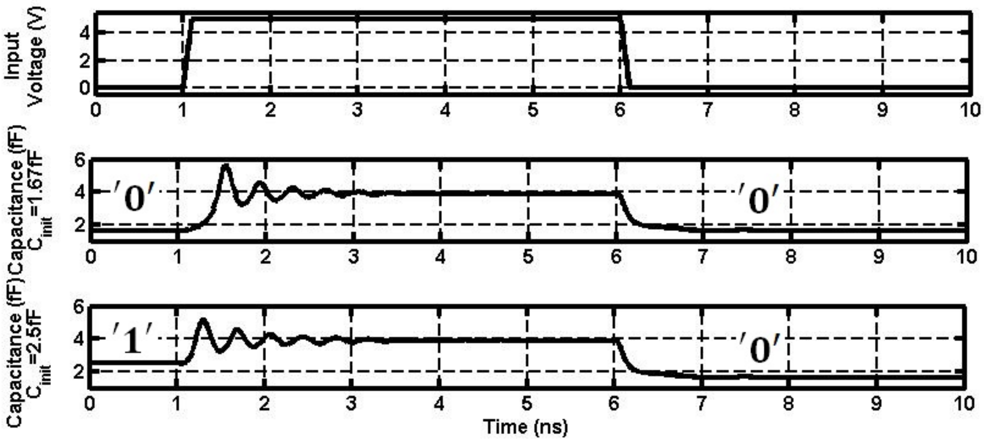


(a) Pulse amplitude of 1V leaves the state unchanged, in the middle slot the memcapacitor starts at state ’0’ ($C = 1.67fF$) and ends in it, and in the lower slot the memcapacitor starts at state ’1’ ($C = 2.5fF$) and ends in it also.



(b) Pulse amplitude of 2.5V drives the memcapacitor to state ’1’, in the middle slot the memcapacitor starts at state ’0’ but ends in state ’1’, while in the lower slot the memcapacitor starts at state ’1’ and ends in it.

Figure 3.2: Simulation results of the application of voltage pulse of duration 5ns to the memcapacitor.



(c) Pulse amplitude of 5V drives the memcapacitor to state '0', in the middle slot the memcapacitor starts at state '0' and ends in it, while in the lower slot the memcapacitor starts at state '1' but ends in state '0'.

Figure 3.2: Simulation results of the application of voltage pulse of duration 5ns to the memcapacitor.

3.2 Crossbar memory array

The crossbar structure of the memory array is composed of memory cells placed at intersection points between upper and lower bars where the upper bars are placed in the form of columns and the lower bars are placed in the form of rows. The upper bars are aligned perpendicular to the lower bars. The memristive crossbar memory array uses memristors as memory cells at the intersection between bars as shown in Fig. 3.3. To select a memory cell, the corresponding row and column are selected. Crossbar memory array can be gated or non-gated. The cell in the gated crossbar memory array is associated with a switch, which is commonly a transistor, to isolate the intended cell from the other cells. To select a certain cell, the switch associated with this cell is turned on while all other switches are turned off. This allows current to pass only through the intended cell and hence, its information is retrieved by reading the current value which depends on the cell state. In the non-gated crossbar memory array, the cells are not isolated with switches; this makes the memory array denser by saving the switches area but causes the sneak paths problem to appear. The problem of the sneak paths arises because when a certain cell is selected, current does not flow in this cell only but can find other paths between the selected row and column as shown in Fig. 3.3. This causes a problem when we sense the value of the selected cell to read the stored information as the other paths parallel to the path through the selected cell will contribute to the current that holds the information of the reading.

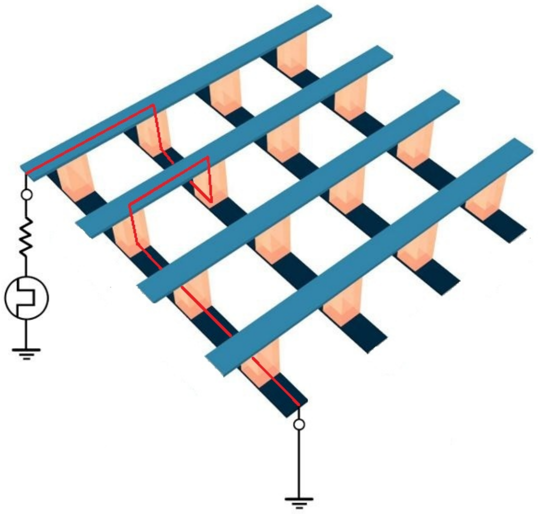


Figure 3.3: The structure of crossbar array. An example of a sneak path is shown in red.

Several methods were proposed to solve the sneak paths problem in the memristive memory array [43–45]. The method in [45] needs many read and write operations to be performed. The method is as follows: 1) The selected cell is read. 2) A value of ’1’ is written to the selected cell and then the value of the cell is read. 3) A value of ’0’ is written to the selected cell and then the value of the cell is read. 4) The initial reading is compared to the two reading of ’0’ and ’1’ to decide the initial information that was stored in the cell. 5) Finally, the retrieved information is written again to the selected cell. The method proposed in [43] relies on using another memristor as a selection device instead of the transistor in series with the information-storing memristor and the node between the two memristors is used for programming the selection memristor. The two in-series memristors with the intermediate node resembles a three terminal device called the “memistor” introduced in [46] which acts like a transistor with memory. This method has fewer operations than the previous one but does not fully eliminate the sneak paths effect but rather greatly weakens their effect. A more advantageous method is the one presented in [44] as it fully eliminates the effect of the sneak paths with only three readings then performing addition and subtraction operation on these readings which will be discussed in detail in the next subsection.

3.2.1 Reading process

The method presented in [44] can be generalized to any gate-less crossbar memory array and not strictly memristive array. Therefore, we will use impedance instead of resistance through the analysis. We assume that the intended cell has impedance Z_m which has one of two possible values: low impedance Z_{on} or high one Z_{off} . When a cell is sensed, the cell has some parallel paths whose effect is sensed too with the required cell to sense in the array as shown in Fig. 3.3. So, we have two variables which are the impedance of required cell and the equivalent impedance of the parallel paths. This is equivalent in mathematics to having one equation and solving for two variables. The selected cell and the parallel paths are analogous to the two variables and the reading is analogous to the equation. But since we have only one reading, we need other information to calculate the value of the required cell. To get more readings, the selected column is connected to node n_1 , the selected row is connected to node n_2 , all the unselected columns are shorted together and connected to node n_3 and all the unselected rows are shorted together and connected to node n_4 as shown in Fig. 3.4. By doing this, we have four nodes and so we can make six readings and we have four variables: the impedance Z_m of the required cell which is between the nodes n_1 and n_2 , the impedance Z_c of the cells along the column of the selected cell other than the required cell which are between the nodes n_2 and n_3 , the impedance Z_r of the cells along the row of the selected cell other than the required cell which are between the nodes n_1 and n_4 and the impedance Z_a of the cells that are not along neither the row nor the column of the required cell which are between the nodes n_3 and n_4 , this is shown in the right panel of Fig. 3.4. We need four readings to solve for four variables but if we lump Z_a and Z_r or Z_a and Z_c as one impedance and let the node between them be floating, then we have three variables only and it is sufficient to make three readings between the three combinations of three left nodes to get the value of Z_m . For example, if we sense the resistance between nodes (n_1 and n_2), (n_1 and n_3) and (n_2 and n_3) while n_4 is let floating, the expressions of the impedance read are expressed in eq.s 3.6, 3.7 and 3.8:

$$Z_{1,2} = \frac{Z_m Z_c + Z_m Z_a + Z_m Z_r}{Z_m + Z_c + Z_a + Z_r} \tag{3.6}$$

$$Z_{2,3} = \frac{Z_c Z_m + Z_c Z_r + Z_c Z_a}{Z_m + Z_c + Z_a + Z_r} \tag{3.7}$$

$$Z_{1,3} = \frac{Z_m Z_r + Z_m Z_a + Z_c Z_r + Z_c Z_a}{Z_m + Z_c + Z_a + Z_r} \tag{3.8}$$

Solving for Z_m we get the expression in eq. 3.9:

$$Z_m = \frac{1}{2}(Z_{1,2} - Z_{2,3} - Z_{1,3}) - \frac{2Z_{2,3}Z_{1,3}}{Z_{1,2} - Z_{2,3} - Z_{1,3}} \tag{3.9}$$

Which can be written as in eq. 3.10:

$$Z_{1,2} = Z_{2,3} + Z_{1,3} + Z_m \pm \sqrt{4Z_{2,3}Z_{1,3} + Z_m^2} \tag{3.10}$$

In [44], it is assumed that in case of Z_{on} , the minus sign is chosen at eq. 3.10 while the plus sign is chosen in case of Z_{off} . But since $Z_{1,2} < Z_m$ because $Z_{1,2}$ is composed of Z_m parallel to other impedances, only the minus sign of the square root can be taken in eq. 3.10.

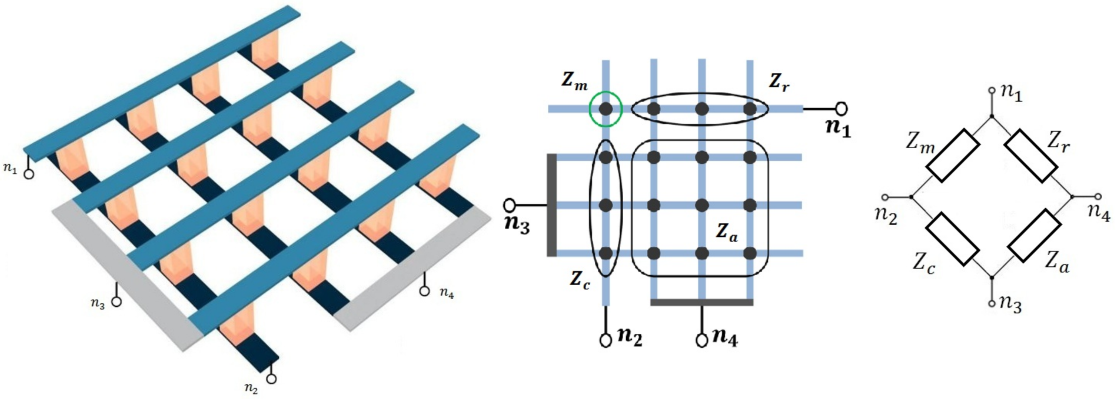


Figure 3.4: The 3D view for crossbar structure after connecting the terminals of the intended cell between n_1 and n_2 , shorting all the unselected columns and connecting them to node n_3 and shorting all the unselected rows and connecting them to node n_4 is shown on the left. The top view of the array showing cells contributing to each lumped impedance is shown in the middle. The equivalent impedance network on the right.

In order to define a threshold, it has to be noted that $Z_{2,3}$ and $Z_{1,3}$ are composed of parallel paths and most probably at least one of the cells in these parallel paths is Z_{on} and so, they are much less than Z_m . So, we can assume that: $4Z_{2,3}Z_{1,3} \ll Z_m^2$. Using Taylor's expansion, we can use the approximation in eq. 3.11:

$$\sqrt{4Z_{2,3}Z_{1,3}+Z_m^2} \approx \frac{2Z_{2,3}Z_{1,3}}{Z_m}+Z_m \tag{3.11}$$

So, eq. 3.10 reduce to the expression in eq. 3.12:

$$Z_{1,2} \approx Z_{2,3}+Z_{1,3}-\frac{2Z_{2,3}Z_{1,3}}{Z_m} \tag{3.12}$$

Since Z_m has only two possible values which are Z_{on} and Z_{off} , $Z_{1,2}$ has two possible expressions: 1) eq. 3.13 when $Z_m = Z_{on}$:

$$Z_{1,2} = Z_{2,3}+Z_{1,3}-\frac{2Z_{2,3}Z_{1,3}}{Z_{on}} \tag{3.13}$$

And 2) eq. 3.14 when $Z_m = Z_{off}$:

$$Z_{1,2} = Z_{2,3}+Z_{1,3}-\frac{2Z_{2,3}Z_{1,3}}{Z_{off}} \tag{3.14}$$

The values of $Z_{1,2}$, $Z_{1,3}$ and $Z_{2,3}$ have expected values that depends on the size of the array if the number of the cells storing the value '0' is nearly the number of cells storing the value '1'. They approach their expected values as the size of the array increases. We define an impedance Z_t in eq. 3.15:

$$Z_t = Z_{2,3}+Z_{1,3}-Z_{1,2} = \frac{2Z_{2,3}Z_{1,3}}{Z_m} \tag{3.15}$$

As the size of the array increases and as the Z_{off}/Z_{on} ratio increases, a threshold value for Z_t can be defined. So, by using this method, we do not need to solve for Z_m , but instead a simple addition and subtraction circuitry only is needed to calculate Z_t in terms of the sensed impedances $Z_{1,2}$, $Z_{1,3}$ and $Z_{2,3}$ which is then compared to the defined threshold value $2Z_{2,3}Z_{1,3}/Z_{av}$, where Z_{av} is the average impedance between Z_{off} and Z_{on} , if Z_t is larger than this threshold then $Z_m = Z_{on}$, otherwise $Z_m = Z_{off}$. If we assume a square array of size $n \times n$, we have on average half the cells of value Z_{on} and the other half of value Z_{off} . From Fig. 3.4, Z_r and Z_c are composed of $n-1$ parallel cells each while Z_a is composed of $(n-1)^2$ cells. Therefore, we can get the expected values of Z_r , Z_c and Z_a in eq.s 3.16 and 3.17:

$$E(Z_c) \quad = \quad E(Z_r) = \frac{2(Z_{off}//Z_{on})}{n-1} \tag{3.16}$$

$$E(Z_a) \quad = \quad \frac{2(Z_{off}//Z_{on})}{(n-1)^2} \tag{3.17}$$

We note from eq.s 3.16 and 3.17 that in large enough arrays, Z_a can be neglected when placed in series with Z_c or Z_r , and the latters can be neglected when placed in series to Z_m . The situation is reversed when they are placed in parallel. Consequently, the expected values of $Z_{1,2}$, $Z_{1,4}$ and $Z_{2,4}$ are as shown in eq.s 3.18 and 3.19:

$$\begin{aligned} E(Z_{1,2}) &= E\left(Z_m//(Z_c+Z_r+Z_a)\right) \\ &\approx E(Z_m//2Z_r) \approx 2E(Z_r) = \frac{4(Z_{off}//Z_{on})}{n-1} \end{aligned} \tag{3.18}$$

$$\begin{aligned} E(Z_{1,3}) = E(Z_{2,3}) &= E\left((Z_m+Z_c)//(Z_r+Z_a)\right) \\ &\approx E(Z_m//Z_r) \approx E(Z_r) = \frac{2(Z_{off}//Z_{on})}{n-1} \end{aligned} \tag{3.19}$$

And hence from eq. 3.15, the threshold for Z_t can be defined in eq. 3.20:

$$Z_{th} \quad = \quad \frac{8(Z_{off}//Z_{on})^2}{(n-1)^2 Z_{av}} \tag{3.20}$$

The previous method can be applied to the memcapacitive network array with the same equations with replacing each impedance Z with the multiplicative inverse of the corresponding memcapacitance $1/C$.

3.2.2 Parasitic Effects

3.2.2.1 Capacitive coupling between adjacent bars

By considering the parasitic effects in the memory array such as the resistance of the bars and the coupling between them, a problem arises. The coupling capacitances between the bars can cause serious problems if these coupling capacitances are of the same order of magnitude or higher than the memcapacitances of the memory cells. This is due to the fact that the equations used are based on the network in Fig. 3.4, but when the coupling capacitances are considered, new impedances must be added to the figure to model the coupling capacitance. As shown in Fig. 3.5a, there is an added capacitance between n_1 and n_3 to model the coupling between the columns, and another one between n_2 and n_4 to model the coupling between the rows. The dominant coupling capacitances are the capacitance between the selected upper bar connected to n_1 and the adjacent unselected bars and the capacitance between the selected lower bar connected to n_2 and the adjacent unselected bars. From Fig. 3.5a, we now have six variables and so, we need now six reading instead of three to estimate C_m as well as solving six non-linear equations to get a closed-form expression for C_m .

To solve this problem, we decided to short the nodes n_3 and n_4 . By doing this, there are now only three variables and three nodes again as shown in Fig. 3.5b and we get three readings and solve for C_m using the same previous equations but with slight modification to account for the effect of the parasitic capacitance on the defined threshold of Z_t . If we assume that the coupling capacitance per cell whose value depends on the dimensions of the cell in the memory array is C_p and the corresponding impedance is Z_p , the total impedance between the selected row or column and its two adjacent ones is $Z_p/2n$ except for the cells at the borders of the memory array which would have twice that value either between adjacent rows or columns or both if they are at the corner of the memory array. In order to unify the value of the total coupling capacitance for all cells of the memory array, two extra rows are added; one at each side of the array, and similarly for columns. Now, the modified expected values are shown in eq. 3.21:

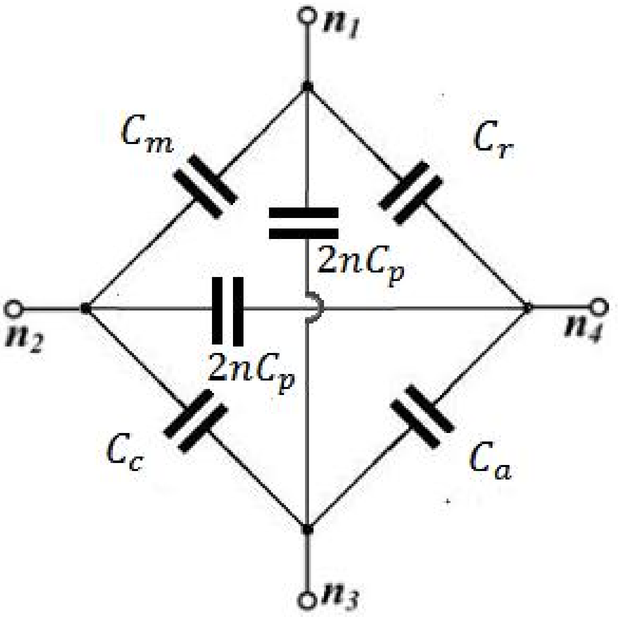
$$E(Z_{1,3}) = E(Z_{2,3}) = \frac{2(Z_{off}//Z_{on})}{n-1}//\frac{Z_p}{2n} \tag{3.21}$$

And the new threshold for Z_t can be defined in eq. 3.22:

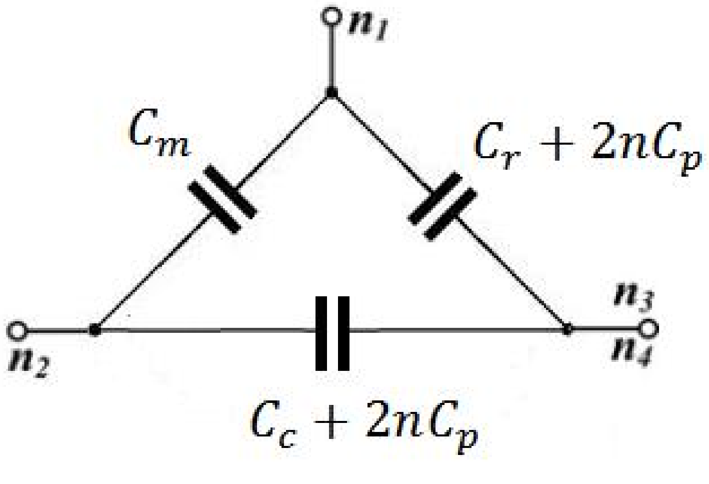
$$Z_{th} = \frac{2}{Z_{av}}\left(\frac{2(Z_{off}//Z_{on})}{n-1}//\frac{Z_p}{2n}\right)^2 \tag{3.22}$$

3.2.2.2 Parasitic resistance of the bars

The parasitic resistances of the bars also degrade the reading as the applied voltage is reduced across the bars. To solve the parasitic effect of the resistance of the bars, reading is performed by applying a voltage pulse to the circuit shown in Fig. 3.6. At steady state of the pulse, the effect of the resistors is eliminated because there is no path free from capacitors and memcapacitors from the source to the ground, and so, the sensed voltage depends only on the values of the memcapacitors and the parasitic coupling capacitors whose effect is eliminated by shorting n_3 and n_4 as shown previously. So, the sensed voltage is proportional to the inverse of the capacitance between the two selected terminals of the memory array. As shown in Fig. 3.6, the circuit is sensing the capacitive reactance of $Z_{1,2}$ and the sensed voltage is shown in eq. 3.23:



(a) Before shorting n_3 and n_4.



(b) After shorting n_3 and n_4 .

Figure 3.5: The equivalent capacitive network in the crossbar structure of a memcapacitive memory array similar to the memristive array in Fig. 3.4 after taking in consideration the effect of the coupling capacitance between bars.

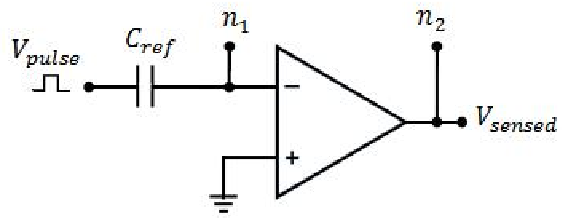


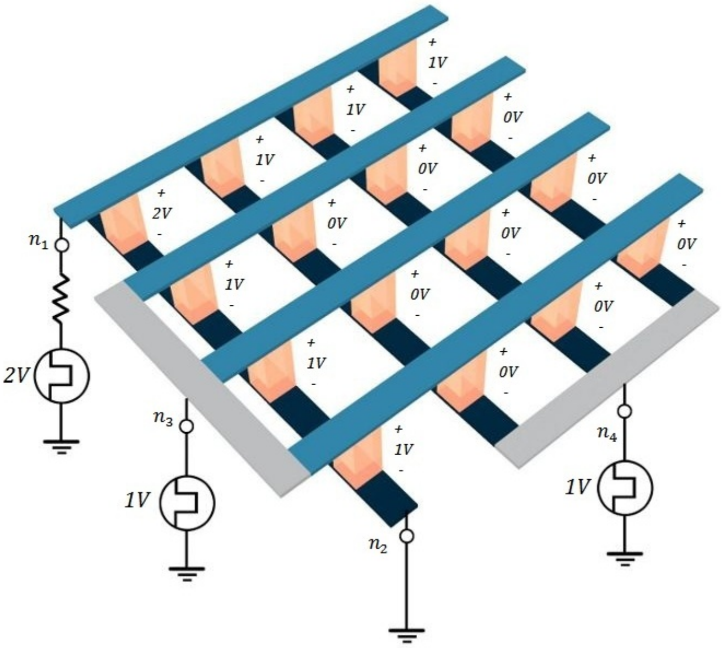
Figure 3.6: A voltage pulse is applied to the circuit to sense the capacitive reactance between the intended terminals (e.g. n_1 and n_2) of the array.

$$V_{sensed} = -\frac{C_{ref}}{C_{1,2}} V_{pulse} \tag{3.23}$$

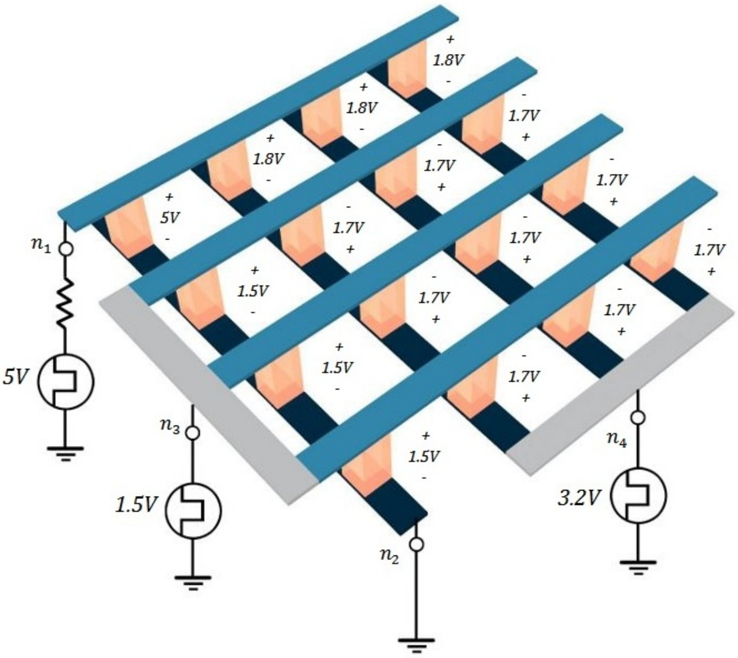
It has to be noted that the value of V_{sensed} must be chosen below the value that would change the memcapacitors' state to avoid destruction of information while reading. The value of C_{ref} can be used to scale the sensed values. In order to get rid of the minus sign in the value of V_{sensed} in case of $Z_{1,3}$ and $Z_{2,3}$, a negative pulse is applied to the circuit.

3.2.3 Writing Process

Considering the writing process to the crossbar array: When a voltage pulse is applied to the elastic membrane memcapacitor with the assumed parameters, we have three situations as discussed earlier: if the pulse amplitude is less than 2V, no change in the state of the memcapacitor, if the pulse amplitude is between 2V and 4.8V, the memcapacitor is driven to state '1' and if the pulse amplitude is larger than 5V, the memcapacitor is driven to state '0'. When we write information to a certain cell, we want to be sure other cells' states are unaffected. To do this will use a technique similar to the one introduced in [47] for memristive crossbar memory array. To write '1' to a memcapacitor cell, a voltage pulse of amplitude 2V is applied to node n_1 while n_2 is grounded. To be sure the other cells are not affected a voltage pulse of amplitude greater than 0V but less than 2V, for example 1V, is applied to nodes n_3 and n_4 . This means that the pulse applied to the cells between n_1 and n_4 is 1V, the pulse applied to the cells between n_3 and n_2 is 1V and the pulse applied to the cells between n_3 and n_4 is 0V. The writing of state '1' is shown in Fig. 3.7a. To write '0' to a memcapacitor cell, a voltage pulse of amplitude 5V is applied to node n_1 while n_2 is grounded. Also, to be sure the other cells are not affected, a voltage pulse of amplitude greater than 0V but less than 2V, for example 1.5V, is applied to node n_3 and a pulse lower than 5V by no more than 2V (greater than 3V) but more than the pulse applied to n_3 by no more than 2V (less than 3.5V), for example 3.2V, is applied to node n_4 . This means that the pulse applied to the cells between n_1 and n_4 is 1.8V, the pulse applied to the cells between n_3 and n_2 is 1.5V and the pulse applied to the cells between n_3 and n_4 is -1.7V. The writing of state '0' is shown in Fig. 3.7b. So, this way ensures that the unselected cells are unaffected by the write process.



(a) Writing state ’1’.



(b) Writing state ’0’.

Figure 3.7: The write process and the voltage across the array cells.

Table 3.1: Reading process for different array parameters against proposed threshold.

$C_p(F)$	$R_l(\Omega)$	$C_{ref}(F)$	$C_m(F)$	$\frac{C_{ref}}{C_{12}}$	$\frac{C_{ref}}{C_{13}}$	$\frac{C_{ref}}{C_{23}}$	$E\left(\frac{C_{ref}}{C_{12}}\right)$	$E\left(\frac{C_{ref}}{C_{13/23}}\right)$	$E\left(\frac{C_{ref}}{C_{13}}\right)+E\left(\frac{C_{ref}}{C_{23}}\right)-E\left(\frac{C_{ref}}{C_{12}}\right)$	$E\left(\frac{C_{ref}}{C_{th}}\right)$
100a	100m	0. 25p	2.5f	1.66234	850.68m	826.834m	1.723	861.5m	15.174m	11.875m
1f	10m	0.25p	2.5f	945.492m	478.874m	471.284m	960m	480m	4.666m	3.6864m
10f	100m	1p	2.5f	706.122m	353.905m	352.858m	708m	354m	0.641m	0. 5012m
100a	100m	0.25p	1.67f	1.67248	853.102m	829.125m	1.723	861.5m	9.747m	11.875m
1f	10m	0.25p	1.67f	948.618m	479.641m	472.025m	960m	480m	3.048m	3.6864m
10f	100m	1p	1.67f	706.34m	352.962m	353.8m	708m	354m	0.422m	0. 5012m

Table 3.2: Settling time of read process for different array parameters.

Array size	$C_p(F)$	$R_l(\Omega)$	$3n^2R_lC_p(s)$	Settling time (s) ($\pm 2\%$ of V_{final})
128x128	1f	1	49.152p	53.629p
128x128	1f	2	98.304p	98.20661p
128x128	1f	3	147.456p	142.8124p
128x128	2f	1	98.304p	97.1086p
128x128	3f	1	147.456p	143.096p
128x64	1f	1	24.576p	27.3576p
64x64	1f	1	12.288p	11.93445p

3.3 Simulation results

The previous approach was tested for memory array size of 128×128 of randomly distributed data in which the method is used to read the value of the cell in the 70th row and 50th column and the results are summarized in Table 3.1 for different values for the coupling capacitances between adjacent bars per cell and bars' resistances per cell. For the chosen parameters, the read time is dominated by the array parameters and not the memcapacitor's parameters. As the results show, the values read from the array changes with the value of the coupling capacitance while bar resistance has no effect and hence, the corrected threshold, that takes coupling capacitance into consideration, must be used to differentiate between ON and OFF values.

To test the read time needed to sense the value of a cell in the memory array, a voltage pulse is applied on a voltage divider consisting of a capacitor in series with the memory array and measure the settling time of the voltage on the memory array. The results are summarized in Table 3.2. Since the values of C_p and R_l are determined by the array size and the materials used in the array fabrication, the results shows that the reading operation speed is determined by the array parameters and not by the memcapacitor's parameters.

3.4 Conclusion

The aim of this chapter is to propose a new approach to achieve the goals of ITRS [41]. We present a Verilog-A model of elastic membrane memcapacitor and use it to simulate the functionality of a single memory cell and a large crossbar memory array. The use of memcapacitors instead of the regular capacitors which exist in DRAM memories has the potential to significantly reduce the power consumed due to the elimination of refresh cycles. The use of a gate-less crossbar structure increases the density of the array. This chapter generalizes the previous approach to solve the sneak paths problem even when the crossbar coupling resistances and capacitances are included. The simulation results indicate that our approach is very viable to produce a non-volatile high-density low-power memory. Due to the lack of fabricated memcapacitor-based memory cells, we will switch back to memristors and discuss memristor-based memory arrays in the next chapter.

Chapter 4

Optimizing threshold

In this chapter, we analyze the threshold used for detecting the information stored at the memory cell by the method introduced in [44] as well as showing the limitations on this threshold. Also, we analyze the effect of the 0/1 distribution in the memory array on the correctness of the readout as well as the method of choice of the threshold to minimize this effect. We also propose an adaptive threshold that can detect the cell value at any 0/1 distribution and is updated either statically or dynamically. Finally, a circuit for performing the three readings without the need to store and then restore the readings is proposed. Our technique is generic enough to be used in crossbar memories with other cells such as memcapacitors.

4.1 Threshold Analysis

As shown in Chapter 3, the threshold value in eq. 3.20 depends on the value of the mean resistance between the ON and OFF values. The mean has to be chosen taking into consideration that the instantaneous distribution of cells in a memory is not uniform between 0's and 1's. So, we must study how much the distribution can deviate from the uniform one such that the detection process does not fail and whether the mean choice can affect this. Throughout the analysis, we will assume that the OFF/ON impedance ratio is $r = R_{off}/R_{on}$ and we will define R_{av} as the generalized mean of R_{on} and R_{off} defined in eq. 4.1:

$$R_{av} \quad = \quad \sqrt[p]{\frac{1}{2}\left(R_{on}^{p} + R_{off}^{p}\right)} = R_{on}\left(\sqrt[p]{\frac{1}{2}(1+r^{p})}\right) \tag{4.1}$$

Where p is a real number which can be positive (e.g. arithmetic mean with $p = 1$ where $R_{av} = \frac{1}{2}\left(R_{on} + R_{of}\right)$), negative (e.g. harmonic mean with $p = -1$ where $\frac{1}{R_{av}} = \frac{1}{2}\left(\frac{1}{R_{on}} + \frac{1}{R_{off}}\right)$) and converges to the geometric mean as $p \to 0$ ($\lim\limits_{p\to 0} R_{on}\left(\sqrt[p]{\frac{1}{2}(1+r^{p})}\right) = R_{on}\sqrt{r} = \sqrt{R_{on}R_{off}}$). The value of p in the generalized mean of two values R_{on} and R_{off} allows the mean to span from $R_{av} = R_{on}$ when $p \to -\infty$ ($\lim\limits_{p\to -\infty} R_{on}\left(\sqrt[p]{\frac{1}{2}(1+r^{p})}\right) = R_{on}$)

to $R_{av} = R_{off}$ when $p\rightarrow\infty$ ($\lim\limits_{p\rightarrow\infty} R_{on}\left(\sqrt[p]{\frac{1}{2}(1+r^p)}\right) = R_{on}r = R_{off}$). We will analyze the readout method to choose the optimum average (optimum value of p) for a given array. To simplify the analysis, the row and the column of the selected cell are assumed to have the same ratio x of R_{on} cells (where x =(number of R_{on} cells)/(Total number of cells)), this gives eq.s 4.2 and 4.3:

$$R_c = R_r = \frac{R_{off}}{(1-x)(n-1)} // \frac{R_{on}}{x(n-1)} \tag{4.2}$$

$$R_a = \frac{R_{off}}{(1-x)(n-1)^2} // \frac{R_{on}}{x(n-1)^2} \tag{4.3}$$

And consequently, eq.s 4.4 and 4.5:

$$R_{1,2} = \frac{2R_{off}}{(1-x)(n-1)} // \frac{2R_{on}}{x(n-1)} \tag{4.4}$$

$$R_{1,3} = R_{2,3} = \frac{R_{off}}{(1-x)(n-1)} // \frac{R_{on}}{x(n-1)} \tag{4.5}$$

From eq. 3.15 in Chapter 3, we conclude that the following two conditions in eq.s 4.6 and 4.7 must be satisfied:

$$\frac{2R_{2,3}R_{1,3}}{R_{on}} > R_{th} \tag{4.6}$$

$$\frac{2R_{2,3}R_{1,3}}{R_{off}} < R_{th} \tag{4.7}$$

From eq.s 3.20, 4.1, 4.5, and 4.6, we get the upper bound on x that leads to correct detection of the memory cell value in eq. 4.8:

$$\frac{2}{R_{on}}\left(\frac{R_{off}}{(1-x)(n-1)} // \frac{R_{on}}{x(n-1)}\right)^2 > \frac{8\left(R_{off}//R_{on}\right)^2}{(n-1)^2 R_{av}} \tag{4.8}$$

Which can be reduced to eq. 4.9:

$$x < \frac{(r+1)\left(\sqrt[2p]{\frac{1}{2}(1+r^p)}\right)-2}{2(r-1)} \tag{4.9}$$

For small OFF/ON ratio ($r \rightarrow 1$), we get eq. 4.10:

$$x < \frac{3}{4} \tag{4.10}$$

While for large OFF/ON ratio ($r \gg 1$), we get eq. 4.11:

$$x < \begin{cases} \frac{\sqrt{r}}{2\left(\sqrt[2p]{2}\right)} & p > 0 \\ \frac{1}{2\left(\sqrt[2p]{2}\right)} & p < 0 \\ \frac{\sqrt[4]{r}}{2} & p\rightarrow 0 \end{cases} \tag{4.11}$$

Similarly, from eq.s 3.20, 4.1, 4.5, and 4.7, we get the lower bound on x for correct detection in eq. 4.12:

$$\frac{2}{R_{off}}\left(\frac{R_{off}}{(1-x)(n-1)}//\frac{R_{on}}{x(n-1)}\right)^2 \quad > \quad \frac{8\left(R_{off}//R_{on}\right)^2}{(n-1)^2 R_{av}} \tag{4.12}$$

Which can be reduced to eq. 4.13:

$$x \quad > \quad \frac{\frac{1}{\sqrt{r}}(r+1)\left(\sqrt[2p]{\frac{1}{2}(1+r^p)}\right)-2}{2(r-1)} \tag{4.13}$$

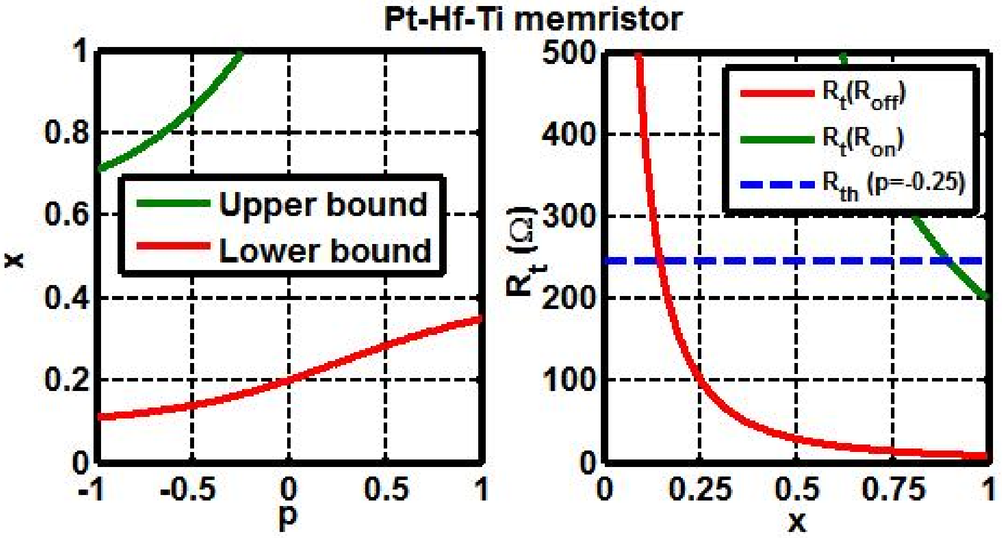
For small OFF/ON ratio ($r \rightarrow 1$), we get eq. 4.14:

$$x \quad > \quad \frac{1}{4} \tag{4.14}$$

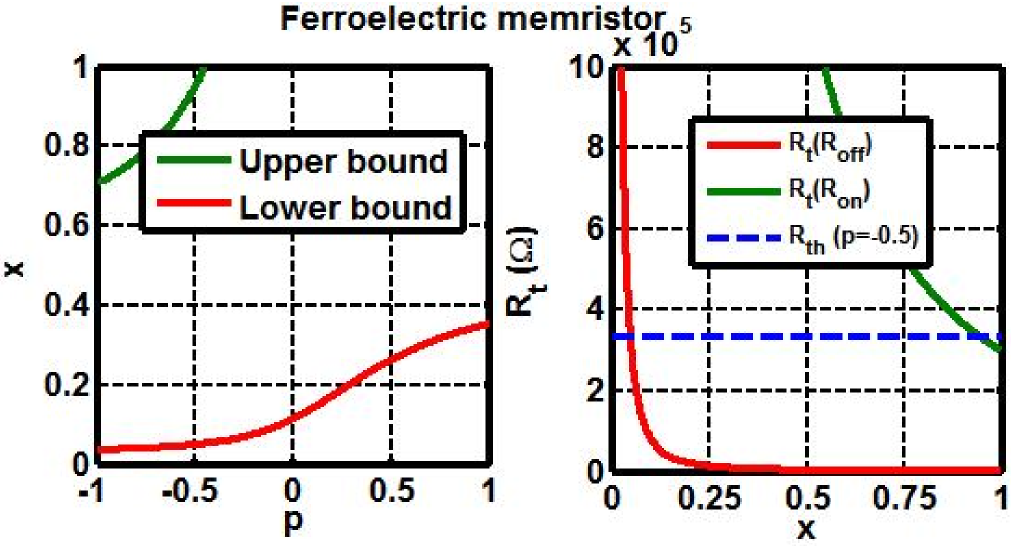
While for large OFF/ON ratio ($r \gg 1$), we get eq. 4.15:

$$x \quad > \quad \begin{cases} \frac{1}{2\left(\sqrt[2p]{2}\right)} & p > 0 \\ \frac{1}{2\left(\sqrt[2p]{2}\right)\sqrt{r}} & p < 0 \\ \frac{1}{2\left(\sqrt[4]{r}\right)} & p \rightarrow 0 \end{cases} \tag{4.15}$$

From the previous analysis, we see that the value of p is insignificant to the boundaries of x for small r . While in case of large r , for the positive values of p , increasing r raises the upper bound on x but p must be small to lower the lower bound. While for negative values of p , increasing r lowers the lower bound on x . The case of $p \rightarrow 0$ has the advantage of both cases but the effect of r is suppressed compared to them due to the presence of the fourth root instead of the square root. It has to be noted that the value of p can be chosen according to the value of r of the memristor. To see this, the effect of p on the boundaries of x of three memristors: Pt-Hf-Ti [32], ferroelectric [7], and metallic nanowire [48], and a memcapacitor (the elastic membrane memcapacitor [30]), is simulated and the results were plotted in Fig. 4.1 on the right. The parameters used for the three memristors were taken from the VTEAM model [22], while for the memcapacitor they are taken from [30] using the Verilog-A model in [49]. In Fig. 4.1, the value of p with the highest distance between the boundaries for each memristor is selected and the values of R_t defined by eq. 3.20 in Chapter 3 for both binary values of R_m are plotted against the distribution x in Fig. 4.1 on the left. It is clear from Fig. 4.1c and Fig. 4.1d that the thresholds for the metal nanowire memristor and the elastic membrane memcapacitor cannot withstand large variation from the uniform one. This is due to the small OFF/ON ratio (L=2,1.5 respectively). The previous results are verified by simulations below in section 4.4 [50].

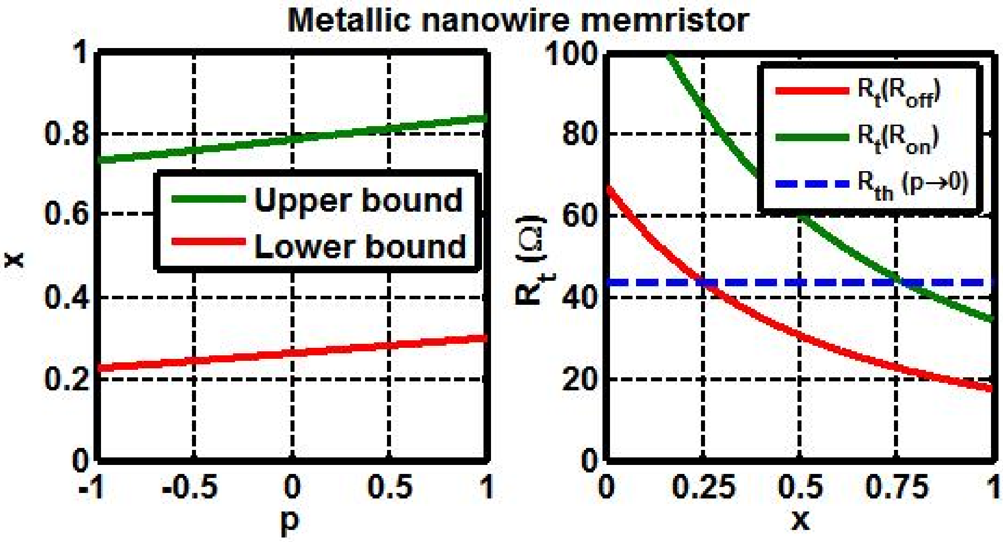


(a) Pt-Hf-Ti memristor: the threshold at $p = -0.25$ is chosen on the right.

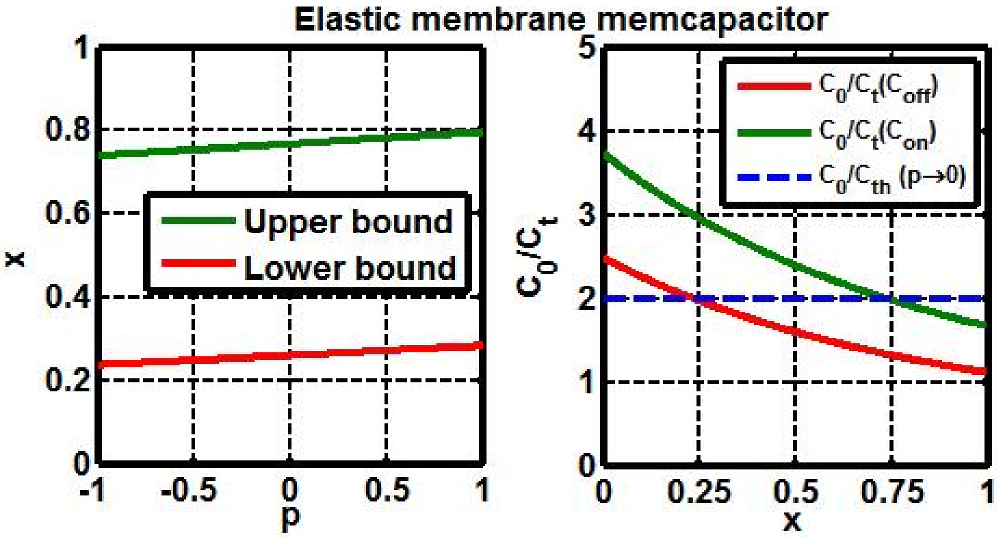


(b) Ferroelectric memristor: the threshold at $p = -0.5$ is chosen on the right.

Figure 4.1: Graph showing the effect of p on the upper and lower boundaries of the fraction of 1's x in the array on the left, and the binary values for R_t as well as the threshold at the value of p that maximizes the range of x versus the fraction of 1's x on the right.



(c) Metallic nanowire memristor: the threshold at $p \rightarrow 0$ is chosen on the right.



(d) Elastic membrane memcapacitor: the threshold at $p \rightarrow 0$ is chosen on the right.

Figure 4.1: Graph showing the effect of p on the upper and lower boundaries of the fraction of 1's x in the array on the left, and the binary values for R_t as well as the threshold at the value of p that maximizes the range of x versus the fraction of 1's x on the right.

4.2 Adaptive threshold

The parameter p in eq. 4.1 is chosen to maximize the range of x (percentage of cells with value of 1) for which the algorithm correctly detects the value of the stored memory cell. It is noted from eq.s 4.11 and 4.14 and shown in Fig. 4.1c and Fig. 4.1d that in case of low OFF/ON ratio, the threshold fails when the 0 or 1 cells is less than quarter of the total cells while in case of large OFF/ON ratio, the threshold fails only at extremely non-uniform distribution between 0's and 1's as shown in Fig. 4.1a and Fig. 4.1b leading to a wide x range. Consequently, we recommend that the array is reset before use to ensure uniform distribution between 0's and 1's to avoid starting at extreme distributions. To overcome the problem of a limited x range in case of low OFF/ON impedance ratio, an adaptive threshold that depends on the ratio between 0's and 1's is introduced. In order to do so, a variable threshold is defined in eq. 4.16:

$$R_{th} = \frac{2R_{2,3}R_{1,3}}{R_{av}} = \frac{2}{R_{av}}\left(\frac{R_{off}}{(1-x)(n-1)}//\frac{R_{on}}{x(n-1)}\right)^2 \approx \frac{2n^2R_{arr}^2}{R_{av}} \tag{4.16}$$

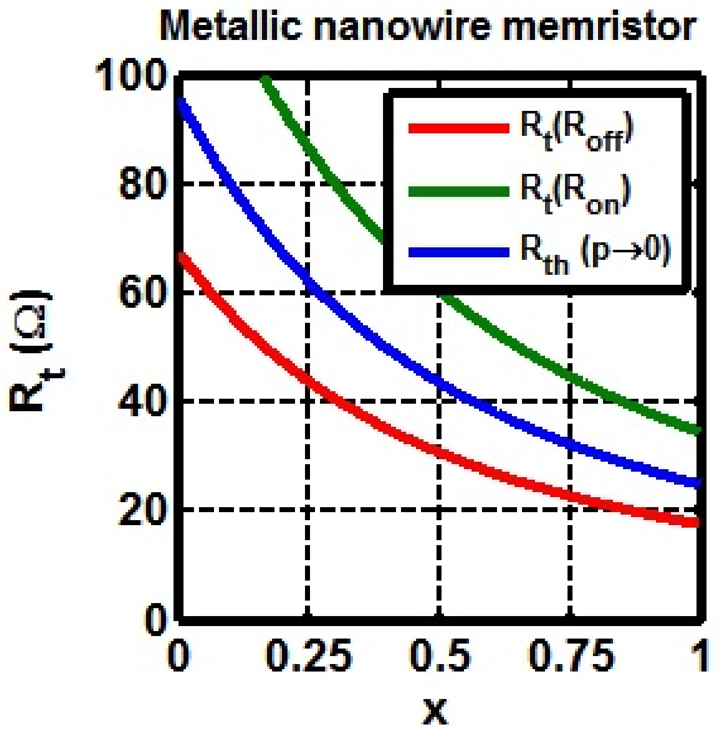
Where R_{arr} is the parallel combination of all the memory cells in the $n \times n$ array and defined in eq. 4.17:

$$R_{arr} = \frac{R_{off}}{(1-x)n^2}//\frac{R_{on}}{xn^2} \tag{4.17}$$

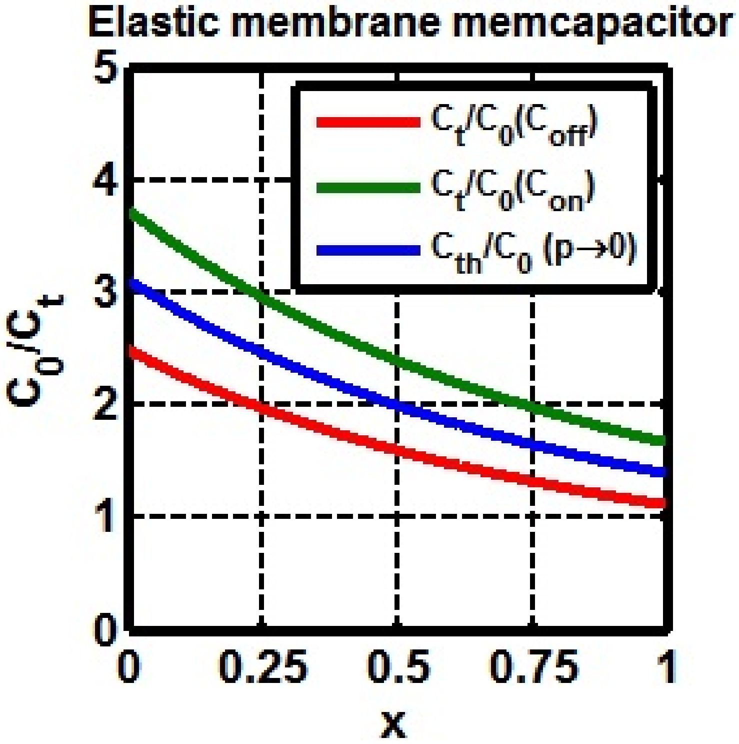
R_{arr} can be measured by shorting n_1 with n_3 and n_2 with n_4 and measuring the resistance R_{arr} between n_1 and n_2 . The adaptive threshold defined by eq. 4.16 is shown in Fig. 4.2a and Fig. 4.2b for the metallic nanowire memristor and the elastic membrane memcapacitor. It is clear that the adaptive threshold is much better compared to the fixed one in Fig. 4.1c and Fig. 4.1d. It increases noise margin at distributions far from the uniform one and decreases the required sensitivity for the measuring circuit significantly. Consequently, the threshold level is chosen based on the measured R_{arr} value. If the ratio x does not change with time, then the chosen threshold value would not need to be changed as well. Fig. 4.2 show that for any given value of x , there exist a threshold level that properly detects the memory cell value. In order to maximize the noise margins, the threshold level can be updated every certain number of write operations in case that the ratio x changes with time. As shown in Fig. 4.2, the bearable deviation is nearly 20% from the initial 0/1 distribution. For example, for an array size of 128×128, the threshold can still detect the stored value after 3000 biased writings. The update can be made either static (i.e. done every fixed number of writings) or dynamic. Dynamic update can be made by means of a counter of range twice the bearable number of writings the threshold can withstand. The counter is reset at each threshold update to half its range. For each '1' writing, the counter counts up, while it counts down for each '0' writing. The threshold is updated when the counter overflows either upwards or downwards. It is clear that dynamic update is more efficient as it saves many unnecessary updates in case writings are, on average, uniformly distributed between 0's and 1's.

4.3 Reading Circuit

In [44] the measurements are applied to an analog-to-digital converter (ADC) to be quantized and applied to a digital arithmetic circuit for add and subtract operations and then to a comparator. This introduces quantization noise to each of the three readings. As obvious from eq.s 3.18, 3.19, and 3.20 in Chapter 3, the measured values' magnitudes



(a) The metallic nanowire memristor.



(b) The elastic membrane memcapacitor.

Figure 4.2: The adaptive threshold versus the density of 1's x .

(which varies with $1/(n-1)$) are very sensitive to the information and are much larger than the final value's magnitude (which varies with $1/(n-1)^2$) especially for large arrays and so, we must avoid quantizing the data before the arithmetic operations.

To perform the three readings without the need for an ADC for quantizing the measured values or a digital arithmetic circuit to add or subtract the sensed resistance values, reading is performed by the circuit shown in Fig. 4.3. The circuit is composed of an inverting amplifier followed by an integrator. The sensed resistance is connected as the feedback resistance of the inverting amplifier so that the output voltage is proportional to the sensed resistance between the two selected terminals of the memory array. The integrator is used to store the value of the read resistance so that the next reading is added or subtracted from it. To read the values, three pulses of equal magnitude are applied sequentially for a duration T , which are separated by zero voltage for a small fraction of T during the switching of the sensed resistance, to read $R_{1,2}$, $R_{1,3}$ and $R_{2,3}$ where the pulse polarity depends on whether the sensed resistance is added or subtracted. As shown in Fig. 4.3, the circuit is sensing the resistance between n_1 and n_2 and a negative pulse is applied, so the sensed voltage V_{sensed} is given by eq. 4.18:

$$V_{sensed} = -\frac{V_pT}{CR^2}R_{1,2} \tag{4.18}$$

The final voltage value after applying a positive pulse when the terminals are connected to n_1 and n_3 , followed by a negative pulse between n_1 and n_2 and another positive pulse between n_2 and n_3 is shown in eq. 4.19:

$$V_{sensed} = \frac{V_pT}{CR^2}(R_{2,3}+R_{1,3}-R_{1,2}) \tag{4.19}$$

The final value is then compared with $R_{th}V_pT/CR^2$ to decide the cell value. The capacitor in the integrator must then be reset after the final output voltage is read so that it does not affect the next reading process. It has to be noted that the value of V_{sensed} at any instant through the reading process must be chosen below the memristor threshold. Hence, reading $R_{1,2}$ should mediate the other two readings as the successive reading of two values of the same sign would increase the value of output voltage unnecessarily. The values of C , R , V_p and T can be used to scale the output voltage. It has to be noted that in the case of memcapacitors, the resistor in the inverting amplifier must be replaced by a capacitor C_0, and V_{sensed} becomes as shown in 4.20:

$$V_{sensed} = \frac{V_pTC_0}{CR}\left(\frac{1}{C_{2,3}}+\frac{1}{C_{1,3}}-\frac{1}{C_{1,2}}\right) \tag{4.20}$$

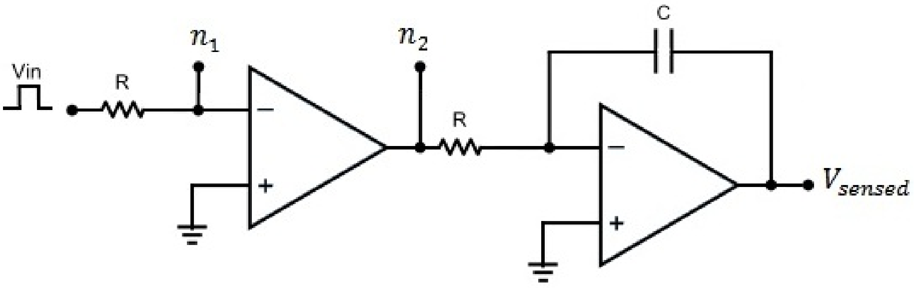


Figure 4.3: Circuit reading the resistance between n_1 and n_2 ($R_{1,2}$).

4.4 Simulation results

4.4.1 Testing various 0/1 distributions and different memristor models

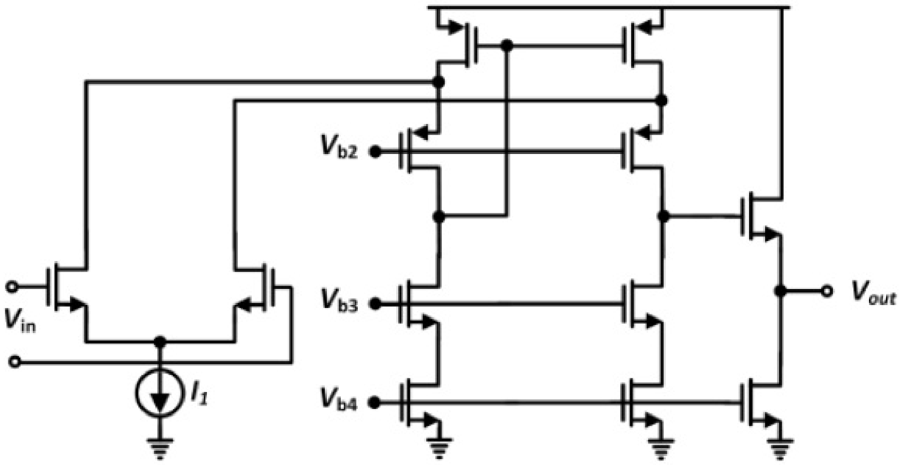
The proposed technique is tested for memory array size of 128×128 of randomly distributed data with different 0/1 probabilities in which the readout method is used to read the value of the cell in the middle of the array (64th row and 64th column) and the results are summarized in Table 4.1. The simulation is done on three different memristors [7, 48, 51] and the elastic membrane memcapacitor [30] which are labeled in Table 4.1 as model 1, 2, 3, and 4 respectively. The models used in simulation are the Verilog-A models of the VTEAM model [22] for the three memristors and the Verilog-A model realizing the elastic membrane memcapacitor introduced in [49]. Each of the three memristor cases has a distinct OFF/ON impedance ratio (L) and is simulated in different memory densities (x) scenarios. Table 4.1 shows also the two possible R_t values according to eq. 3.15 in Chapter 3 (R_m is either R_{on} or R_{off}). Table 4.1 is also reporting two threshold values for each case: 1) Fixed threshold ($F.R_{th}$) according to eq. 3.20 in Chapter 3 that is chosen based on the value of OFF/ON impedance ratio (L) by picking the optimum value of the parameter p to maximize the x range where this threshold is a valid threshold and hence allow for the maximum memory density range of the memory array, 2) Variable threshold ($V.R_{th}$) based on the x value in eq. 4.16 which depends on the average cell value of the whole array as given by eq. 4.17 as well as the R_{on} and R_{off} values for each memory type. Table 4.1 shows that for large OFF/ON impedance ratios, the fixed threshold level can properly detect the memory cell value for very wide ranges of memory distribution (1s:0s). For smaller OFF/ON impedance ratios (L), the fixed threshold fails at narrower memory densities. For example in model 3, the limit is 25%-75% ratios between 1s and 0s or vice versa for proper R_m detection. The variable threshold reported in the last column shows that for all the given memory densities, there exist a threshold level that properly detects the memory cell value as well as increases the noise margins for the detection circuit. The only exception is in model 2 for the extreme case of all 1's case as the large

OFF/ON ratio of model 2 makes the array size not enough for the approximations made in eq.s 4.8 and 4.9 to be valid.

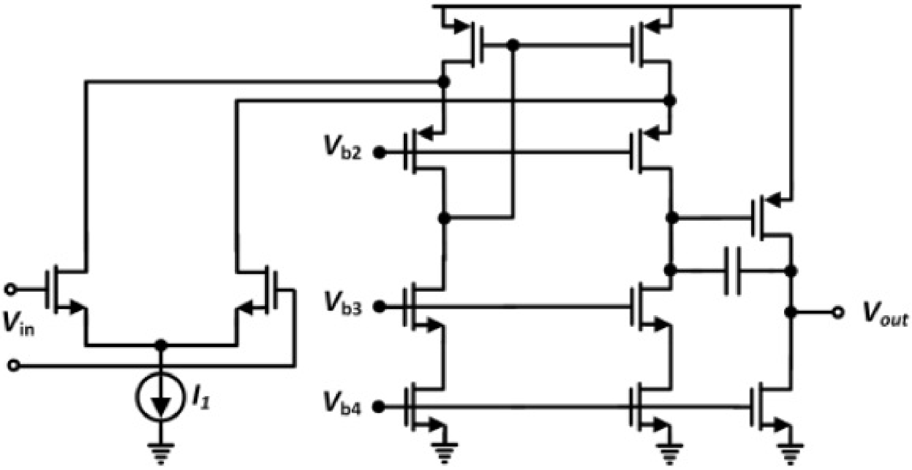
Table 4.1: Simulation results for the values of R_t after performing the multiport readout technique for different cell values and different 0/1 cell densities. The values of the fixed and adaptive thresholds are also shown where the failing thresholds are marked with '*'. The values of model 4 are normalized with respect to C_0 .

model	r	x(1s:0s)	$R_t(R_{on})(\Omega)$	$R_t(R_{off})(\Omega)$	$F.R_{th}(\Omega)$	$V.R_{th}(\Omega)$
1	25	50-50	1.8m	60m	12.5m	12.27m
1	25	85-15	12.3m	0.28	12.5m	101.4m
1	25	90-10	20m	0.45	12.5m*	179.15
1	25	10-90	0.5m	13.8m	12.5m	4.1m
1	25	5-95	0.5m	12m	12.5m*	3.7m
2	333	50-50	0.23	83.4	20.57	20.17
2	333	95-5	13.2	3.5k	20.57	1.7k
2	333	100-0	6.15k	322.2k	20.57*	543.6k*
2	333	10-90	70m	22.26	20.57	6.26
2	333	5-95	60m	19.83	20.57*	5.6
3	2	50-50	1.9m	3.7m	2.689m	2.64m
3	2	75-25	2.683m	5.2m	2.689m	3.76m
3	2	80-20	2.75m	5.34m	2.689m*	4m
3	2	25-75	1.4m	2.7m	2.689m	1.95m
3	2	20-80	1.38m	2.683m	2.689m *	1.85m
4	1.5	50-50	0.14m	0.09m	0.116m	0.115m
4	1.5	75-25	0.117m	0.077m	0.116m	0.095m
4	1.5	80-20	0.1m	0.08m	0.116m *	0.09m
4	1.5	25-75	0.17m	0.11m	0.116m	0.14m
4	1.5	20-80	0.17m	0.119m	0.116m*	0.148m

4.4.2 Reading circuit



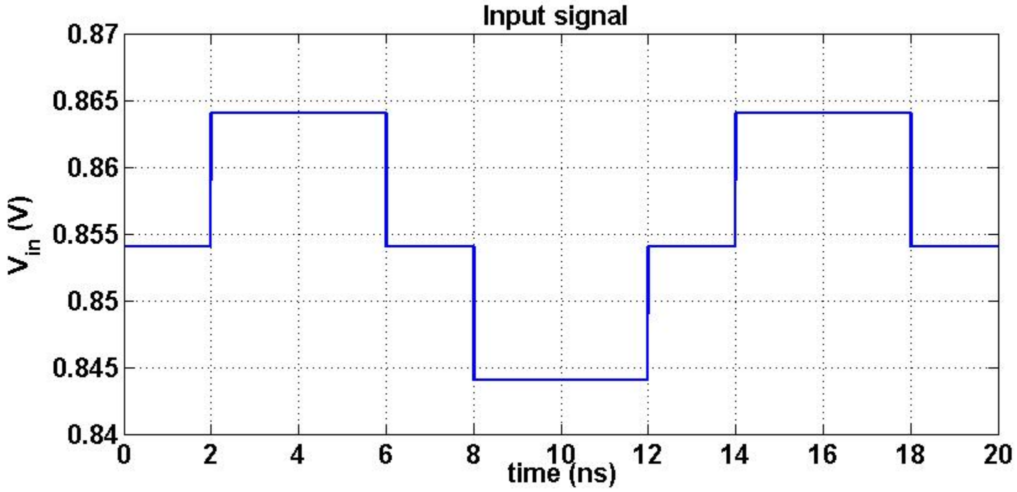
(a) The opamp in the inverting amplifier.



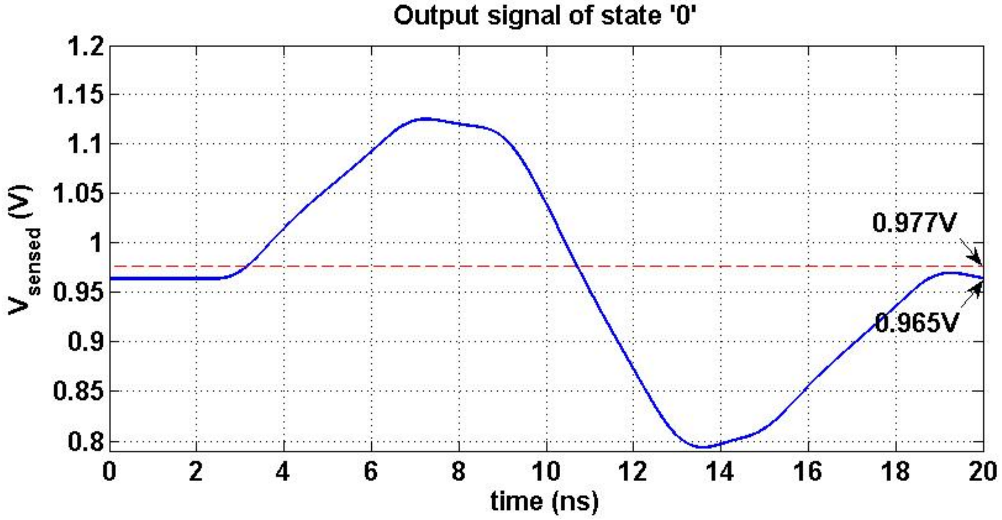
(b) The opamp in the integrator.

Figure 4.4: CMOS implementation of the two opamps in the circuit in Fig. 4.3.

To test the performance of the readout circuit shown in Fig. 4.3, we implemented a practical design using CMOS-based circuit which is shown in Fig. 4.4. The design of the first opamp of the inverting amplifier is shown in Fig. 4.4a. The opamp is a differential pair amplifier stage followed by a common drain amplifier stage that acts as a buffer to isolate the gain of the two opamps. It has DC loop gain of 46dB, gain bandwidth product of 580MHz, gain margin of 39dB and phase margin of 58^o. While the design of the opamp of the integrator is shown in Fig. 4.4b. The opamp is a differential pair amplifier stage followed by a common source amplifier stage to increase the output swing of the opamp. A capacitor was added between the outputs of the two stages for frequency compensation to make the opamp stable. It has DC loop gain of 69dB, gain bandwidth product of 550MHz, gain margin of 13.7dB and phase margin of 45^o. The design is simulated using Cadence Virtuoso Platform. The circuit is tested for an array of 1Kb (32×32) of ferroelectric memristors [7] also using the VTEAM Verilog-A model [22]. The results are shown in Fig. 4.5. As shown in the figure, there is a distinction between the output levels of the cases of 0 and 1. The read time is less than 20ns which is comparable to the sensing speed of the DRAM reported in [41].

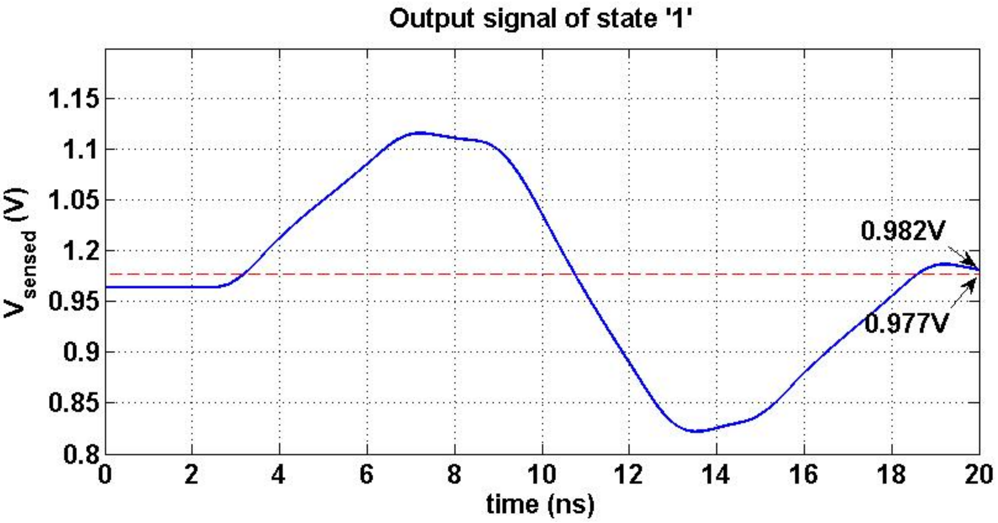


(a) Alternating square input signal of alphitude 10mV.



(b) When the sensed state is ’0’, the output signal is 965mV.

Figure 4.5: Results of CMOS implementation of the circuit in 0.3. The threshold is shown with both output signals in dashed red and has value of 977mV which is 13mV (calculated from eq. 3.20) above the DC value of the output signal.



(c) When the sensed state is '1', the output signal is 982mV.

Figure 4.5: Results of CMOS implementation of the circuit in 0.3. The threshold is shown with both output signals in dashed red and has value of 977mV which is 13mV (calculated from eq. 3.20) above the DC value of the output signal.

4.5 Conclusion

This chapter proposes a new approach to achieve the goals of ITRS [41]. We focused on a readout method used for restoring data from gate-less memristive crossbar memory array using three readings and performing arithmetic operation on them to detect the value of the stored information [44]. We analyzed the threshold defined for that method and showed how to choose this threshold. We analyzed the limitations for this threshold according to the 0/1 density of the array. Furthermore, we proposed a reading circuit to perform the three reading without need to store, restore, or perform arithmetic operations on the readings. We also proposed a new threshold level that guarantees correct cell value detection irrespective of the memory 0/1 density and that can be updated to guarantee proper memory operation while also improving the noise margins of the detection circuits. Finally, circuit simulations were performed to verify the analytical results for both fixed and variable threshold levels and test the performance of a practical design of the readout circuit. As noted from Fig. 4.5, the information extracted from the measured values is of much lower order of magnitude and hence, we will discuss this issue in the next chapter.

Chapter 5

Single-measurement method

In this chapter, a simple, fast and accurate single measurement readout method is proposed to read memory cells within non-gated crossbar memory arrays. The proposed technique overcomes the effect of sneak paths that causes inaccuracies in reading the stored value. It also relaxes the circuit requirements on the measuring circuits by increasing noise margins. Simulation results show that the proposed method yields large differences between the measured voltages representing values “1” and “0”as opposed to the previous three-measurements method.

5.1 Sensitivity of three-measurements method

The previous method introduced in [44] needs highly sensitive measurements. We will use the big-O notation through the analysis to define the order of magnitude of a variable in terms of N . If we assume a large array of size $N \times N$, the resistance R_r is composed of $N-1$ parallel memory cells. Hence its relative size to the resistance R_m is of $O(1/N)$. Similarly R_c is $O(1/N)$ while R_a , which has $(N-1)^2$ memory cells in parallel, is of $O(1/N^2)$. The resistance R_{12} is that of R_m ($O(1)$) in parallel with the series combination of R_r , R_a , and R_c (the series combination is $O(1/N)$). Thus R_{12} is $O(1/N)$ which means that the value of the current i_r shown in Fig. 5.1 is almost N times the value of i_m and the total current i_x is dominated by i_r . Consequently, the measurement of R_{12} is not sensitive to R_m . Similarly, R_{13} and R_{23} are $O(1/N)$. Given these relative sizes, the approximation made previously in eq. 3.11 in Chapter 3 can be deduced and R_t , which was defined in eq. 3.15, is $O(1/N^2)$. This means that the measuring circuits of R_{12} , R_{13} , and R_{23} ($O(1/N)$) must have sensitivity $O(1/N^2)$ to correctly calculate R_t . Table 5.1 list the orders of the variables as well as the measured values.

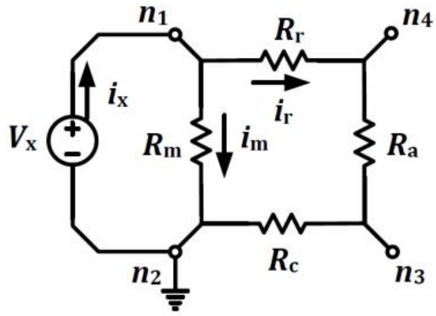


Figure 5.1: Circuit equivalent of the array shown in Fig. 3.4 in Chapter 3 when measuring R_{12}.

Table 5.1: The orders of variables and measurements.

Variable	$O(\,)$
R_m	1
R_r , R_c	$1/N$
R_a	$1/N^2$
R_{12} , R_{14} , R_{24}	$1/N$
$R_t = R_{13} + R_{23} - R_{12}$	$1/N^2$

5.2 Proposed Technique

In this section, we propose a solution that allows the detection of the selected cell's value using only one measurement. The proposed method depends upon preventing current from flowing through sneak paths. The method is as follows: A measuring circuit is applied between nodes n_1 and n_2 to measure R_{12} and a voltage buffer is connected between n_1 and n_4 as shown in Fig. 5.2. The buffer forces the potential difference between n_1 and n_4 to be zero which eliminates i_r and the buffer does not draw current from n_1 . This means the current flowing through n_1 has no path except through R_m and hence, the measuring circuit measures R_m directly by sensing the current flowing into n_1 ($R_{12} = R_m$). The measuring circuit parameters can be scaled to fit the order of the measured resistance. It has to be noted that the buffer can be connected between n_1 and either n_3 or n_4 as both will prevent the current to flow through sneak paths. Shorting n_3 and n_4 may also be more efficient for suppressing the effect of bar resistances. The circuit, shown at Fig. 5.2, senses R_m using a voltage divider by measuring the voltage difference between n_1 and n_2 (V_x) when the array is connected in series with a test resistance R_{test} . Therefore, the voltage difference between n_1 and n_2 (V_x) is given by eq. 5.1:

$$V_x = (V_{test}R_m)/(R_m + R_{test}) \quad (5.1)$$

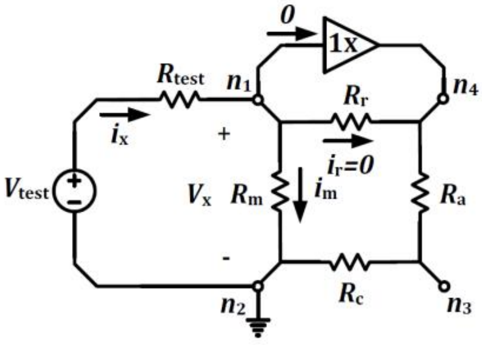


Figure 5.2: The proposed technique applied to the circuit equivalent of the crossbar memory array.

Where V_{test} is the applied test voltage. R_m has only two possible values and hence a threshold voltage can be defined to decide the value of R_m based on the value of V_x . It is clear from eq. 5.1 that with the proper choice of R_{test} , the correct value of R_m can be easily detected even for close values of R_{on} and R_{off} representing “0” and “1”.

The proposed solution has two main advantages over the one presented of [44]. First, this method is much simpler and faster. It uses a single measurement as opposed to three measurements then performing an arithmetic operation on those measurements. Second, the measured value in this proposal is itself the selected cell’s value. While in the technique of [44], the circuit must be sensitive to an order of $1/N$ less than the measured value. For example, in an array of size 512x512, if the measured voltage values corresponding to R_{12} , R_{13} , and R_{23} are in the order of 1V, the corresponding result for R_t will be in order of 2mV. This causes serious problems especially in the case of low R_{off}/R_{on} ratios where the two possible values of R_t are close to the threshold.

5.3 Simulation Results

To show the discussed advantages, a simulation comparing the two methods is done for different square array sizes using the VTEAM model [22] with the parameters designed to fit the Pt-Hf-Ti memristor [51] in which $R_{on} = 100\Omega$ and $R_{off} = 2.5k\Omega$. Table 5.2 gives the comparisons for arrays of sizes $N \times N$ for N =128, 256, and 512 with half the cells storing 1 and the other half storing 0. For the method proposed of [44], the measurements R_{12} , R_{13} , R_{23} and the result of the arithmetic operation on them R_t were recorded as well as a possible threshold value used for detection R_{th} . Table 5.2 shows also the measurement R_{12} using the proposed method which yields the exact values of R_m given that i_r was completely eliminated. As it is clear from the table, the measurements R_{12} , R_{13} , and R_{23} in case of the method of [44] are orders of magnitude larger than R_t but much smaller than R_m . On the other hand, for the proposed method there is only one measurement

Table 5.2: Results from the readout method in [44] and the proposed method.

N	Cell value	The readout method in [44]					Proposed method
		$R_{12}(\Omega)$	$R_{13}(\Omega)$	$R_{23}(\Omega)$	$R_t(\Omega)$	$R_{th}(\Omega)$	$R_{12}(\Omega)$
128	0	3.036	1.524	1.514	0.002	0.02	2.5k
128	1	2.95	1.502	1.492	0.044	0.02	100
256	0	1.4553	0.6735	0.7822	0.0004	0.005	2.5k
256	1	1.4352	0.6692	0.7764	0.0104	0.005	100
512	0	0.77	0.3911	0.379	0.0001	0.001	2.5k
512	1	0.7644	0.3896	0.3776	0.0028	0.001	100

that measures R_m directly. This shows the advantage of the proposed method in terms of accuracy as it does not require highly sensitive measuring circuit compared to the other technique. Table 5.2 shows that the problem becomes more acute when the array size increases. The small difference between the measured values makes the proposed method much better in terms of noise margin.

5.4 Conclusion

In this Chapter, we introduce a new method for reading the value of a cell in a non-gated crossbar memory array. This method is found to be more accurate compared to the previous three-measurements method as well as being simpler and faster. Simulations were carried on memristive arrays to prove the accuracy of the proposed method. However, although the previous discussed reading methods suppress sneak paths, they are vulnerable to the parasitic resistanceof the bars whose effect will be discussed in the next chapter.

Chapter 6

Discussion and Future work

Throughout the work, we dealt with the characteristics of memelements that makes them good candidates for use in many applications, of which we focused on gate-less memory array ones. We discussed some of the common problems in gate-less crossbar memory arrays such as: sneak paths, coupling capacitance, line resistance, and uneven distribution of binary information among cells and how these problems degrade the information extracted from the cells. We generalized an existing three-measurement that solves sneak paths problem to be used for memcapacitive cells beside memristive cells and enhanced it to overcome coupling capacitance. We showed afterwards how to optimize the threshold to account for uneven distribution of binary information among the array's cells.

In this chapter, we explore some possible approaches that can be used for enhancement of the readout process in gate-less crossbar memories in terms of line resistance effect for the future work. In Chapter 5, we introduced a new readout technique that uses single measurement to directly extract the data stored from the cell without need for other measurements or processing on the extracted information. However, this technique, as well as other techniques, suffers from the bars resistance effect that distorts the data extracted from a cell. The previous methods used shorting unselected rows as well as unselected columns to reduce the $2N$ nodes to only four nodes in an $N \times N$ array. However, bar resistances changes the crossbar memory array from the simple four-node equivalent circuit in Fig. 3.4 in Chapter 3 to a complicated distributed network of resistors of $2N^2$ nodes as shown in Fig. 6.1. This makes the mathematical analysis of the bar resistances effect on the reading process very difficult. However, it can be simulated using electronic simulators or by using a program to solve the mathematical formulation of the circuit including all variables as cell values, applied voltage scheme, and bar resistances as in the model introduced in [52]. This model applies Kirchhoff's law at the two nodes at the terminals of the N^2 memory cells giving $2N^2$ linear system of equations that forms $2N^2 \times 2N^2$ matrix system of large complexity $O(N^4)$. The system is solved for the cells' currents to get the current in the selected cell. A MATLAB code for solving this linear system of equations is shown in Appendix B. Also, the bar resistance degrades the voltage desired to be applied

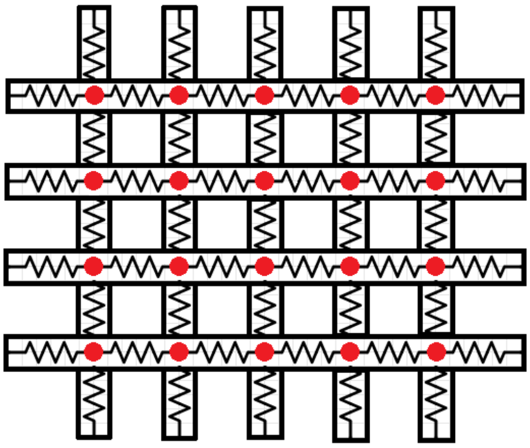


Figure 6.1: Top view of the equivalent circuit of the crossbar array showing line resistances where memory cells are the interconnections at the intersections of the upper bars and lower bars shown in red.

to the selected cell or the unselected cells due to the voltage drop on the bar resistances as shown in bitmap in Fig. 6.2. Although metallic bar resistance, which is often associated with memristive arrays, is less than that of semiconductor one, this problem becomes very serious for large arrays due to the increase in the length of the bars, and dense arrays due to the decrease in the cross-sectional area of the bars. Moreover, the effect of the bar resistances depends on the position of the selected cell. As the selected cell's position goes further from the external sides of the array i.e. further from the applied voltage source, the effect is increased as shown in Fig. 6.2.

6.1 Recent sneak-paths solving methods

It has to be noted that besides the discussed methods [43–45] and the method of Chapter 5, there are other recent methods that tend to estimate the sneak paths effect and cancel out its effect from the measurement [53–55]. All of these methods suffer from the line resistance problem as well. We will give a brief note about those methods before proposing a possible approach for solving the line resistance effect. As in Fig. 3.4 in Chapter 3 of the method of [44], the method of [53] shorts unselected rows to $n_3$and unselected columns to n_4. Also, $n_3$and n_4 are biased to the same voltage V_B which eliminates the effect of R_a. As shown in Fig. 6.3, the current measured from n_1 is the sum of the current in the selected cell and the current in R_r. The method depends on the fact that two cells on the same row have nearly the same R_r and the only difference is that they switch roles when selected: the selected cell R_m does not contribute to R_r while the unselected one contributes to it. The difference between the two contributions to R_r is insignificant in large arrays of high OFF/ON ratio and acceptable number of ON cells in the selected row. The method takes advantage of this similarity of the R_r parameter between cells of the

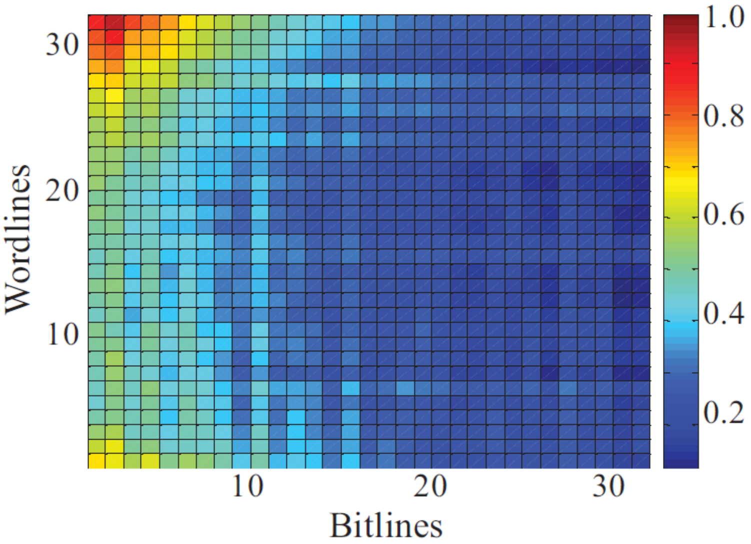


Figure 6.2: Bitmap from [52] of the voltage delivered to each cell according to its position normalized to the applied voltage.

same row to estimate the sneak paths effect to the cells of the certain row by deducing its effect from a dumb cell of known value in that row. The method is as follows: 1) Add a column of dumb cells of known values to the array. This means that each row contains a dumb cell of known value. 2) Read the current I_{sense0} entering the array while selecting the dumb cell of the selected row. This current is the sum of the current of the dumb cell and the sneak paths current $I_{sense0} = I_{m0} + I_r$. Since we know the dumb cell's value and consequently the value of I_{m0}, we can get the sneak paths current $I_r = I_{sense0} - I_{m0}$. 3) Read the current I_{sense} entering the array while selecting the intended cell. Since the sneak paths current of two cells is nearly the same and equals I_r, sneak paths current of the dumb cell can be subtracted from this measured current of the selected cell to get the current of intended cell $I_m = I_{sense} - I_r$. It has to be noted that although this method uses two measurements, the value of I_r calculated from the dummy cell can be used for all the cells of its row and due to locality of memories, blocks of data are stored sequentially which makes it likely that bits of the same row are decoded sequentially in practical uses. This means that statistically, the number of readings can be arbitrarily much less than two readings.

Concerning the method of [54], it relies on the fact that the distortion of the data is dominated by the number of ON cells. The measured value $\hat{S}$ is the sum of cell's current value S and the distortion D present in the form of sneak paths current $\hat{S} = S + D$. The maximum distortion D_{max} added to the value of the current in a cell in a selected row is when all the selected column cells are 1's. We can safely assume and verify by simulations that in case of high OFF/ON ratio, the distortion D added to the current in the selected cell is proportional to the number of 1's N_{on} in the selected column and hence $D = D_{max}N_{on}/N$. The method is as follows: 1) Add an all-ones row and an all-ones column to the array as

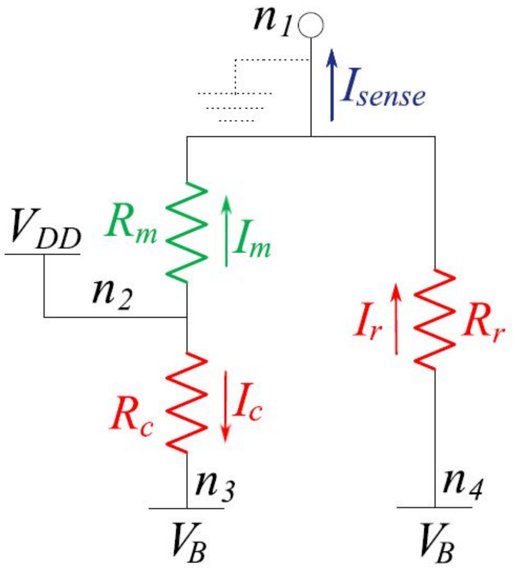


Figure 6.3: Circuit equivalent of the method of [53].

shown in Fig. 6.4. 2) Read the value of the cell in the selected row and all ones column. Since this cell is contained in an all-ones column, we can use it to estimate the maximum distortion D_{max} added to cell in the selected column. 3) Read the cell in the all-ones row and the selected column to get an estimate of the number of ones N_{on} in the selected column. We can also safely assume that this cell's value is a linear function of N_{on} which can be verified by simulations also. 4) Read the selected cell's value and use the values of D_{max} and N_{on} to get D and subtract it from the measured value to get the undistorted value of the cell $S = \hat{S} - D$. Although this method uses three measurements, the property of locality reduces the average number of measurements as in the case of [53].

Finally, the method of [55] introduces another port to estimate the sneak paths effect. This method is applied to memristors with diode characteristics i.e. memristors that suppress reverse currents due to high resistance R_{rev} in reverse bias and can have R_{on} or R_{off} values in forward bias. By treating every memristor as a diode too, we note as in Fig. 3.3 in Chapter 3 that every sneak path contains two forward biased cells (one cell from R_c and the other from R_r) mediated by a reverse biased cell (a cell from R_a). This means that memristors with diode characteristics suppress sneak paths but however, they do not completely remove them. Since the reverse biased cell has much higher resistance than the forward biased ones (whether they are ON or OFF), we can assume that most of the voltage drop on a sneak path is applied to the reverse biased cell in that sneak path. This means the resistance along the sneak paths is nearly $R_a = R_{rev}/(N-1)^2$. The method is as follows: 1) A row of dumb cells is added and the same voltage applied to the selected column V_{SS} is applied to it as shown in Fig. 6.5. 2) Apply V_R to the selected column to read the currents through the selected column I_{main} and through the row of dumb cells I_{comp}. I_{main} is the sum of the current in the cell I_{cell} and the sneak paths current. The

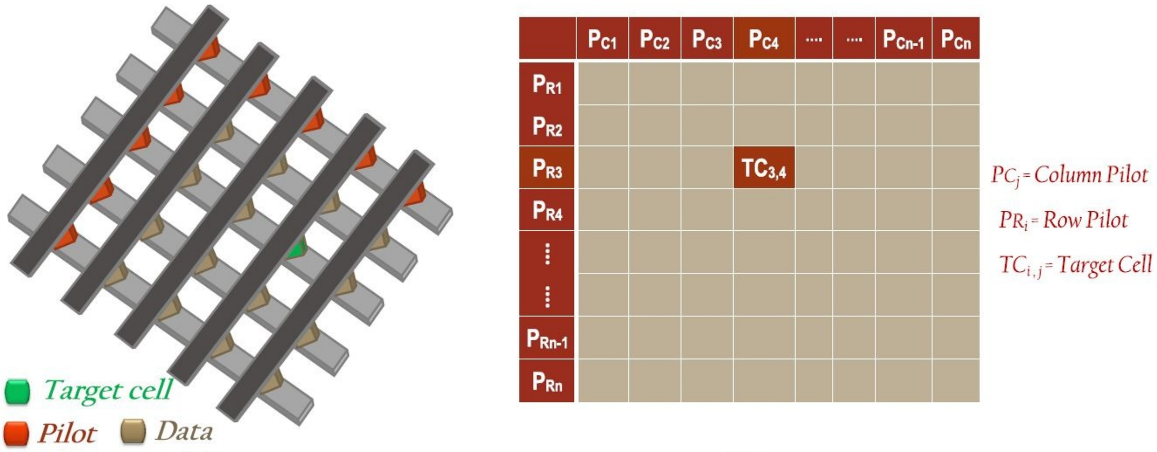


Figure 6.4: Illustration of the method of [54].

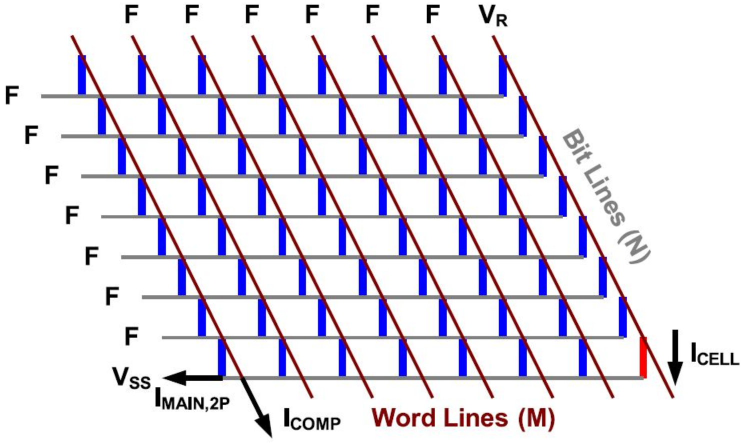


Figure 6.5: Illustration of the method of [55].

sneak paths current is $(V_R - V_{SS})/R_a$ as it is dominated by reverse biased cells as mentioned previously. SinceV_{SS} is applied to the row of dumb cells, the sneak paths do not pass through the cells of that row and hence, $R_a = R_{rev}/(N-1)(N-2)$. This gives eq. 6.1:

$$I_{main} \quad = \quad I_{cell} + (V_R - V_{SS})(N-1)(N-2)/R_{rev} \tag{6.1}$$

I_{comp} passes through cells of the selected row (cells are forward biased) to the cells of the row of dumb cells (dumb cells are reverse biased) and hence the voltage drop is dominated by the dumb cells. This gives eq. 6.2:

$$I_{comp} \quad = \quad (V_R - V_{SS})(N-1)/R_{rev} \tag{6.2}$$

From eq.s 6.1 and 6.2, we can get I_{cell} from eq. 6.3:

$$I_{cell} \quad = \quad I_{main} - (N-2)I_{comp} \tag{6.3}$$

6.2 Possible solution for bar resistance problem

To overcome the bar resistance problem, an array can be treated as a noisy communication channel to benefit from the use of communication techniques. The array can be considered a channel in which we are trying to transmit data through during the write process, or receive data from during the read process. Constant channel distortion is overcome by equalization i.e. inverting the effect of the channel. Although the bar resistances are constant for an array, their effect is too complicated for equalization as it varies from cell to cell according to its position from the source as mentioned and it is very inefficient to use different equalization for each cell position. Consequently, the array can be treated as a random channel where the randomness comes from the ignorance of the selected cell's position. To overcome the effect of the random channel, redundancy is added to the data such that the errors introduced by the randomness of the channel can be checked for. Each random channel has a capacity which means that the effect of the channel determine how much redundancy should be added to the data.

6.2.1 Time/Frequency diversity

Data redundancy can be added by channel coding. Channel coding, in its simplest form, converts k bits to n bits ($n > k$) such that the k bits can be retrieved from the n bits. This means the effect of the channel is averaged over the bits. The channel coding benefits from the randomness of the effect of the channel and so, if a bit is affected severely, its information can still be retrieved or checked for its correctness from other bits. This technique can be simulated in memory arrays by using different memory cell positions, over which the bar resistance effect varies, as different time slots in a fading channel. It has to be noted that the cells must be placed at distant positions in order for the bar resistance effect to vary between them. Otherwise, if the positions of the coded cells are near the applied voltage source, there would be no need for coding, and conversely, if they are placed far from the source, the coding might not help.

Besides diversity using time slots, diversity using frequency components can be used in frequency selective channels. Since the channel affects frequency components differently, data can be coded in the frequency domain, using Orthogonal Frequency Division Multiplexing (OFDM) for example, to average the channel effect over frequency components. Since frequency bins in a frequency selective channel would be analogous to different cell positions in a memory array like the time slots in a fading channel, this analogy is the same as its time counterpart. It has to be noted that Spread Spectrum techniques as Direct-Sequence Spread Spectrum (DSSS) that spreads data in frequency domain cannot be used to suppress noise as the cell positions are not actual physical frequency slots and the bar resistances effect is not an added noise effect on the memory cell.

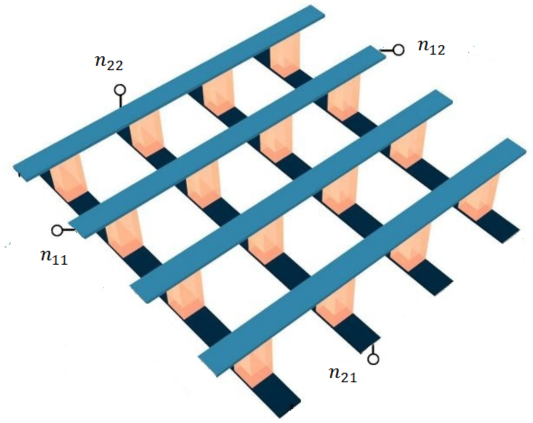


Figure 6.6: Taking several measurement of the same cell through different paths.

6.2.2 Space diversity

There is also space diversity which makes redundancy between the transmitter and the receiver by using multiple antennas at the transmitter, the receiver, or both to receive data through different channels as in Single-Input-Multi-Output (SIMO), Multi-Input-Single-Output (MISO), and Multi-Input-Multi-Output (MIMO) systems. This means the redundancy is through different versions of same data through different channels rather than in sent data itself. For the first glance, this can be realized in memory arrays by reading through different paths or even by using different reading techniques. Different paths can be created by reading the cell from either sides of the array. Hence, the cell is read by applying the voltage source between either sides of the upper bar and either sides of the lower bar which gives four possible channels as shown in Fig. 6.6 where the four measurement can be taken between the pairs: (n_{11},n_{21}) , (n_{11},n_{22}) , (n_{12},n_{21}) , and (n_{12},n_{22}) . However, this analogy needs more analysis to be formulated correctly as it seems the optimal combination of the different readings is to choose the one through the strongest path and this is deterministic for each cell position as the strongest path is the reading between the sides of the upper and lower bars nearest to the cell.

6.3 Conclusion

In this chapter, we discussed different novel reading techniques in literature that also overcome sneak paths effect. Then, we offered some insight to possible approaches to extract data from memory array suffering from parasitic bar resistances effect for future work. We used different analogies for the position-dependent bar resistance effect with some aspects of a communication channel. Analogies with time slots in fading channels, frequency bins in frequency selective channels and different paths in MIMO systems were discussed.

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Appendix A

Verilog-A Linear dopant drift memristor model

```
‘include “constants.vams”
‘include “disciplines.vams”
module memristor_model2 (p, n) ;
inout p, n;
electrical p, n;
parameter real uv = 10f;
parameter real d = 10n;
parameter real ron = 100;
parameter real roff = 38k;
parameter real rinit = 5k;
real k, r0, r1, r2, R ,assert ,i;
analog begin if(i == 0) r0 = rinit;
k = 2 * uv * ron * (roff - ron) / pow(d,2);
if((R==ron)&&(V(p,n)>=0)||((R==roff)&&(V(p,n)<0)))
begin
r0 = R;
assert = 1;
end
else if(assert!=0)
begin
r0 = R;
assert = 0;
end
r1 = pow(r0,2) - k * idt( V(p,n), 0 ,assert);
r2 = min( pow(roff,2) , max(r1,pow(ron,2) ) );
R = sqrt(r2);
V(p,n) <+ R * I(p,n) ;
i = 1;
```

```
end
endmodule
```

Appendix B

MATLAB code for memory array solution

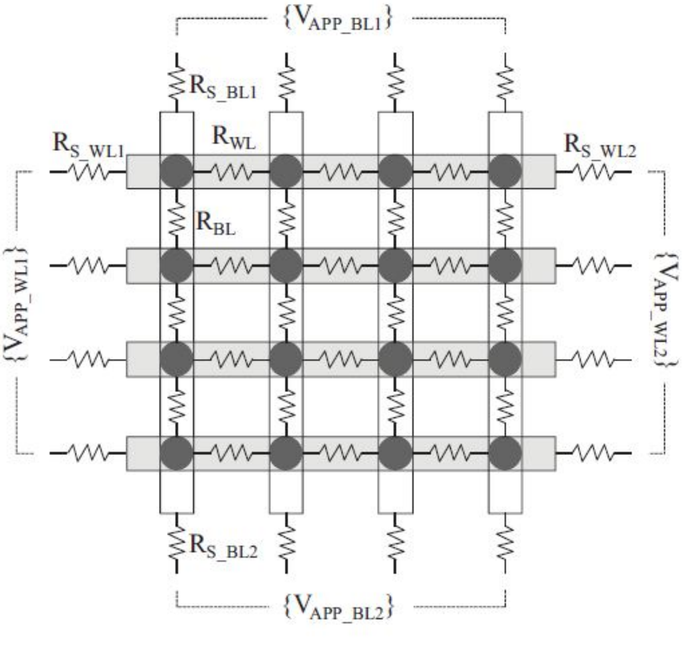

Figure B.1: The parameters used in the code taken from [52].

Using the notation in Fig. B.1, the following code is developed:

```
m=10;n=10; %array size
rsel=5;csel=5; %row and column of selected cell
Ron=100;Roff=2500; %LRS and HRS
Rwl=2;Rbl=2; %bar resistance
%input source resistances of word lines from both ends
Rswl1=ones(1,m);Rswl2=1e9*ones(1,m);
%input source resistances of bit lines from both ends
```

```
Rsbl1=ones(1,n);Rsbl2=1e9*ones(1,n);
%voltage sources applied to word lines from both ends
Vappwl1=ones(1,m);Vappwl2=ones(1,m);
%voltage sources applied to bit lines from both ends
Vappbl1=ones(1,n);Vappbl2=ones(1,n);
R=randi([0,1],m,n)*(Roff-Ron)+Ron; %cell values
Vappwl1(rsel)=1;Vappwl2(rsel)=1;
Vappbl1(csel)=0;Vappbl2(csel)=0;
Rswl1(rsel)=1;Rswl2(rsel)=1;
Rsbl1(csel)=1;Rsbl2(csel)=1;
A=[];
for i=1:m
    Ai=zeros(n);
    Ai(1,1)=1/Rswl1(i)+1/R(i,1)+1/Rwl;
    Ai(1,2)=-1/Rwl;
    Ai(n,n-1)=-1/Rwl;
    Ai(n,n)=1/Rswl2(i)+1/R(i,n)+1/Rwl;
    for j=2:n-1
        Ai(j,j-1)=-1/Rwl;
        Ai(j,j)=1/R(i,j)+2/Rwl;
        Ai(j,j+1)=-1/Rwl;
    end
    if mod(i,2)
        Atemp=blkdiag(A,Ai);
        clearvars A;
        else A=blkdiag(Atemp,Ai);
        clearvars Atemp;
    end
end
B=diag(reshape(-1./R',[1,m*n]));
C=[];
for j=1:n
    Cj=zeros(m,m*n);
    for i=1:m
        Cj(i,n*(i-1)+j)=1/R(i,j);
    end
    if mod(j,2)
        Ctemp=vertcat(C,Cj);
        clearvars C;
        else C=vertcat(Ctemp,Cj);
```

```
        clearvars Ctemp;
    end
end
D=[];
for j=1:n
    Dj=zeros(m,m*n);
    Dj(1,j)=-1/Rsbl1(j)-1/R(1,j)-1/Rbl;
    Dj(1,n+j)=1/Rbl;
    Dj(m,n*(m-2)+j)=1/Rbl;
    Dj(m,n*(m-1)+j)=-1/Rsbl2(j)-1/R(m,j)-1/Rbl;
    for i=2:m-1
        Dj(i,n*(i-2)+j)=1/Rbl;
        Dj(i,n*(i-1)+j)=-1/R(i,j)-2/Rbl;
        Dj(i,n*i+j)=1/Rbl;
    end
    if mod(j,2)
        Dtemp=vertcat(D,Dj);
        clearvars D;
        else D=vertcat(Dtemp,Dj);
        clearvars Dtemp;
    end
end
E=[];
for i=1:m
    Ewi=zeros(n,1);
    Ewi(1)=Vappwl1(i)/Rswl1(i);
    Ewi(n)=Vappwl2(i)/Rswl2(i);
    E=[E;Ewi];
end
for j=1:n
    Ebj=zeros(m,1);
    Ebj(1)=-Vappbl1(j)/Rsbl1(j);
    Ebj(m)=-Vappbl2(j)/Rsbl2(j);
    E=[E;Ebj];
end
V=[A B;C D]\E;
Vwl=reshape(V(1:m*n),[m n])’; %cells’ upper nodes voltages
Vbl=reshape(V(m*n+1:2*m*n),[m n])’; %cells’ lower nodes voltages
```

```
%voltages across word lines
Vwl1=horzcat(Vappwl1’,Vwl(:,1:m),Vappwl2’);
%voltages across bit lines
Vbl1=vertcat(Vappbl1,Vbl(1:n,:),Vappbl2);
Rawl=horzcat(Rswl1’,Rwl*ones(m,n-1),Rswl2’);
Rabl=vertcat(Rsbl1,Rbl*ones(m-1,n),Rsbl2);
Vx=Vwl-Vbl;Ix=Vx./R; %voltages and currents of cells
%currents through word lines
Iwl=(Vwl1(:,1:m+1)-Vwl1(:,2:m+2))./Rawl;
%currents through bit lines
Ibl=(Vbl1(1:n+1,:)-Vbl1(2:n+2,:))./Rabl;
Iin=Iwl(rsel,1); %current entering selected word line
Iout=Ibl(end,csel); %current exiting selected bit line
Isel=Ix(rsel,csel); %current through selected cell
%checking Kirchhoff’s law at each node:
check1=zeros(m,n);check2=zeros(m,n);
for i=1:m

    for j=1:n
        check1(i,j)=Iwl(i,j+1)+Ix(i,j)-Iwl(i,j);
        check2(i,j)=Ibl(i,j)+Ix(i,j)-Ibl(i+1,j);
    end

end
%check values must be zeroes after the nested loop
k1=find(check1);k2=find(check2);
```

مما يعطيه مميزات عن الطريقة السابقة من ناحية السرعة وحد الضوضاء. وفي النهاية، تم طرح بعض الاقتراحات النظرية للعمل عليها مستقبلاً للتغلب على تأثير مقاومة القضبان على البيانات المستخرجة من المصفوفة عن طريق تمثيل المصفوفة كقناة اتصال واستخدام طرق الاتصالات للتغلب على تحريف المعلومات المرسلة عبرها.

وقد تم تنظيم هذا العمل كالتالي: الباب الأول يناقش تعريف الممريستور وخصائصه والنماذج الرياضية ونماذج الدوائر الخاصة به وبعض مكونات الدوائر التي تحتوي على خصائصه وأيضاً بعض التطبيقات المستخدم فيها. وبالمثل، فإن الباب الثاني يناقش الفئة الممتدة للمكثف والحاث ذوي الذاكرة وخصائصهم وبعض المواد التي تحتوي على خصائصهم وأيضاً المزيد من التعميمات والامتدادات لمكونات الدوائر. بعد ذلك يبحث الباب الثالث في استخدام المكثف ذو الذاكرة كخلية ذاكرة، ويناقش مصفوفات الذاكرة الخالية من بوابات الاختيار ومشكلتها في المسارات المتسللة مع التركيز على طريقة الثلاثة قياسات المميزة. وذد طبقت هذه الطريقة لمصفوفات مكونة من مكثفات ذوي ذاكرة لإخماد الاقتران السعوي ومقاومة القضبان. ثم يناقش الباب الرابع كيفية اختيار الحد الفاصل الأمثل وكيفية جعله يتكيف على توزيع قيم المعلومات في المصفوفة. والباب الخامس يقترح طريقة تستخدم قياس واحد لاستخراج البيانات. وأخيراً، يختم الباب السادس الأبواب السابقة ويقدم رؤية لحل تأثير مقاومة القضبان باستخدام طرق الاتصالات للتغلب على تأثير القنوات.

ملخص الرسالة

في هذه الرسالة، يتم فحص خصائص إحدى مكونات الدوائر الالكترونية الحديثة نسبياً وهي الممريستور، والذي يعمل كمقاومة الكترونية ذات ذاكرة والتي تعتبر رابع عنصر أساسي من مكونات الدوائر التي تضم المقاومات والمكثفات والمحثات. الممريستور لديه خاصية تبديل المقاومة ويستطيع الحفاظ على حالته بعد زوال المؤثرات الكهربية عليه. هذه الخصائص تجعلها مرشحة جيدة للاستخدام كخلية ذاكرة في تطبيقات الذاكرة، والدوائر المنطقية، والمذبذبات الاكترونية الخالية من المفاعلة الكهربية، والشبكات العصبية، وغيرها الكثير من التطبيقات المفيدة. يتم أيضاً فحص الفئة الموسعة التي تضم المكثف ذو الذاكرة والحاث ذو الذاكرة واللذان يشبهان نظيريهما المكثف والحاث العاديين مع تأثير الذاكرة. وهم أيضاً جزء من فئة أكبر تحوي على مكونات ذوات رتب أعلى وأيضاً الفئة الأكبر التي تحوى على المكونات الكسرية. يتم دراسة كيفية استخدام هذه المكونات كخلايا ذاكرة في مصفوفات الذاكرة ذات القضبان المتقاطعة التي لا تحتوي على بوابات لاختيار الخلية، وكيفية تحقيق اهداف خارطة الطريق الدولية لتكنولوجيا أشباه الموصلات أو الITRS. وتهدف تلك الخارطة إلى تحقيق مصفوفات ذاكرة ذات سرعة وكثافة عاليتين مع استهلاك قليل للطاقة. وقد تم إجراء العديد من الأبحاث على المكونات الالكترونية المستجدة ليتم استخدامها كبديل لتكنولوجيا شبه موصل–أكسيد الفلز المتكامل أو الCMOS والتي يتوقع قصور إمكانية تصغيرخا مستقبلاً ونهاية قانون مور الشهير. المصفوفات الخالية من البوابات تستغني عن المكونات التي تسخدم لاختيار الخلية المراد استخراج المعلومة منها لتوفير مساحتها واستغلالها لجعل المصفوفة أكثر كثافة. وقد تم التركيز على مشكلة المسارات المتسللة في المصفوفات التي تخلو من بوابات اختيار الخلية وكيفية التغلب عليها. والمسارات المتسللة هي مسارات غير مرغوب فيها عبر الخلايا غير المختارة لغياب تيارات الاختيار ولكن يتم التخلص منها عبر طرق صعبة. وقد تم تحليل إحدى الطرق المميزة التخلص من المسارات المتسللة في مصفوفات الذاكرة التي تعتمد على الممريستور والتي لا تحتوي على بوابات عن طريق أخذ ثلاثة قياسات وإجراء بعض العمليات الحسابية عليها لاستخراج المعلومة إلغاء تأثير التيارات المتسللة رياضياً، وبيان ان الطريقة صالحة للاستخدام مع كل مكونات الذوائر ذوات الذاكرة، وانها قد تعدل لإخماد تأثير السعة الناتجة عن اقتران القضبان المستخدمة لاختيار الخلية. كما تم تحليل الحد الفاصل المستخدم للكشف عن المعلومة الثنائية القيمة، وكيفية الحصول على أفضل حد فاصل لتحمل أقصي انحراف عن التوزيع المتساوي للقيم الثنائية للمعلومات في المصفوفة، وكيفية جعل الحد الفاصل يتكيف على توزيع قيم المعلومات في المصفوفة. وقد تم أخيراً عرض طريقة تستخدم قياس واحد بدون إجراء عمليات حسابية ويستطيع أيضاً إخماد تأثير التيارات المتسللة

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عنوان الرسالة:

بحث في مصفوفات الذاكرة غير المحتوية على بوابات اختيار
والمعتمدة على المقاومة والمكثف ذوي الذاكرة

الكلمات الدالة:

ممريستور، مكثف ذو ذاكرة، مصفوفات الذاكرة بدون بوابات اختيار الخلايا، المسارات المتسللة

ملخص الرسالة:

تهدف هذه الرسالة إلى استكشاف خصائص مكونات الدوائر المستجدة مثل الممريستور (المقاومة ذات الذاكرة) والمكثف ذو الذاكرة.ويتم دراسة استخدام هذه المكونات كخلايا ذاكرة في تطبيقات الذاكرة والطرق المستخدمة لاستخراج المعلومات منها. ويساعد هذا البحث على إعطاء حلول أفضل للتغلب على عدة مشاكل مثل المسارات المتسللة في المصفوفات التي لا تحتوي على بوابات لاختيار الخلية، والسعة الناتجة عن اقتران القضبان المستخدمة في اختيار الخلية، وعدم تماثل توزيع المعلومات بين خلايا الذاكرة. كما يعطي هذا العمل توجيهاً لحل مشكلة تأثير مقاومة القضبان على المعلومات المستخرجة للعمل عليها مستقبلاً.

بحث في مصفوفات الذاكرة غير المحتوية على بوابات اختيار والمعتمدة على المقاومة والمكثف ذوي الذاكرة

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بحث في مصفوفات الذاكرة غير المحتوية على بوابات اختيار والمعتمدة على المقاومة والمكثف ذوي الذاكرة

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بحث في مصفوفات الذاكرة غير المحتوية على بوابات اختيار والمعتمدة على المقاومة والمكثف ذوي الذاكرة

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