# Novel Memristor-based Wireless Communications Blocks

By

**Nahla Elazab Abd El-Lateif**

A Thesis Submitted to the

Faculty of Engineering at Cairo University

In Partial Fulfillment of the Requirements for the Degree of

**DOCTOR OF PHILOSOPHY**

In

## Electronics and communication Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
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Title of Thesis: **Novel Memristor-based Wireless Communications Blocks**

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Summary:

The distinction of memristor device as being non-volatile, having nanoscale dimension, and CMOS compatible makes it a real alternative to CMOS device. In this context, the main objective of this thesis is to study the dependence of the memristor resistance on initial phase of the applied periodic signal. Based on that, a set of building blocks for communication applications are designed, i.e. BPSK, QPSK, QAM, and BFSK demodulators. Next, memristor based sinusoidal phase frequency detector, voltage controlled oscillator, and phase locked loop are presented.

# Disclaimer

I hereby declare that this thesis is my own original work and that no part of it has been submitted for a degree qualification at any other university or institute.

I further declare that I have appropriately acknowledged all sources used and have cited them in the references section.

Name: Date:

Signature:

# Dedication

This dissertation is lovingly dedicated to the spirit of my father, **Elazab Elashkar**, who had always dreamed of completing my academic studies and to my mother, **Aida Mohamed Othman** for her praying to progress in my life.

# ACKNOWLEDGEMENTS

First of all, I thank Almighty God for His blessings and generosity. Second, I am glad to express my deep sense of gratitude to ***Dr. Ahmed Hussein*** for his co-operation in completing this research work. Also, I am greatly thankful to ***Dr. Hossam Fahmy*** for his intuitive thinking and giving me the honour to pursue my PhD studies under his supervision.

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# LIST OF ACRONYMS

AD: Analog to Digital
ALD: Atomic Layer Deposition
AM: Amplitude Modulation
ASK: Amplitude Shift Keying
BFSK: Binary Frequency Shift Keying
BPSK: Binary Phase Shift Keying
CMOS: complementary metal-oxide-semiconductor
CO: Condition of Oscillation
DA: Digital to Analog
DC: Direct current
ESD: Electro Static Discharge
FM: Frequency Modulation
FO: Frequency of Oscillation
FSK: Frequency Shift Keying
HP: Hewlett–Packard
LANs: wireless Local Area Networks
LPF: low pass filter
MIM: Metal-Insulator-Metal
NIL: Nano-Imprint Lithography
Op Amp: Operational Amplifier
OTA: Operational Transconductance Amplifier
PLL: Phase Locked Loop
PM: Phase Modulation
QAM: Quadrature Amplitude Modulation
QPSK: Quadrature Phase Shift Keying
RCG: Resistance Controlled Gain
RFID: Radio-Frequency Identification
TEAM: ThrEshold Adaptive Memristor Model
UWB: Ultra Wide Band
VCO: Voltage Controlled Oscillator
VTEAM: Voltage ThrEshold Adaptive Memristor Model

# ABSTRACT

The continued scaling down for physical feature size of Complementary Metal Oxide Semiconductor (CMOS) transistors is expected to reach its boundary. Material, technological, economical, and power-thermal challenges limit further CMOS scaling.

The distinction of memristor device as being non-volatile, low power consumers, having nanoscale dimension, and CMOS compatible makes it a real complementary or alternative to CMOS device. Further, the emerging of more memristor based designs for the traditional essential or new structured circuits enhances the chance of memristor technology to replace CMOS technology.

Generally, a lot of memristor based applications that include nonvolatile memory realizations, neuromorphic systems, adaptive amplifiers, filters have been proposed in the last ten years. In these applications, the adaptation of memristor resistance according to the applied signal amplitude or its frequency has been exploited. However, till now, little efforts were devoted to synthesis of the nonlinear memristive circuits in communication systems.

Moreover, in most of aforementioned analog applications, the linear dopant drift model has been adopted. Although, this model satisfies the basic memristive system equations, it deviates significantly from the behavior of the reported fabricated memristive devices. Additionally, this model is applicable at very low frequency so most proposed designs that adopted this model were verified at low frequency (1–100Hz) which reduces the probability of utilizing them in practical applications.

In this context, the main objective of this thesis is to study the dependence of the memristor resistance on initial phase of the applied periodic signal. Based on that, a set of building blocks for communication applications are designed.

In the beginning, digital communication memristor based demodulators are proposed and investigated. The proposed demodulators are for Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK), 8-Quadrature Amplitude Shift Modulation (QAM), and Binary Frequency Shift Keying (BFSK) modulation schemes. Since all proposed demodulators are asynchronous, the proposed circuits do not need any carrier recovery circuits.

Next, memristor based sinusoidal phase frequency detector is presented for the first time ever as well as the memristor based demodulators. The proposed detector is able to generate a DC signal that represents the difference in phase or frequency between the two sinusoidal inputs. Therefore, it eliminates the need for Low Pass Filter (LPF) block in the conventional Phase Locked Loop (PLL) structure which reduces the area and dissipated power of the overall PLL system.

After that, a novel memristor based Voltage Controlled Oscillator (VCO) using a single dual current output OTA (Operational Transconductance Amplifier) is

proposed. The proposed circuit includes a single dual current output OTA and only three passive components (one memristor and two capacitors). The two used capacitors in this oscillator circuit are grounded hence it is preferred for integration. Resistance Controlled Gain (RCG) property of the OTA is used for achieving memristance independent oscillation condition. Whilst this requirement did not consider in any of the literature pre-presented memristor based Wien bridge sinusoidal oscillators.

Finally, the memristor based phase frequency detector is integrated with the memristor based VCO to form a novel structure memristor based switching mode PLL system with suggestion of some important biomedical applications that operate in same frequency range.

It is worthy to mention that, the experimental-based 'nonlinear' dopant drift model is used along with the proposed circuits providing incorporation of all known non-idealities of practically realized memristor and gaining high operation frequency.

The remainder of this thesis is organized along the following chapters: first, Chapter one provides an overview of the memristor as a nano-device. This overview involves memristor history, physical implementations, the description models, and applications. Second, Chapter two studies the effect of amplitude, frequency, and phase change of a sinusoidal, triangle, and square signal on a memristor in terms of its memristance dynamics and its I–V characteristics using the linear and nonlinear dopant drift models. Thirdly, Chapter three presents the proposed memristor based demodulators for some digital modulation schemes. Fourthly, the proposed memristor based phase frequency detector at 25Mhz is introduced in Chapter four with verifying of its validation using analytical analysis and circuit simulation. Fifthly, a memristor based VCO and a switching mode PLL system are suggested in Chapter five. Finally, the thesis conclusion and the arising future work are discussed in Chapter six.

# Chapter One

# AN OVERVIEW OF THE FOURTH PRIMARY CIRCUIT ELEMENT 'THE MEMRISTOR AS A NANO-DEVICE'

The nano-device memristor is considered the fourth basic circuit element besides the resistor, the capacitor and the inductor. It acts as a variable resistor, whose resistance at any time is a function of the charge, which has traveled through the device (charge controlled memristor) or the flux that has impinged on the device (flux controlled memristor). Another attractive property is that the memristor is non-volatile device where once the memristor is disconnected from the minimum potential difference required for programming, the value of the resistance before the disconnection will be retained. As a simplified picture, a memristor can be thought as special type of pipe that shrinks or expands when water flows throughout it. If water pressure is stopped, pipe will keep its most recent diameter, until water is turned back on. Accordingly, this passive element has a nonlinear performance, and a feature of remembrance of last applied state. These distinctive properties make it significant circuit element for several applications.

## *1.1 Memristor history*

The word 'memristor', as a contraction of memory resistor, emerged for the first time by Prof. Chua in [1]. It was a result of his established mathematical foundations for nonlinear network theory [2]. In these studies, Chua generalized the mathematical relations between the basic electrical circuit quantities, charge, current, flux, and voltage, to be nonlinear relations. He demonstrated that the absolutely linear circuits are very restrictive, because real physical systems will show nonlinearity outside some operating range. Moreover, he observed the existence of a possible differential relationship between the charge passing through the circuit and the electrical flux in the circuit. This relationship should lead to the definition of new two terminals passive circuit element. Similarly, the other differential relationships between the four fundamental electrical circuit quantities are the definitions of the three well known fundamental circuit elements, the resistor, the capacitor, and the inductor. The properties of this new element were mathematically explored by Chua founding that it is a resistor with memory. In other words, the device resistance changes depending on the amount of charge flowing through it. Therefore, Chua called this device a memristor. The mathematical representation of the memristor was interpreted as in (1-1) [3].

$$\boldsymbol{R_m(W) = \frac{d\Phi}{dq} = \frac{v(t)}{i(t)}} \tag{1-1}$$

He clarified that the memristor current-voltage (I/V) characteristic should have the pinched hysteresis form rather than linear relationship as the normal resistor. This

deduction of the properties of a new circuit element from symmetry arguments, and not using any experimental observations, was totally revolutionary and unique [4].

Although the memristor definition is not constrained by certain functional form of the flux-charge relationship, it was not clear at that time whether the physical implementation of this element exist or not. Therefore, Chua named it "the missing element". However, earlier experimental results have shown memristive properties, such as the resistive switching properties of titanium dioxide that were originally described in 1968 [5] and ferroelectric based memory which was proposed in 1963 [6]. In 2008, four decades after Chua postulations, the Hewlett–Packard (HP) researchers published a seminal paper in "Nature" announcing the practical implementation of a new circuit device. This device completes the missing link between charge and electric flux. They also developed its first behavioral model [3]. From that time, the research community offered a huge pool of anticipated applications of the memristor, presenting the describing models, and investigating active emulating circuits. Thereby, more detailed discussions about the recent memristor implementations, models, and applications will be reported in the following subsections.

## *1.2 Memristor schematic symbol*

The memristor schematic symbol is shown in Fig. 1-1. It is obvious that, the memristor is a polarized device, polarity sensitive, and its positive lead distinguished from its negative one by solid line. Accordingly, the memristor voltage in general means the difference between the positive and negative leads voltages.


**Fig. 1-1 The memristor schematic symbol.**

## *1.3 Memristor physical implementations*

As the hysteresis is an indicator of the memristive properties in any material, there are enormous efforts to demonstrate the memristor behavior experimentally by characterizing several materials.

### *1.3. 1 Titanium dioxide memristor*

The titanium dioxide resistive switchin g characteristics were initially described in 1968 [5]. Then, several papers and patents were published in this issue [3], [7]–[9]. A TiO2 memristor is in general, prepared from a metal-insulator-metal (MIM) sandwich

with the insulator typically consisting of a thin film of $TiO_2$ as shown in Fig. 1-2. One of the explanations the memristive effect remained concealed for so long is the fact that memristive effect vanishes quickly when the thin film thickness is raised beyond the nanometer scale [3]. Presently, there are only some known techniques of fabricating the memristor. The most extensively used methods are atomic layer deposition (ALD) and nano-imprint lithography (NIL). Both methods need costly equipment and various fabrication steps as well as a high temperature annealing step and a "forming" step [10]. The HP memristor was fabricated using annealed $TiO_2$ [3]. Annealing is a mean of baking a material, mostly for the purpose of restructuring an amorphous material into a crystal. In this case, annealing is used to generate oxygen vacancies. The annealing heat gives enough energy to the oxygen for escaping the $TiO_2$ bonds. The annealing is accomplished in an atmosphere of hydrogen therefore any escaped oxygen will unite with hydrogen to form water vapor [10]. Oxygen vacancies are essential to the operation of the memristor as will be described later in HP memristor model subsection [11]. Hitherto, HP $TiO_2$ memristor is one of the most famous implementations of the $TiO_2$ memristor [3].

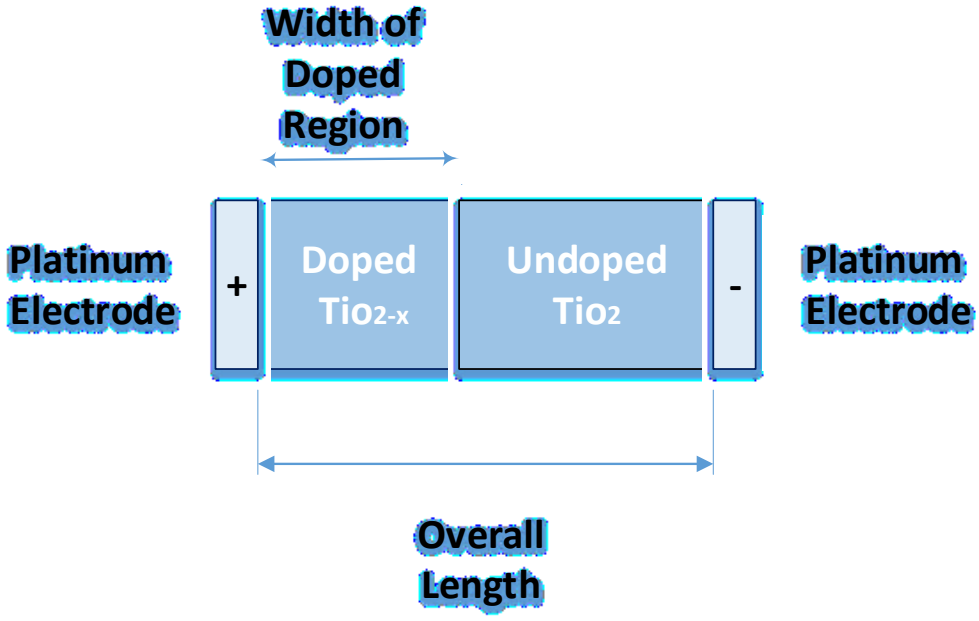



**Fig. 1-2 Structure of Titanium dioxide memristor.**

### *1.3.2 Graphene Oxide memristors Ionic (Polymeric) memristor*

Flexible memristors were made by Choi and his team using films of thin graphene oxide [12]. They adopted a device structure similar to the titanium dioxide device, exchanging titanium dioxide by graphene oxide as shown in Fig. 1-3. They deposited wires of 50-micrometer-wide aluminum on a 6.5 $cm^2$ plastic piece. Next, a solution including suspended graphene oxide chips was span onto the surface. As a result, a thin film of overlapping flakes of graphene oxide was formed. Then, the top aluminum wire array was deposited over this thin film. This led to 25 memristor devices, each of 50 µm width.

Additionally, Williams team in Hewlett-Packard company introduced a patent, in 2012, in which the fabrication of the graphene based memristor was demonstrated [13]. This memristor includes two electrodes. Whereas, a defective graphene layer is adjacent to the first electrode, and a memristive material that contains a number of ions is adjacent to the defective graphene layer. While, a second electrode is neighboring the memristive material. Normally, a voltage source that generates an electric field is applied between the two electrodes. Under the influence of this electric field, ions in the memristive material construct an ion conducting channel between the defective graphene layer and the second electrode [11].

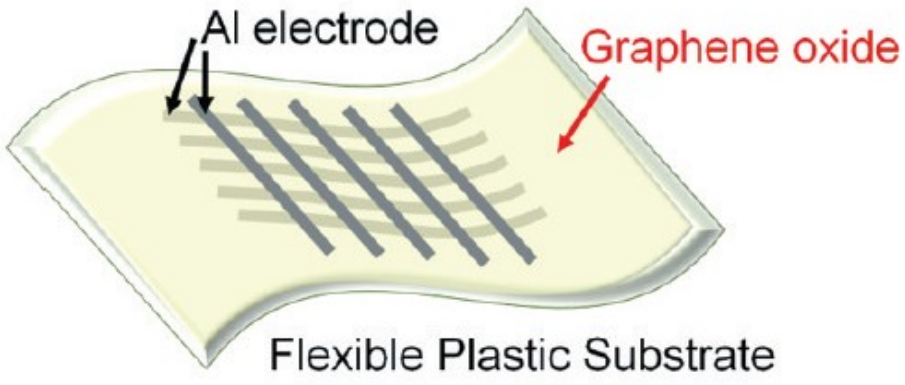



**Fig. 1-3 Structure of a G-O based flexible memristor device (adopted from [12]).**

### *1.3.3 Silicon Oxide memristors*

The silicon oxide memristive substrates have been developed in 2010 by Mehonic and other researchers [14]. The silicon oxide memristor shows high compatibility with current micro-fabrication infrastructure. In this silicon based memristor device, the active layer is silicon-rich silica as illustrated in Fig 1-4.

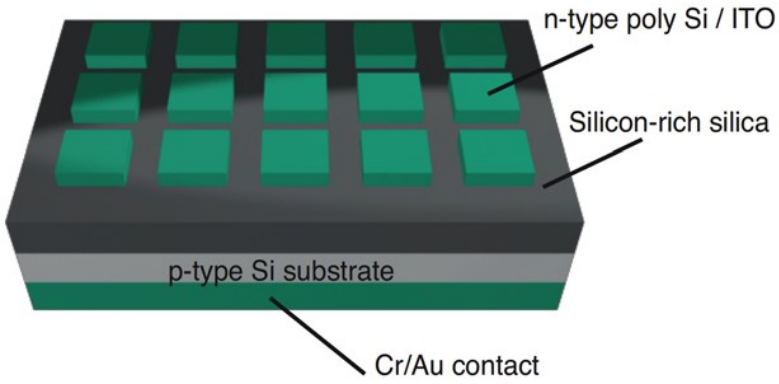



**Fig. 1-4 Structure of Silicon Oxide memristor device (adopted from [14]).**

The resistive switching property is an inherent phenomenon of the silicon-rich oxide layer and it does not rely on the metallic ions diffusion for forming conductive paths. Therefore, switching of the silicon oxide memristor has the pinched hysteresis I/V

loop characteristic of other memristive systems, and off/on resistance ratios of higher than 104:1 can be easily obtained. Experimental results demonstrate transition times in nanosecond scale and programming currents as low as 2μA. The diameter of switchable conductive pathways was revealed to be 10 nm or smaller using the scanning tunneling microscopy [14],[11].

### *1.3.4 Ferroelectric memristor*

The main idea of this device is to achieve the function of memory in ferroelectric material, and to exploit the permanent polarization of the ferroelectric material to control the semiconductor field-effect conductance. This concept was firstly proposed in 1963 [6]. Another structure of ferroelectric memristor was proposed in 2012 [15]. It consists of a thin barrier of ferroelectric material sandwiched between two metallic electrodes. The polarization of the ferroelectric material is switched by applying a negative or positive voltage across the junction. Hence, the resistance varies between two values called $R_{off}$ and $R_{on}$ which is lower by two orders of magnitudes. This effect is termed as *tunnel electro- resistance*. It is worthy to mention that the polarization does not switch suddenly, the exchange occurs gradually by the development of ferroelectric domains having opposite polarization. Throughout this process, the resistance is between $R_{off}$ and $R_{on}$.

The uniqueness of the ferroelectric memristor is that the memristor response can be engineered well since the dynamics of the ferroelectric domain can be tuned purely electronically. Thereby, the device reliability is enhanced where no serious change is encountered in the material structure [10], [11].

### *1.3.5 Resonant-tunneling diode memristors*

Certain types of quantum well diodes show memristive characteristics. They have spacer layers with special doping profiles between the drain and source regions. More details can be found in [16], [17].

### *1.3.6 Ionic (Polymeric) memristor*

Some implementations of ionic memristor have been announced even before the HP memristor. For example, Krieger et al. suggested a structure of a passive layer between active and electrode thin films, shown in Fig. 1-5, the structure enhanced the pulling out of ions from the electrode to make nonvolatile memory functioning cells [18].

In addition, Fontana and Erokhin investigated a polymeric memristor [19]. Then Berzina et al. presented results on the enhanced performance of electro-chemically controlled ionic memristors [20].

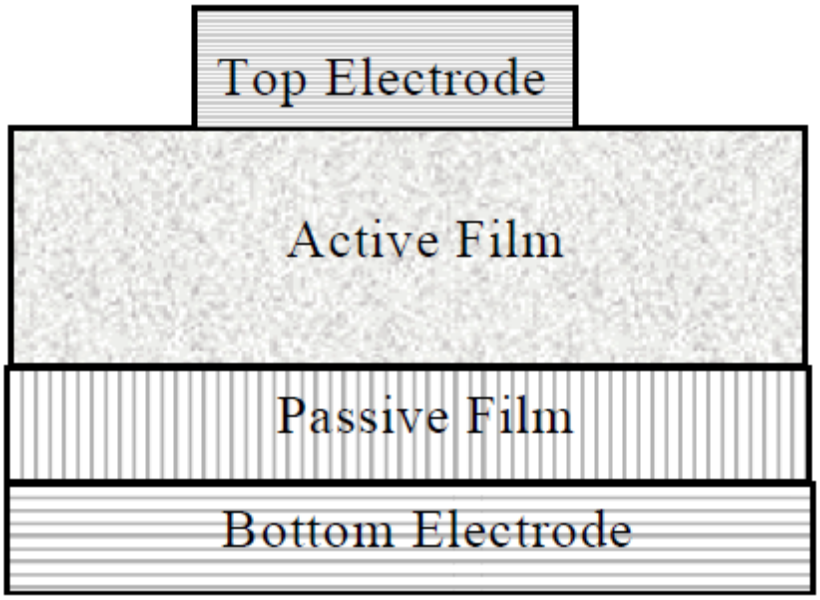



**Fig. 1-5 Structure of Polymeric memristor device (adopted from [18]).**

### *1.3.7 Spin memristive systems*

Spin-based memristive systems, on the contrary to ionic and molecular nano structured systems, depend on the degree of freedom property in electron spin. In these systems, the polarization of electron spin is altered allowing for hysteresis like behaviors to occur. This alternation is often throughout the movement in a magnetic domain wall which separates magnetic domains of different polarities [11].

Wang and some researchers showed three examples of probable spintronic memristors in 2009 [21]. These instances are based upon magnetic domain wall motion and switching of spin-torque-induced magnetization as shown in Fig. 1-6. Also, they verified that the spintronic device can be designed to memorize and explore the continuum state of voltage and current. Furthermore, in 2011, the existence of spintronic memristor based on domain wall motion was demonstrated experimentally. More discussion about this spintronic memristor is presented in [22].

Some types of semiconductor based spintronic structures have a memristor like behavior. This behavior is totally based on the degree of freedom of the electron spin which allows for more beneficial control than the nanostructures ionic transport .When the external excitation is alternated, the tuning of electron spin polarization takes place after time because of the relaxation processes and diffusion resulting in hysteresis [23].

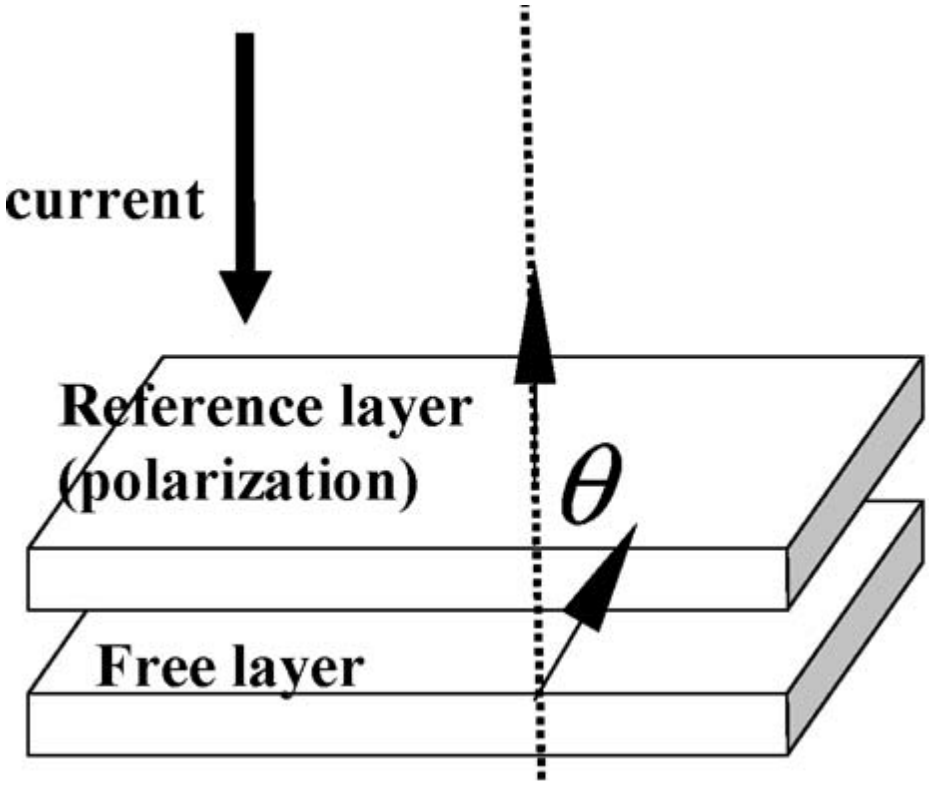



**Fig. 1-6 An example of Spin memristive systems (adopted from[21]).**

## *1.4 Memristor models*

Due to the potential of memristor device in life applications and the absence of commercially available physical devices, it should be appropriately modeled in order to be used in the simulation, design, and analysis of memristor based circuits. Besides, the required attributes of the memristive systems for different applications are not the same, i.e., in memristor based memory applications, the state variable is required to arise nonlinear dependence on charge for providing non-destructive read operations. While in some other applications as the analogue counter, the state variable is preferred to linearly relate on the charge [24]. Thus there is a need to derive certain models of various memristive systems for their particular applications under the assumption that the industry would manage to develop nano-memristive devices enjoying the recommended characteristics [25]. Instead, the researchers suggest models describing the required characteristics while fitting the measured data of the practically realized memristors. A number of electronic models have been introduced to describe the electrical behavior of memristor devices. For example, the linear dopand (ion) drift model [3], the nonlinear dopand (ion) drift model [26], [27], Simmons tunnel barrier model [28], [29], the ThrEshold Adaptive Memristor (TEAM) model [24], and Voltage ThrEshold Adaptive Memristor (VTEAM) model [30]. Some of them represent the device as two resistors in series as in [31], [32] and others suggest different device representations. i.e., resistor in series with tunneling barrier as in [29] or conduction, transition, and insulation regions as in [33]. There are also many research groups who developed SPICE macro models of memristor [32], Verilog-A models [34], and Matlab model [35].

A memristive system, in the main, is described by two equations, the dynamical equation and the 'quasi-static' conduction equation. The 'quasi-static' conduction equation illustrates the relation between the voltage across the device to the current through it at any time instant via a generalized resistance R $(w, i)$, or generalized conductance G $(w, v)$, as follow

$$\begin{cases} v = R(w,i)i, & for\ charge\ controlled\ memristor \\ i = G(w,v)v, & for\ flux\ controlled\ memristor \end{cases} \quad (1\text{-}2)$$

on the other side , the dynamical equation clearly emphasizes that the derivative of the state variable $(w)$ is a function of the current through the device and the state itself [36],

$$\frac{dw}{dt} = \begin{cases} f(w,i) & for\ charge\ controlled\ memristor \\ f(w,v) & for\ flux\ controlled\ memristor \end{cases} . \quad (1\text{-}3)$$

Hereinafter, the most well known memristor models:

*1.4.1 HP memristor model*

HP $TiO_2$ memristor was the first implementation carrying the name of memristor. This memristor is simply composed of two sub-layers of titanium dioxid, which is a stable compound. These sub-layers are chemically different and sandwiched between two platinum electrodes as shown in Fig 1.7. The first sub-layer is $TiO_2$ of high impedance perfect titanium oxide, but the other sub-layer misses some of its oxygen which make it conductive. This is called oxygen-vacationed titanium dioxide ($TiO_{2-x}$) sub-layer and it is regarded as the originally doped region. The oxygen vacancies are donors of electrons. Hence, the vacancies are positively charged. At the time a positive voltage into the top electrode is applied, it will repel the oxygen vacancies in the $TiO_{2-x}$ sub-layer (doped region) downward into the pure $TiO_2$ sub-layer (undoped region). Transferring the oxygen vacancies from the $TiO_{2-x}$ layer to $TiO_2$ layer increases the width of $TiO_{2-x}$ layer and decreases $TiO_2$ width.

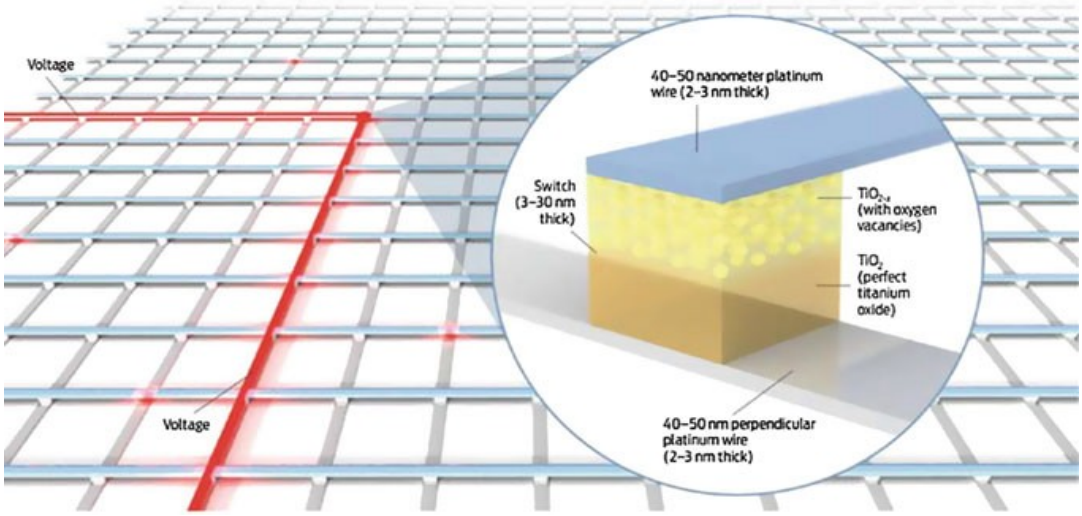



**Fig. 1-7 Construction of Hp memristor (adopted from [26])**

On the contrary, applying a negative voltage has the opposite result where the oxygen vacancies are attracted towards the top electrode making the undoped sub-layer wider and shrinks the doped sub-layer.

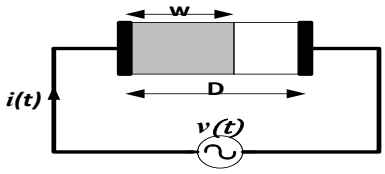



**Fig 1-8 An AC excitation "v (t)" is applied across a memristor element with total width "D" and doped region of width "w" and passing current "i(t)". (adapted from [27])**

According to the previous device structure, the HP team introduced a basic mathematical behavioral model for their proposed memristor [3], [37]. This model is based on two series resistors $R_{on}$ and $R_{off}$ which are the resistances of the doped and the undoped regions respectively. It is assumed that the doped region of width, *w*, and the physical device is of total width, *D*, as demonstrated in Fig. 1-8.

Thus, the instantaneous memristor resistance is written as in (1-4).

$$R_m = X.R_{on} + (1 - X).R_{off} \tag{1-4}$$

, where $X=W/D$, $R_{on}$ is the resistance when memristor is fully doped, and $R_{off}$ is for the fully undoped memristor [3][38]. Correspondingly, the expression of the rate of state change as a function of the current is expressed in (1-5) [31].

$$\frac{dX}{dt} = k \cdot i(t), \tag{1-5}$$

In the above equation, $X = w/D$, $k = \mu_v R_{on} / D^2$, $\mu_v$ is the memristor dopant drift average mobility, and $R_{on}$ is the memristance minimum value which is reached when the device is fully doped [31]. The state change equation is a linear function in current as shown in (1-5), so this model is called linear dopand drift model where the velocity of the dopands is assumed to be linearly dependant on the current [3].

From [31], the memristor current can be expressed as

$$i(t) = \frac{v(t)}{\sqrt{R_{init}^2 - 2kR_d\Phi(t)}}, \tag{1-6}$$

$R_{init}$ is the initial memristor resistance, $\Phi(t) = \int_0^t v(t)dt$ is the instantaneous flux, and $R_d = R_{off} - R_{on}$ is the difference between the memristance margins. For sinusoidal input voltage $v(t) = V_0 \sin(\omega_0 t + \theta_0)$, whereas $V_0, \omega_0$, and $\theta_0$ are the sinusoid input peak, radial frequency, and initial phase, respectively. So, the memristor pinched hysteric I-V characteristics for sinusoidal input using this linear model is drawn utilizing Matlab simulation environment as shown in Fig.1-9.

Consequently, the expression of a memristance as function in time can be estimated using (1-6) as in (1-7) and modeled using Verilog-A as in [34].

$$R_m(\mathrm{t}) = v(\mathrm{t})/\mathrm{i}(\mathrm{t}) = \sqrt{R_{init}^2 - 2kR_d\Phi(t)} \quad (1\text{-}7)$$

It is obvious that, this model assumes that the vacancies have no restrictions to move through the whole length of the device. However, it is not true given that, the vacancies decelerate a lot at the device boundaries. Since, if they move freely from end to end of the device, it implies that there will be no oxygen vacancies physically in the device and the doped region length is zero, which is not logical. Likewise, the doped region cannot seize all the length; because it will cause no undoped region then the device will not perform as intended. In order to get over the problem of the boundaries, a window function (f (w) or f (x)) is assumed and inserted to the state variable derivative as follow [32].

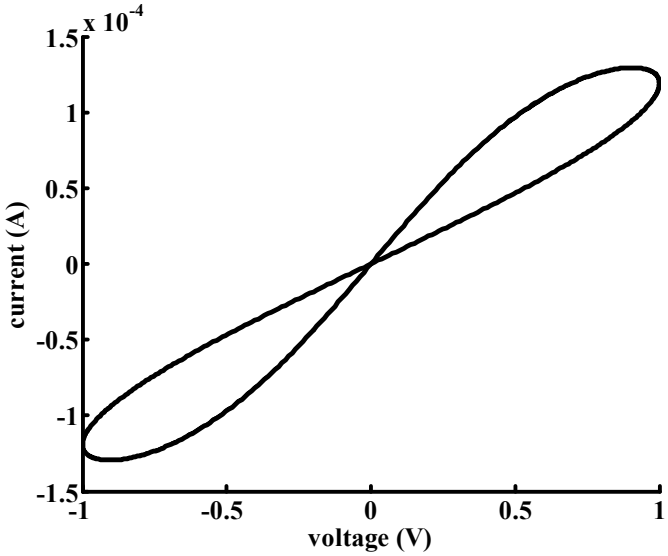



**Fig. 1-9. Simulated memristor current versus voltage using linear dopant drift model for $0^0$ phase shift with memristor parameters: $R_{on}$ =100Ω, $R_{off}$=38kΩ, $R_{init}$=11kΩ, $D$=10nm, $\mu_v$=10f $m^2s^{-1}v^{-1}$, with 1v amplitude voltage and frequency of 1Hz.**

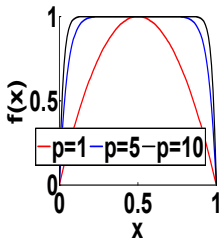
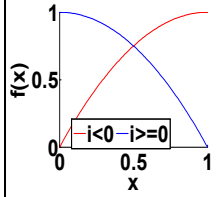
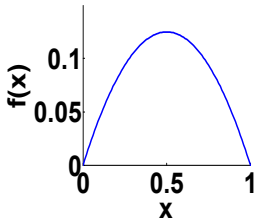
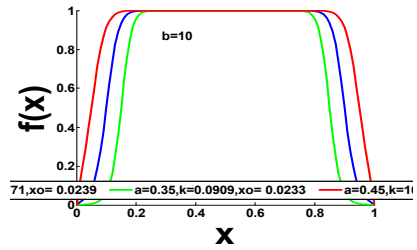
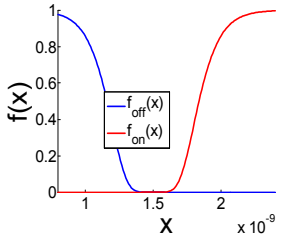
*1.4.1.1 Window functions*

In the linear ion/dopant drift model (HP model), the acceptable value of the state variable is bounded to the interval [0, D]. To fulfill these bounds, $dXdt{=}k{\cdot}i(t),$ at boundaries is multiplied by (1-3). It constrains the state derivative to be identical to zero at boundaries. One possible approximation for the needed function is an ideal rectangular window function (where the value of the function is zero at the boundaries and one for any other values of the state variable). It is also possible to add a nonlinear ion drift phenomenon, such as a decrease of the ion drift speed close to the bounds. Joglekar, Biolek, Prodromakise, Piecewise, and Team are the most popular nonlinear windows. The comparison between these functions is reported in Table 1-1.

*1.4.2 Non-linear dopant drift model*

Although, the linear ion drift model is axiomatic and fulfills the equations of the basic memristive system, experiments have demonstrated that the performance of implemented memristive devices diverges vastly from this linear model and is greatly

**Table 1--1 comparison between the most popular window functions ( adopted from [11])**

| **Window function** | **Joglekar** [40] | **Biolek** [41] | **Prodromakis** [42] | **Piecewise** [43] | **Team** [24] |
|---|---|---|---|---|---|
| *f(x)* | $1-(2x-1)^{2p}$ | $1-(x-stp(-i))^{2p}$ | $j(1-[(x-0.5)^2+0.75]^p)$ | $\begin{cases}(1+(\frac{x-0.5}{a})^{2b})^{-1} & x_o \le x \le 1-x_o \\ kx(1-x) & otherwise\end{cases}$ | $exp[-exp(\frac{\lvert x-x_{on,off}}{we})]$ |
| symmetry | yes | yes | yes | Yes | Not necessary |
| Resolve boundary conditions | No | yes | Partially yes | Partially yes | Partially yes |
| Impose nonlinear drift | partially | partially | partially | partially | yes |
| Scalable factor $f_{max} \le 1$ | No | No | Yes | Yes | No |
| Fits memristor model | Linear / Nonlinear ion drift/ TEAM | Linear/ nonlinear ion drift/ TEAM | Linear/ nonlinear ion drift/ TEAM | Linear/nonlinear ion drift/ TEAM | TEAM for Simmons tunneling barrier fitting |
| Function response |   |   |   |   |   |

nonlinear [27][39]. This nonlinear I-V characteristic is desirable for some applications as logic circuits. Accordingly, more proper memristive device models have been introduced. In [26], a model is presented based on the experimental findings described in [27]. Thereby, the non-linear dopant drift model is regarded as a more realistic model compared to the linear dopant drift model. It incorporates the most known non-idealities of practically implemented memristors such as asymmetrical on/off switching, threshold, and nonlinear memristance (versus voltage and state) relationships [26]. Besides, it is dependent on the experimental measurements of a realistically fabricated memristor [27]. In this model, the current voltage relationship is

$$i(t) = (w(t))^n \cdot \beta \cdot sinh\big(\alpha v(t)\big) + \chi\big(exp\big(\gamma v(t)\big) - 1\big), \tag{1-8}$$

where n is a variable that determines the state variable impact on the current, while α, β, $\gamma$ and $\chi$ are experimental fitting parameters. The state variable, in this model, is a normalized parameter restricted by the interval [0, 1]. This model assumes asymmetric switching actions. At the time the device is in the 'ON' status, the state variable is close to 'one' then the current is governed by the first term in (1-8) which expresses a tunneling phenomenon.

On the contrary, when the device is in the 'OFF' status, the state variable is close to 'zero' and hence the current is governed by the second term in (1-8), which look like an ideal diode equation. This model assumes a nonlinear dependence on the voltage in the differential equation of the state variable, as clear in (1-9)

$$\frac{dw}{dt} = \begin{cases} a \cdot f(w) \cdot v(t)^m & |v(t)| > v_{th} \\ 0 & |v(t)| < v_{th} \end{cases} \tag{1-9}$$

whereas $a$ and $m$ are constants, $m$ is an odd integer, $v_{th}$ is the threshold voltage below which the change in the state variable is neglected and $f(w)$ is the model window function. Joglekar window was selected to be used in the SPICE form of the simulation model [26] which is $f(w) = 1-(2w-1)^{2P}$, $P$ is an integer constant. The I-V characteristics of a nonlinear ion drift memristive device for sinusoidal input signal is demonstrated in Fig. 1-10. A comparable model is suggested by the same authors in [44]. In which, the same I-V relationship is described with a more complex state derivative equation.

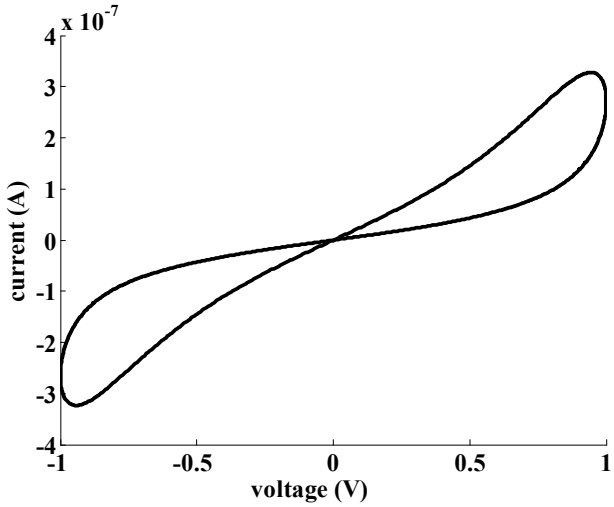



**Fig. 1-10 Memristor current versus voltage using nonlinear dopant drift model.**

*1.4.3 Simmons Tunnel Barrier Model*

The aforementioned models (linear and nonlinear ion drift) rely on representing the memristor as two resistors in series. One of them is for the oxide region and the other for the doped oxide region. In [28], a more precise physical model was proposed. In which, an asymmetric and nonlinear switching behavior is assumed. Moreover, the movement of the ionized dopants depends exponentially on the current in the state change equation. In this model, the memristor is represented as an electron tunnel barrier in series with a resistor which differs than the two resistors in series in the linear drift model, as shown in Fig 1-11. The state variable, in this case, is the width of Simmons tunnel barrier (x) [29]. Here, the derivative of x can be explained as the drift velocity of the oxygen vacancy, which is

$$\frac{dx(t)}{dt} = \begin{cases} C_{off}\ sinh(\frac{i}{i_{off}})\ exp\left[-exp\left(\frac{x-a_{off}}{w_c}-\frac{|i|}{b}\right)-\frac{x}{w_c}\right], & i>0\,, \\ C_{on}\,sinh(\frac{i}{i_{on}})\ exp\left[-exp\left(-\frac{x-a_{on}}{w_c}-\frac{|i|}{b}\right)-\frac{x}{w_c}\right], & i<0, \end{cases} \tag{1-10}$$

where $\boldsymbol{c_{off}}$ , $\boldsymbol{c_{on}}$ , $\boldsymbol{i_{off}}$, $\boldsymbol{i_{on}}$, ,$\boldsymbol{a_{off}}$ ,$\boldsymbol{a_{on}}$, and $\boldsymbol{w_c}$are fitting parameters. Fig.1-12 illustrates (1-10) for the fitting parameters proposed in [28].

The physical meaning behind the performance shown in (1-10) is not fully understood up till now, but it is interpreted as a combination of local Joule heating developing the oxygen vacancies and high electric fields nonlinear drift [24]. In realized memristive devices, the OFF switching is considerably slower than the ON switching because each of the diffusion of the oxygen vacancies from $\mathbf{TiO_{2-x}}$ to $\mathbf{TiO_2}$, and the drift of the oxygen vacancies resulting from the internal electric field is not same for positive and negative voltages.

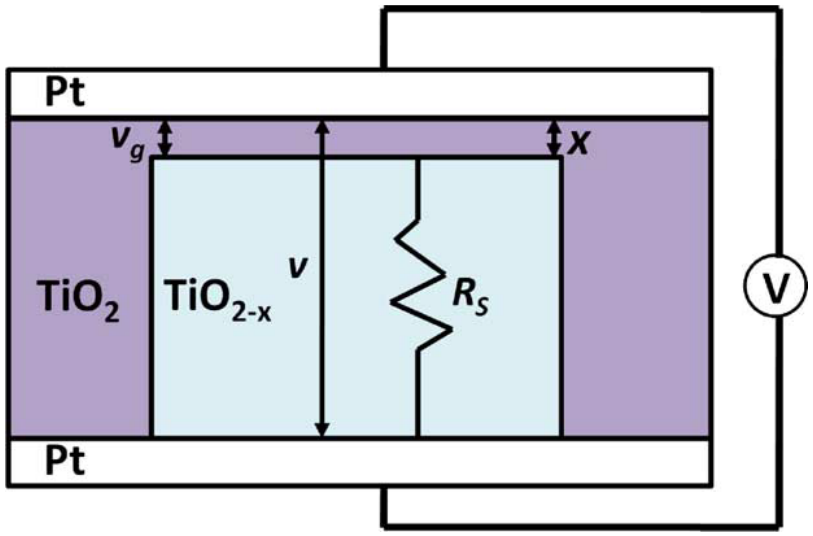



**Fig. 1-11 Physical model of Simmons tunnel barrier memristive device.$x$ is the width of the oxide region (the state variable), $V$ is the voltage applied on the device, $v_g$ is the undoped region voltage, and $v$ is the device internal voltage (adopted from [27]).**

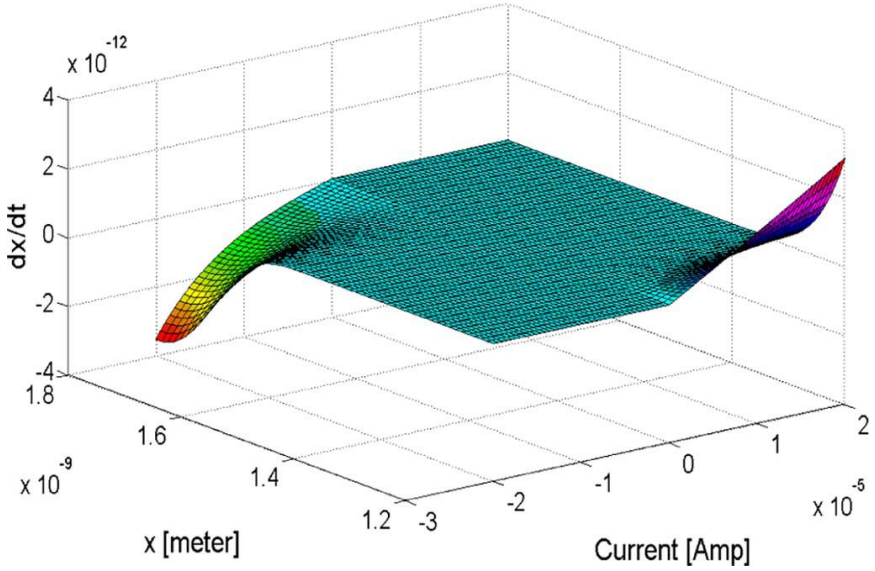



**Fig. 1-12 The state variable rate of change as described in (1-10) (adopted from [24]).**

For a positive voltage, the direction of diffusion and drift is opposite, while for negative voltage, the drift of the oxygen vacancies and the diffusion are in the same direction [45]. The parameter $\boldsymbol{c_{on}}$ is of magnitude larger than the parameter $\mathbf{c_{off}}$ and both influence the magnitude of the change of $\boldsymbol{x}$. The parameters $\boldsymbol{a_{off}}$ and $\boldsymbol{a_{on}}$ restrict, respectively, the maximum and minimum bounds for $\boldsymbol{x}$. The parameters $\boldsymbol{i_{off}}$ and $\boldsymbol{i_{on}}$ significantly constrain the current threshold. Below the current threshold, the change in the derivative of $\boldsymbol{x}$ is neglected. As this nonlinear I-V characteristic is required for logic circuits, the current threshold feature is also desirable for digital applications. Therefore, the features represented in this model are encouraging for memristor based digital logic

applications. Resulting from the exponential dependence on $\boldsymbol{x - a_{off}}$ or $\boldsymbol{x - a_{on}}$, the change of the state variable is much smaller within the allowable range. For that reason, there is no need for a window function within this model. However, the relationship between the current and voltage , in this model, is regarded as an implicit equation depending on the Simmons tunneling model [29], where the internal voltage on the device $\boldsymbol{v}$ is not essentially equal to the voltage applied on the device $\boldsymbol{V}$. A SPICE model of the Simmons tunnel barrier model is available in[46]. Nevertheless, this model is complex and computational inefficient.

### *1.4.4 ThrEshold Adaptive Memristor Model (TEAM) and Voltage ThrEshold Adaptive Memristor Model (VTEAM)*

Although, Simmons tunnel barrier model is one of the most precise physical models of memristive devices, this model is somewhat complicated, with no clear relationship between voltage and current. This model suits only a certain type of memristive devices (so it is not generic in nature).

Digital applications such as logic and memory require a model that is not only highly nonlinear, and sufficiently accurate, but also simple for calculations. Hence,

Simmons tunnel barrier model is not an encouraging candidate for memristor based applications. Therefore, a reasonably accurate and computationally efficient model was desired. TEAM model provides these features and also can be fit to other practical memristive devices which makes it appropriate for circuit simulation [24]. TEAM model has simpler equations rather than the complex expressions in the Simmons tunnel barrier model while describing the same physical behavior using uncomplicated mathematical functions. The author assumed that no change in the state variable below a specific threshold, and a polynomial dependence of the state rather than an exponential dependence. He modeled the dependence of the internal state derivative as independently multiplying two independent functions; one function depends on the current and the other function depends on the state variable. He augmented the separation of variables performed in the state variable equation to the small changes in the electric tunnel width. Under these hypotheses, the derivative of the state variable in TEAM simplified model is

$$\frac{\mathrm{dx(t)}}{\mathrm{dt}} = \begin{cases} \mathrm{k_{off}} \cdot \left(\frac{\mathrm{i(t)}}{\mathrm{i_{off}}} - 1\right)^{\alpha_{\mathrm{off}}} \cdot \mathrm{f_{off}(x)}, & 0 < \mathrm{i_{off}} < i \\ 0, & \mathrm{i_{on}} < i < \mathrm{i_{off}} \\ \mathrm{k_{on}} \cdot \left(\frac{\mathrm{i(t)}}{\mathrm{i_{on}}} - 1\right)^{\alpha_{\mathrm{on}}} \cdot \mathrm{f_{on}(x)}, & \mathrm{i} < \mathrm{i_{on}} < 0, \end{cases} \qquad (1\text{-}11)$$

where $\alpha_{off}$ ,$\alpha_{on}$ ,$k_{off}$ ,and $\mathrm{k_{on}}$ are constants, $i_{on}$ and $i_{off}$ are current thresholds, and the internal state variable here is the effective electric tunnel width which is represented by the variable $(x)$. The constant $k_{off}$ is a positive number, whereas the constant $k_{on}$ is a negative number. The functions $f_{on}(x)$ and $f_{off}(x)$ $are$ window functions as described previously. The functions $f_{on}(x)$ and $f_{off}(x)$ are not essentially equal, where the dependence on $x$ may be asymmetric.

Besides, the assumed polynomial current voltage relationship in TEAM is

$$v(t) = \left[R_{on} + \frac{R_{off} - R_{on}}{x_{off} - x_{on}}(x - x_{on})\right] \cdot i(t) \qquad (1\text{-}12)$$

It is foreseen that, the assumptions proposed in TEAM increase the analysis simplicity and its computational efficiency [24]. Additionally, the author extended the TEAM model, which particularly describes the behavior of the current controlled memristors, in a form of new model called VTEAM [30]. VTEAM (Voltage ThrEshold Adaptive Memristor Model) describes the performance of the voltage controlled memristors. This developed model has the same advantage of TEAM model and is suitable for the voltage controlled memristors based applications. The current-voltage relationship of the VTEAM model is undefined, it can be arbitrary selected from any current-voltage characteristics supporting the voltage threshold feature. The dynamical equation (the realization of (1-3) in the VTEAM model is comparable to the derivative of the state variable in the TEAM model, which is

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}\ (\frac{v(t)}{v_{off}} - 1)^{\alpha_{off}} \cdot f_{off}(w), & 0 < v_{off} < v \\ 0, & v_{on} < v < v_{off}. \\ k_{on}\ (\frac{v(t)}{v_{on}} - 1)^{\alpha_{on}} \cdot f_{on}(w), & v < v_{on} < 0 \end{cases} \qquad (1\text{-}13)$$

Like TEAM, $\alpha_{off}$ ,$\alpha_{on}$ ,$k_{off}$ ,and $k_{on}$ are constants, $v_{on}$ and $v_{off}$ are voltage thresholds.

It turns out that, the memristor characteristics that maximize the performance improvement of memristor based systems depend on the target application. Therefore one model cannot meet the requirements of all memristor based applications. This necessitates the existence of different models to describe different memristor systems. For example, the linear and nonlinear ions drift models describe memristors of relatively large dynamic ranges. Hence they are proper for analog applications, while the TEAM and VTEAM models are more appropriate for memory and logic applications where they describe the rapidly switching memristors (with respect to the operating frequency) between the two memristance extremes values.

### *1.4.5 Models exploited in the thesis*

Within the scope of the thesis, specific range of memristor dynamics is employed for implementing the proposed demodulators, phase detector, and VCO (Voltage Controlled Oscillator) circuits. These circuits work on the principle of a voltage divider with adaptively varying dividing ratio. Therefore, the linear and nonlinear ion drift models were more suitable than TEAM and VTEAM models. As well as, the linear and nonlinear ion drift models were more suitable than some recent accurate and practical memristor representative compact modeling works [47]–[50]. Since these recent models are quite complicated, without an explicit relationship between current and voltage, computationally incompetent, and not general in nature.

Initially, linear dopant drift model has been used to provide closed form formulas which prove the proposed concept analytically. After that, the use of more realistic nonlinear model has been adopted to validate the results of the first model taking into considerations the non-ideality features. The nonlinear ion drift models is based on fitting real measured data incorporating most known nonlinear effects (threshold, nonlinear memristance versus state and voltage relationships). It is also stable over long simulation time, correctly predicts the behavior of circuits and provides a better accuracy.

## *1.5 Memristor Applications*

Memristive devices are innovative devices [24], which offer several advantages: good scalability, nonvolatility, compatibility with Complementary Metal-oxide-Semiconductor (CMOS) technology (both electrically and in terms of manufacturing technology), and effectively no leakage current. Therefore, it can be used in applications ranging from memory and logic to neuromorphic systems. Nonvolatile memories for computer manufacturing [51]–[54] are considered the most promising applications of memristive systems. Also, there are several research groups investigated their possible exploitation for analog signal processing [25], [55]–[58]. By in-depth exploring one of the famous databases of memristor research publications called "Memlinks", [59], some statistics can be derived:

1. About 30 percent of the typical papers are about oscillators [60], one half of them about chaotic oscillators.

2. Around 20 percent of the publications are dedicated to memristive systems for analog computations, mainly in the function of neuromorphic learning circuits [61] and massively-parallel computational systems [62].

3. About 20 percent of the publications proposed linear and nonlinear applications of memristive systems, i.e.: controllers [63], filters [57], and amplifiers with electronically modifiable parameters [56], nonlinear non-inertia circuits (MIN/MAX circuits designed for fuzzy logic [64], circuits for ESD protection [65], etc.), modulators and demodulators (UWB receivers [66], shift-keying techniques [67], and conventional analog modulations [68]).

It can be also noted that until now, papers from the area of audio- [69] or image-signal processing [70], AD and DA conversion [71], and sensors [72] emerge only seldom. The idea of replacing a resistor by a memristor, where its memristance can be adjusted by the user, acts as a starting point for designing programmable filters [57], oscillators [73], comparators [56], or amplifiers. However in this case, the designer should be aware of the importance of using a memristor model considering the threshold feature which is illustrated in (1-14) for charge controlled memristors and (1-15) for flux controlled memristors.

$$\frac{dw}{dt} = \begin{cases} f(w,i) & |v(t)| > v_{th} \\ 0 & |v(t)| < v_{th} \end{cases} \quad \text{(1-14)},$$

$$\frac{dw}{dt} = \begin{cases} f(w,v) & |i(t)| > i_{th} \\ 0 & |i(t)| < i_{th} \end{cases} \quad \text{(1-15).}$$

$v_{th}$, $i_{th}$ are the voltage and the current thresholds respectively and below them the change in the state variable is neglected. In these designs, the memristors voltages should not exceed the threshold voltage "$v_{th}$" to ensure that there is no change in the memristors state variables so the memristors operate as linear resistors in these applications. By this way, the designer avoids the undesirable nonlinear distortion.

# Chapter Two

# MEMRISTOR RESPONSE FOR DC AND PERIODIC SIGNALS USING LINEAR AND NONLINEAR DOPANT DRIFT MODELS

It is worth noting that for maximizing the exploitation of memristor elements in different applications, the response of this element for different input signals should be studied profoundly. Therefore in this chapter, the dependence of the instantaneous memristance value and its I–V characteristics on the attributes of the applied signals is investigated for DC, sinusoidal, square, and triangle periodic signals. The linear dopant drift model is used to derive a closed form expression for the instantaneous memristance for each applied input signal. Furthermore, simulations using linear and nonlinear dopant drift memristor models are performed in Matlab and Cadence simulation environments, in order to validate the analytical results and confirm the same tendency.

## *2.1 Memristor response for DC input*

According to the linear dopant drift model and for a memristor with a DC input, the boundary of the dopants will move in one direction towards $w = D$ or $w = 0$ limits, relying on the polarity of the input voltage. After dopants arrive one of its two borders, the memristor will operate as a constant resistance equals to $R_{on}$ in case of $w = D$ or $R_{off}$ for $w = 0$. By calculating the flux, $\Phi(t)$, in (1-7), the instantaneous memristance can be evaluated as [38],

$$R_m^2(t) = R_{init}^2 - 2kR_d V_{DC} t \tag{2-1}$$

where $V_{DC}$ is the amount of the DC voltage. Let the time required for memristance saturation be represented by $t_{sat}$, at which $R_m$ reaches either $R_{off}$ or $R_{on}$. It can be evaluated using (2-1) such that,

$$t_{sat} = \begin{cases} \frac{R_{init}^2 - R_{off}^2}{2V_{DC} K R_d}, V_{DC<0} \\ \frac{R_{init}^2 - R_{on}^2}{2V_{DC} K R_d}, V_{DC>0} \end{cases} \tag{2-2}$$

Equation (2-2) shows that more time is needed for memristance saturation using smaller input voltages. The maximum required saturation time is obtained in case of a memristance initialized at one boundary and the applied DC pushes it to the other boundary. Therefore, the maximum required saturation time without considering the initial memristance value is given by [38].

$$\mathrm{t_{sat}(max)} = \frac{\mathrm{R_{off} + R_{on}}}{2\mathrm{K}|\mathrm{V_{DC}}|} \tag{2-3}$$

Which can be approximated as

$$t_{sat}(\max) \approx \frac{D^2 R_{off}}{2\mu_v R_{on} |V_{DC}|} \quad \text{for} \quad R_{off} \gg R_{on} \tag{2-4}$$

as noticed previously by HP scientists [3].

## 2.2 Memristor response for sinusoidal input

As a starting point, the linear dopant drift model [32] is adopted in order to demonstrate analytically the response of the memristor to the different attributes of the sinusoidal signal (amplitude, frequency, and initial phase) in compact form, and later compared with the simulation results using Matlab linear dopant drift model [35]. In [35], '*p*' is a positive number which is responsible for the nonlinearity of the dopant drift model. The reduction of '*p*' stands for the increase of the nonlinearity degree for the memristor dopant drift model [32], [35], [74].Next, the simulation results using a more realistic non-linear model is presented [26].

### 2.2.1 Analytical analysis and simulated results using the linear dopant drift model

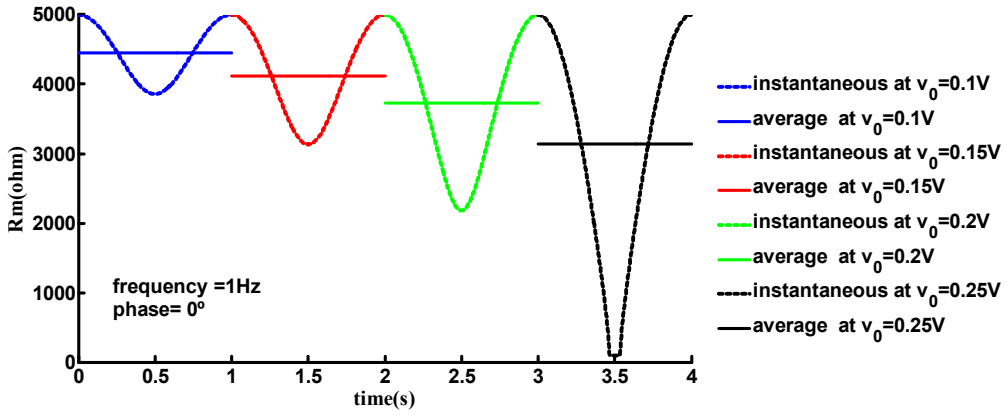
If the input voltage is represented as: $v(t) = v_0 \sin(w_0 t + \theta_0)$, using (1-7), the instantaneous memristance as a function in the sinusoidal signal attributes can be expressed as:

$$R_m^2 = R_{init}^2 + \frac{2kR_d V_0}{\omega_0}(\cos(\omega_0 t + \theta_0) - \cos\theta_0), \qquad R_m \in (R_{on}, R_{off}) \tag{2-5}$$

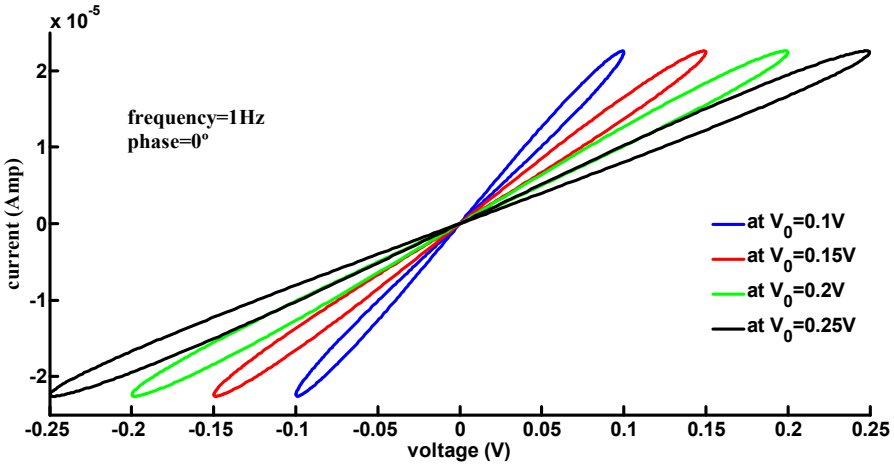
$\omega_0, V_0$ ,and $\theta_0$ are the sinusoid input radial frequency, peak, and initial phase, respectively [75]. The instantaneous memristance and i-v curves for different amplitude values are displayed in Fig. 2-1(a) and Fig. 2-1(b), respectively. From which it can be noticed that, the dynamic range of the memristance increases as the amplitude increases, the memristance may saturate at one or both of its boundaries in case of relatively high amplitude value (as in case of $V_0$=0.25V where $R_m$ saturated at $R_{on}$), and the pinched hysteresis loop of *i-v* characteristic is independent on the amplitude of the stimulus. The parameters of the memristor for Fig. 2-1, Fig. 2-2, Fig. 2-3, and Fig. 2-4 are selected as in Table 2-1.

**Table 2.1 The memristor parameters used for plotting Fig. 2-1, Fig. 2-2, Fig. 2-3, and Fig. 2-4.**

| Parameter | Fig.2-1 | Fig.2-2 | Fig.2-3 | Fig.2-4 |
|---|---|---|---|---|
| $R_{on}$ | 100Ω | 100Ω | 100Ω | 100Ω |
| $R_{off}$ | 16kΩ | 16kΩ | 38kΩ | 16kΩ |
| $R_{init}$ | 5kΩ | 11kΩ | 11kΩ | 10kΩ |
| $\mu_v$ | 10f $m^2s^{-1}v^{-1}$ | 10f $m^2s^{-1}v^{-1}$ | 10f $m^2s^{-1}v^{-1}$ | 10f $m^2s^{-1}v^{-1}$ |
| $D$ | 10nm | 10nm | 10nm | 10nm |




(a)



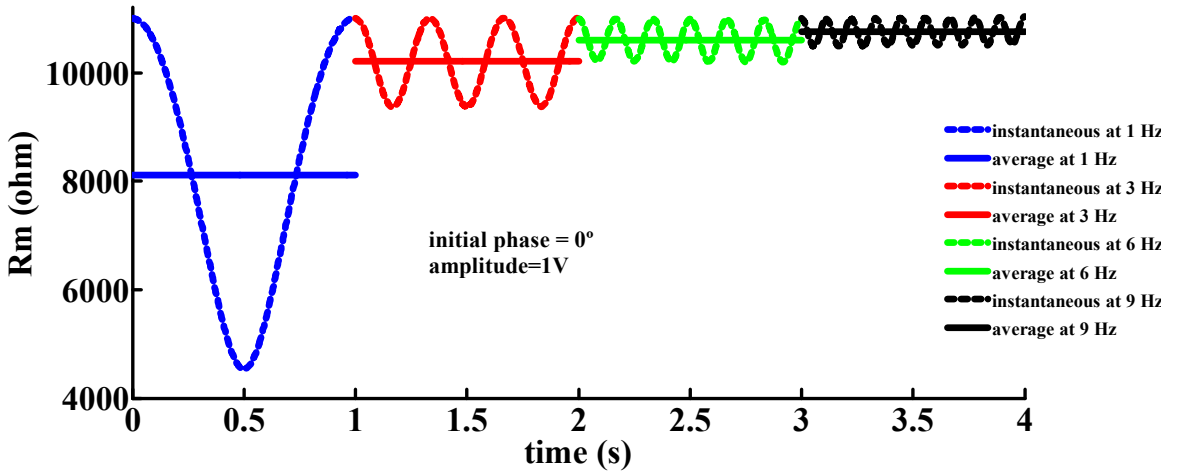

(b)

**Fig. 2-1 (a). Analytical instantaneous and average memristance for 0.1, 0.15, 0.2, and 0.25V amplitude values.**

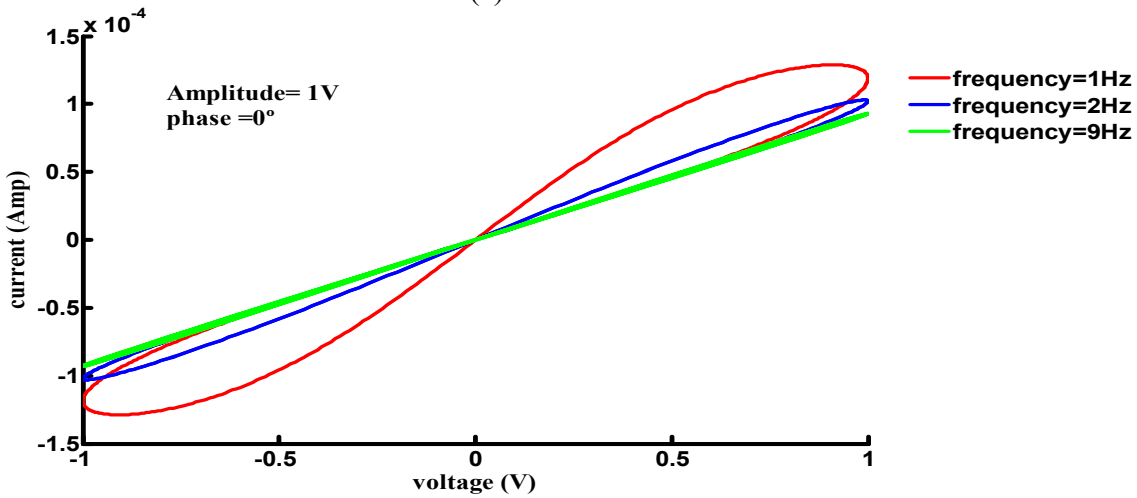
**(b). Analytical memristor current versus voltage for 0.1, 0.15, 0.2, and 0.25V amplitude values.**

While the instantaneous memristance and *i-v* curves for different frequency values are displayed in Fig. 2-2(a) and Fig. 2-2(b) respectively. It can be seen from Fig. 2-2 that the hysteresis loops are always pinched at the origin, the lobe area shrinks with the increase of the frequency, and finally the hysteresis loop turns into a single-value function at infinite frequency [76].

On the other hand, the influence of the initial phase on the memristance variation and the average of the memristance over a complete single cycle was recently studied by us, [75] and [77]. The gained results have allowed the incorporation of memristors in new circuit building blocks for common communication applications as will be exhibited in next chapters.




(a)




(b)

**Fig.2-2 (a). Analytical instantaneous and average memristance for different stimulus frequencies.**

**(b). Analytical memristor current versus voltage for different stimulus frequencies.**

Due to the association between the instantaneous memristance and the signal initial phase which is clear in (2-5), it is expected that the width of the hysteresis loop and the slope of the memristor pinched I-V hysteresis are both varied by changing the phase of the sinusoid input signal. Simulations through Matlab linear dopant drift model [35] are carried out to prove the consistency of the analytical results as demonstrated in Fig. 2--3. The parameters of the memristor used to plot Fig. 2-3 are selected as stated in Table 2-1. Fig. 2-3(a) illustrates a sinusoidal input signal with unlike phase shift in each cycle. Fig. 2-3(b) shows the analytical instantaneous memristance and its average over a complete single cycle using (2-5) and the simulated results using Matlab [35]. The pre-mentioned computations are evaluated and plotted for $0^o$, $90^o$, $180^o$, and $270^o$ phase shift. The difference in memristance variation for different phases can be easily noticed, since for $0^o$ phase sinusoid, as an instance, the memristance falls down in the first cycle half (as

shown in Fig. 2-3(b) in the time between 0s and 0.5s) because the voltage applied on the memristor is positive (as shown in Fig. 2-3(a) in the time between 0s and 0.5s). Nevertheless, it returns to raise from its least value in the second cycle half since the voltage applied is negative (through 0.5s to 1s), which finally rests it to the initial state, that is $R_m$=$R_{init}$ , thus, the memristance average becomes smaller than the initial value.

However, the memristance increases in the first cycle half for $180^o$ phase shift (as demonstrated in Fig. 2-3(b) for the duration between 2s to 2.5s) when the applied voltage is negative (as shown in Fig. 2-3(a) through the time between 2s to 2.5s) and goes back to decrease from its highest value in the second cycle half when the applied input voltage is positive (for the period between 2.5s to 3s) hence the memristance average over this cycle is larger than its initial value.

Apparently from Fig. 2-3 (b) that, the memristance variation during the first cycle half in case of 90º (starting from 1s to1.5s) is similar to that during the second cycle half if the phase shift equals 270º (beginning from 3.5s to 4s) and the opposite is correct for 270º (between 1.5s to 2s) and 90º (betweens 3s to 3.5s), for that reason the memristance average for each of 270º and 90º phase shifts are the same.

Consequently, one memristor can be used to discriminate between signals of unlike phases if the average memristance at these phases is different (e.g. signals of $0^o$ and $180^o$ phase shift), whereas one memristor is not sufficient to distinguish between signals with $270^o$ and $90^o$ phase shift, as an example.

In this way, the demonstrated response of the average memristance against different phase shifts would construct a basis for our suggested set of demodulators designs (as will be depicted in the next chapter).

The memristor resistance versus voltage and its hysteric I-V characteristics are also clarified in Fig. 2-3(c), and Fig. 2-3(d) respectively, all of the preceding subfigures includes both simulated and analytical results and are identified for $0^o$, $90^o$, $180^o$, and $270^o$ phase shifts. Fig. 2-3(c) shows the variation of the width and slope of the pinched I-V characteristic with the variation of the sinusoid input phase. The change in the dynamic range of the memristance with different initial phases is apparent in Fig. 2-3(d). The conformity between simulated and analytical results (using the linear dopant drift model) is clear in Fig. 2-3(b) and Fig. 2-3(d) in cases of 270º, 90º, and 0º phase shifts, but small error exists with 180º phase shift [75], [77].

Furthermore, the average resistance of the memristor over the cycle for 45º shifted form of the prior sinusoid input instances ($270^o$, $0^o$, $90^o$, and $180^o$) resulting into $315^o$, $45^o$, $135^o$, and $225^o$ phase shifts are displayed in Fig. 2-4. The parameters of the memristor used to plot Fig. 2-4 are selected as stated in Table 2-1. The memristor performance at 45º shifted versions will represent the core of the proposed Quadrature Phase Shift Keying (QPSK) demodulator investigated in section 3.3.

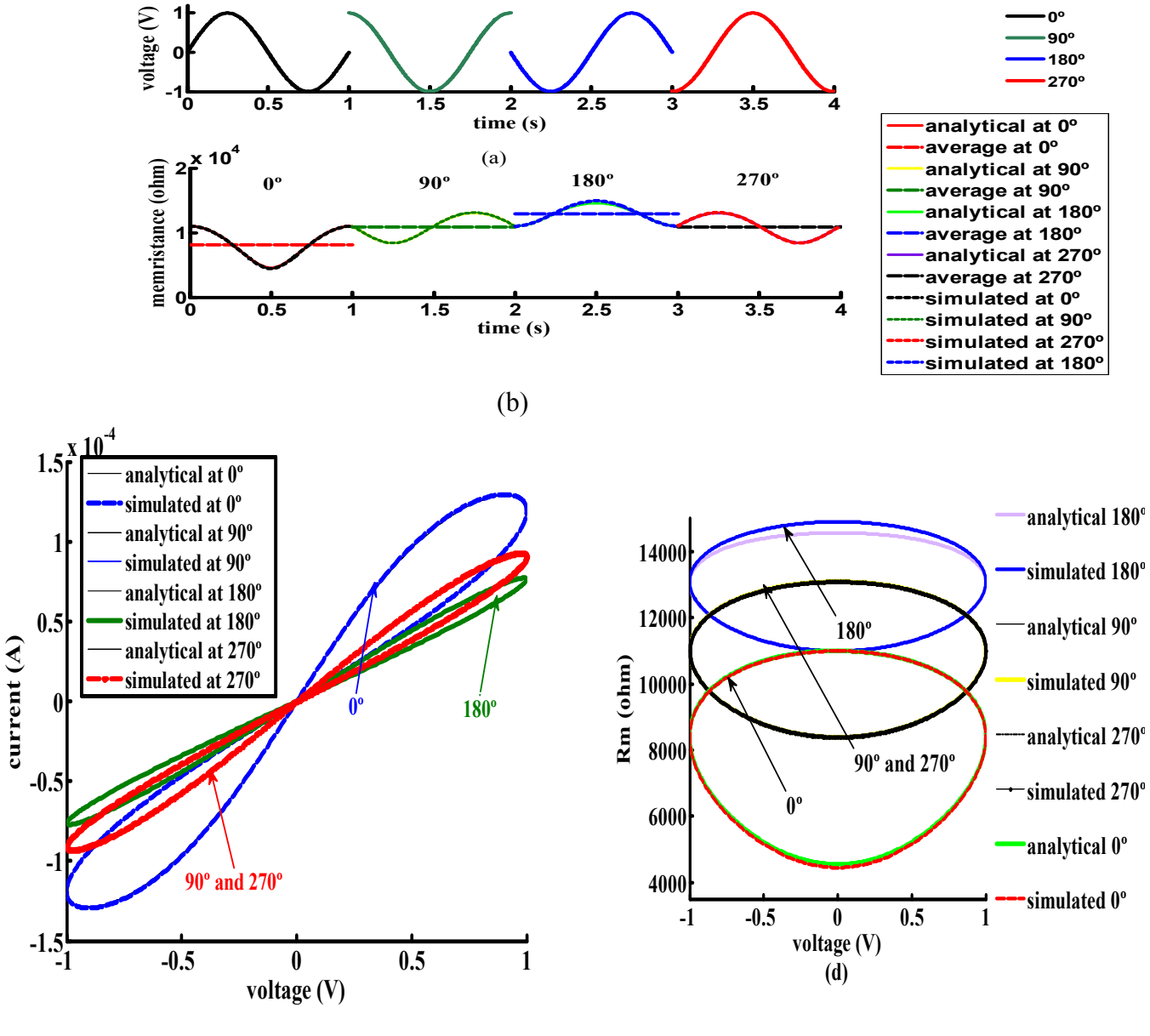



**Fig.2-3 (a). Sinusoid input voltage versus time for $0^0$ (0s-1s), $90^0$ (1s-2s), $180^0$ (2s-3s), and $270^0$ (3s-4s) phase shift using the linear dopant drift model.**
**(b). Simulated and Analytical memristor resistance versus time for shifted sinusoid input in case $0^0$ (0s-1s), $90^0$ (1s-2s), $180^0$ (2s-3s), and $270^0$ (3s-4s) phase shift.**
**(c). Simulated and Analytical memristor current versus voltage for $0^0$, $90^0$, $180^0$, and $270^0$ phase shift**
**(d). Simulated and Analytical memristor resistance versus voltage for $0^0$, $90^0$, $180^0$, and $270^0$ phase shift.**
**with 1v amplitude voltage and frequency of 1 Hz. (adapted from** [75].

### 2.2.2 Verification using more realistic model (Non-Linear Dopant Drift Model)

With the intention of verifying the results of the preceding subsection, a more realistic model is employed to consider all recognized memristor non-idealities. In this thesis, we applied the non-linear dopant drift model [26]. Non-idealities of realistically

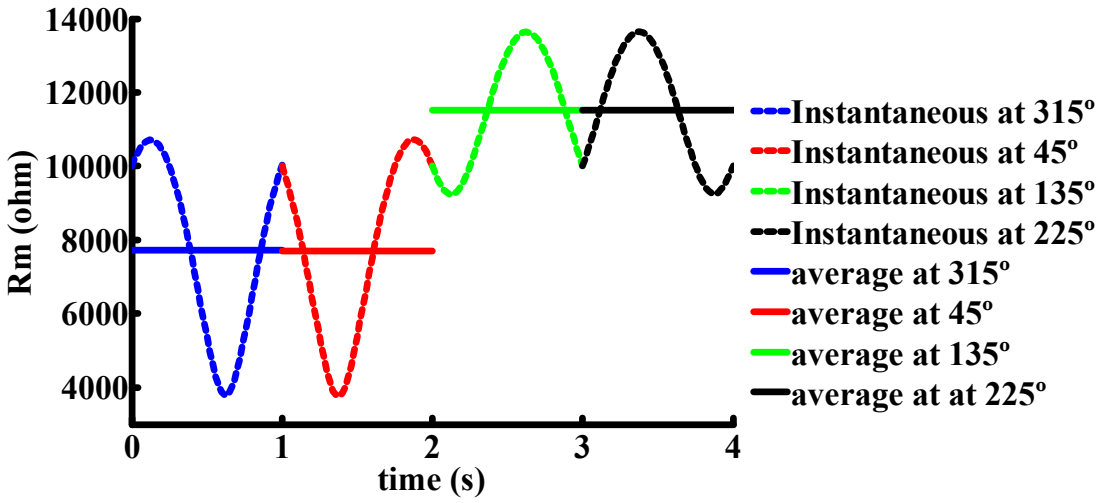



**Fig. 2-4. The instantaneous and average memristor resistance in case of following phases: 315°, 45°, 135°, and 225° using the linear dopant drift model ( adapted from** [77]**).**

fabricated memristors such as nonlinear memristance relationships (versus state and voltage), asymmetrical ON and OFF switching, and voltage thresholds are taken into account in this model [27]. The equation of the state change rate and the I-V relationship for the nonlinear model are exhibited in (2-6) and (2-7), respectively.

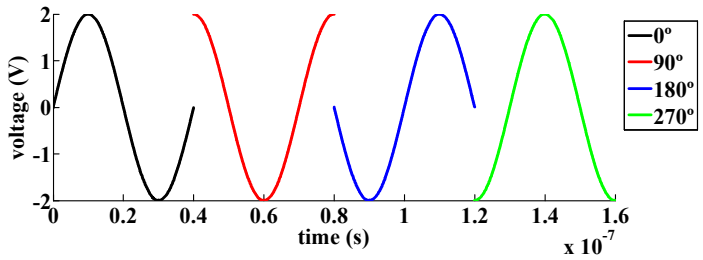
$$\frac{dw}{dt} = \begin{cases} a \cdot f(w) v(t)^m & |v(t)| > v_{th} \\ 0 & |v(t)| < v_{th} \end{cases}, \tag{2-6}$$

where $m$ is an odd integer constant , $a$ is a constant, and $f(w)$ is a window function [26].

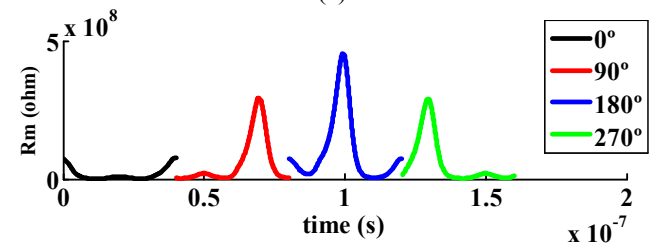
$$i(t) = (w(t))^n \cdot \beta \cdot sinh\big(\alpha v(t)\big) + \chi\big(exp\big(\gamma v(t)\big) - 1\big), \tag{2-7}$$

where $\chi$, $\beta, \gamma$ , and $\alpha$ are the fitting parameters for the experimental measurements. While $v_{th}$ is the threshold voltage, and $n$ is a constant to govern the dependence on the current state [26]. Through all simulations using the nonlinear model, the fitting parameter values are match the values used in [26] as long as other values are not explicitly mentioned. The model has been investigated and a Verilog-A version of it has been developed to be used in circuit simulations using Cadence. Moreover, the correction supposed in [34] and a capability of controllable initial state and threshold voltage have been added to the developed version. Accordingly, the developed Verilog-A model version is provided and listed in Appendix-A. Fig. 2-5 demonstrates the simulation outcomes adopting the nonlinear dopant drift model. In more detail, Fig. 2-5(a) illustrates the sinusoidal input waveform with distinct phase shift for each cycle. Fig. 2-5(b) demonstrates the unlike variation of the instantaneous memristance for unlike phase values. The unequal memristance averages ($Rm_{avg}$) for several initial phase values are shown in Fig. 2-5 (c). Moreover, Fig. 2-5 (d) illustrates the different slope I-V hysteresis loops for different phase values. Advantageously, the dependence on the initial phase can be satisfied regardless of linearity [75]. Additionally, the simulation results (using

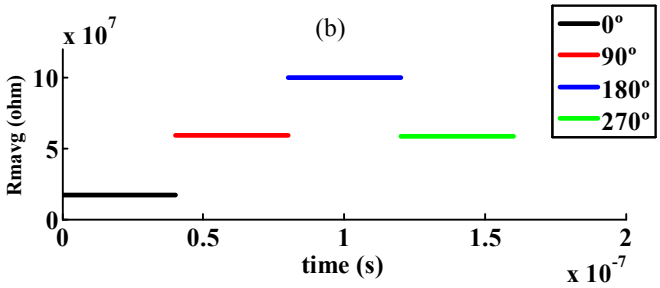
nonlinear dopant drift model) still confirm the validity of the proposed concept in spite of taking into consideration the basic nonlinear influences of the real devices [75].



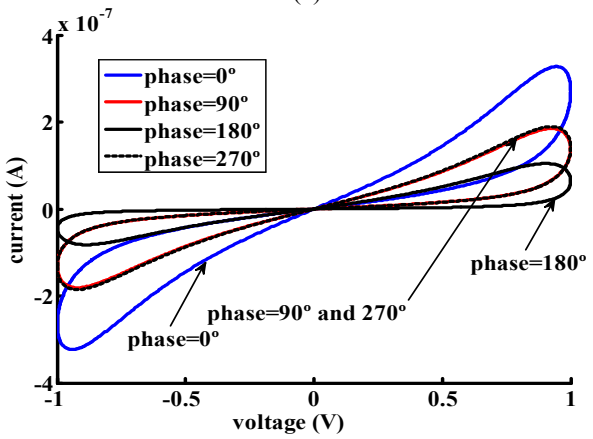

(a)




(b)




(c)




(d)

**Fig.2-5. Simulation results using nonlinear dopant drift model $a$ =1, $m$ =5, $n$=2, β = 0.9e-6, α = 2, χ =1e-10, γ =4, with 2V amplitude voltage, $v_{th}$=0.1 V, and frequency of 25 M Hz, using Biolek window function with $p$=10**
**(a). Sinusoid input voltage versus time for $0^0$ , $90^0$ , $180^0$ , and $270^0$ phase shift.**
**(b). The memristor resistance versus time for shifted sinusoid input in case $0^0$, $90^0$, $180^0$, and $270^0$ phase shift.**
**(c). Average of memristor resistance at the end of each cycle versus time for shifted sinusoid input in case $0^0$, $90^0$ , $180^0$, and $270^0$ phase shift.**
**(d). Memristor current versus voltage for $0^0$, $90^0$, $180^0$, and $270^0$ phase shift.**

## 2.3 Memristor response for square waveform input using the linear dopant drift model

The voltage as function of time for symmetrical shifted square waveform can be represented using (2-8) in the cases of an initial phase shift less and greater than 180°.

For $\theta_0 \leq 180^o$,

$$V(t) = \begin{cases} V_0 & 0 < t < \frac{\pi-\theta_0}{\omega_0} \\ -V_0 & \frac{\pi-\theta_0}{\omega_0} < t < \frac{2\pi-\theta_0}{\omega_0} \\ V_0 & \frac{2\pi-\theta_0}{\omega_0} < t < \frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}8a)$$

For $\theta_0 \geq 180^o$,

$$V(t) = \begin{cases} -V_0 & 0 < t < \frac{2\pi-\theta_0}{\omega_0} \\ V_0 & \frac{2\pi-\theta_0}{\omega_0} < t < \frac{3\pi-\theta_0}{\omega_0} \\ -V_0 & \frac{3\pi-\theta_0}{\omega_0} < t < \frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}8b)$$

$2V_0$ represents the peak to peak amplitude and $\omega_0$ represents the radial frequency [74]

Using (2-8) the flux, $\Phi(t) = \int_0^t v(t)dt$, for the square wave input voltage at any instant is

For $\theta_0 \leq 180^o$,

$$\Phi(t) = \begin{cases} V_0\, t & 0 < t < \frac{\pi-\theta_0}{\omega_0} \\ 2V_0\left(\frac{\pi-\theta_0}{\omega_0}\right) - V_0 t & \frac{\pi-\theta_0}{\omega_0} < t < \frac{2\pi-\theta_0}{\omega_0} \\ \frac{-2\pi V_0}{\omega_0} + V_0 t & \frac{2\pi-\theta_0}{\omega_0} < t < \frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}9a)$$

For $\theta_0 \geq 180^o$,

$$\Phi(t) = \begin{cases} -V_0\, t & 0 < t < \frac{2\pi-\theta_0}{\omega_0} \\ -2V_0\left(\frac{2\pi-\theta_0}{\omega_0}\right) + V_0 t & \frac{2\pi-\theta_0}{\omega_0} < t < \frac{3\pi-\theta_0}{\omega_0} \\ \frac{2\pi V_0}{\omega_0} - V_0 t & \frac{3\pi-\theta_0}{\omega_0} < t < \frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}9b)$$

The flux dependence on the initial phase is noticeable in (2-9) so from (1-6) and (2-9) the memristance $R_m(t)$ at any time during the cycle is [74].

For $\theta_0 \leq 180^o$,

$$R_m^2(t)=\begin{cases} R_{init}^2-2kR_d(Vo\,t) & 0<t<\frac{\pi-\theta_0}{\omega_0} \\ R_{init}^2-2kR_d(2Vo\left(\frac{\pi-\theta_0}{\omega_0}\right)-V_0t) & \frac{\pi-\theta_0}{\omega_0}<t<\frac{2\pi-\theta_0}{\omega_0} \\ R_{init}^2-2kR_d(\frac{-2\pi V_0}{\omega_0}+Vot) & \frac{2\pi-\theta_0}{\omega_0}<t<\frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}10a)$$

For $\theta_0 \geq 180^o$,

$$R_m^2(t)=\begin{cases} R_{init}^2-2kR_d(-Vo\,t) & 0<t<\frac{2\pi-\theta_0}{\omega_0} \\ R_{init}^2-2kR_d\left(-2Vo\left(\frac{2\pi-\theta_0}{\omega_0}\right)+V_0t\right) & \frac{2\pi-\theta_0}{\omega_0}<t<\frac{3\pi-\theta_0}{\omega_0} \\ R_{init}^2-2kR_d\left(\frac{2\pi V_0}{\omega_0}-Vot\right) & \frac{3\pi-\theta_0}{\omega_0}<t<\frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}10b)$$

and $R_m \in (R_{on}, R_{off})$. It is observable from (2-10) that the memristor resistance, in case of a periodic square signal input, is also phase reliant. In addition, the analytical resistance values are repeated in each cycle because of the symmetry, also $R_m$ comes back to $R_{init}$ again at the ending of each cycle. The returning of $R_m$ to $R_{init}$ at the end of every cycle is for the reason that the flux at these moments, for the zero net-area waveform, is zero for any phase shift [38]. Fig. 2-6 (a) illustrates four different phase shift square input waveforms while Fig. 2-6 (b) illustrates the memristor instantaneous resistance for $0^o$, $90^o$, $180^o$, and $270^o$ phase shifts, using (2-10). Also, Fig. 2-6 (b) demonstrates the average value of the memristance over the cycle time. It can be noticed from Fig. 2-6 (b) that for symmetrical square input waveform, the average of memristor resistance is greater than $R_{init}$ in case of $180^o$ phase shift, is smaller than $R_{init}$ in case of $0^o$ phase shift, and equals to $R_{init}$ in case of $270^o$ and $90^o$ phase shift [74]. The same as the case of the sinusoidal input excitation, the reaction of the memristance for different phase shifts square input excitation gives memristances of different average for phase shifts $180^o$ and $0^o$ and equal ones for $270^o$ and $90^o$.

In Fig. 2-6 (c), the pinched hysteric I-V characteristics of the memristor are shown after simulation, using the linear dopant drift model [32] for $0^o$, $90^o$, $180^o$, and $270^o$ initial phase shifts [74]. Fig. 2-7 (a) and Fig. 2-7 (b) show simulated memristance using Matlab model [35] for four values, $0^o$, $90^o$, $180^o$, and $270^o$, of phase shifts in case of (p=10) and (p=1) respectively. While, Fig. 2-8 (a) and Fig. 2-8 (b) show simulated memristance using *SPICE* model [32] for four values, $0^o$, $90^o$, $180^o$, and $270^o$, of phase shifts in case of (p=10) and (p=1) respectively. The max error between the simulated and analytical memristance for $0^o$, $90^o$, $180^o$, and $270^o$ phase shifts is averaged and listed in Table 2-2 for the cases of Matlab (p=10), Matlab (p=1), SPICE (p=10), and SPICE (p=1). It is clear that, for $p$=10 the error between the calculated and simulation results is smaller than that for $p$=1. Since the nonlinearity degree for p=10 is less than it for p=1. It is worth mentioned that, both Matlab and the SPICE models use the linear dopant drift model with Joglekar window multiplied by (1-3) while the ideal linear dopant drift model considering f(x) = 1 was used through the analytical analysis. However, SPICE simulation environment uses implicit integration methods, Newton's method, and sparse matrix techniques to solve the differential equations implicit in the memristor models but in Matlab simulations, the Runge-Kutta method is used to solve the memristor model differential equations.

The memristor parameters used in this section are chosen equal to those used in [38] (i.e. $R_{on}$=100Ω, $R_{off}$=16kΩ, $R_{init}$=11kΩ, $D$=10nm, $\mu_v$=10fm$^2$s$^{-1}$v$^{-1}$). The input periodic square has been assumed to have frequency of 1 Hz and 0.5v amplitude voltage.

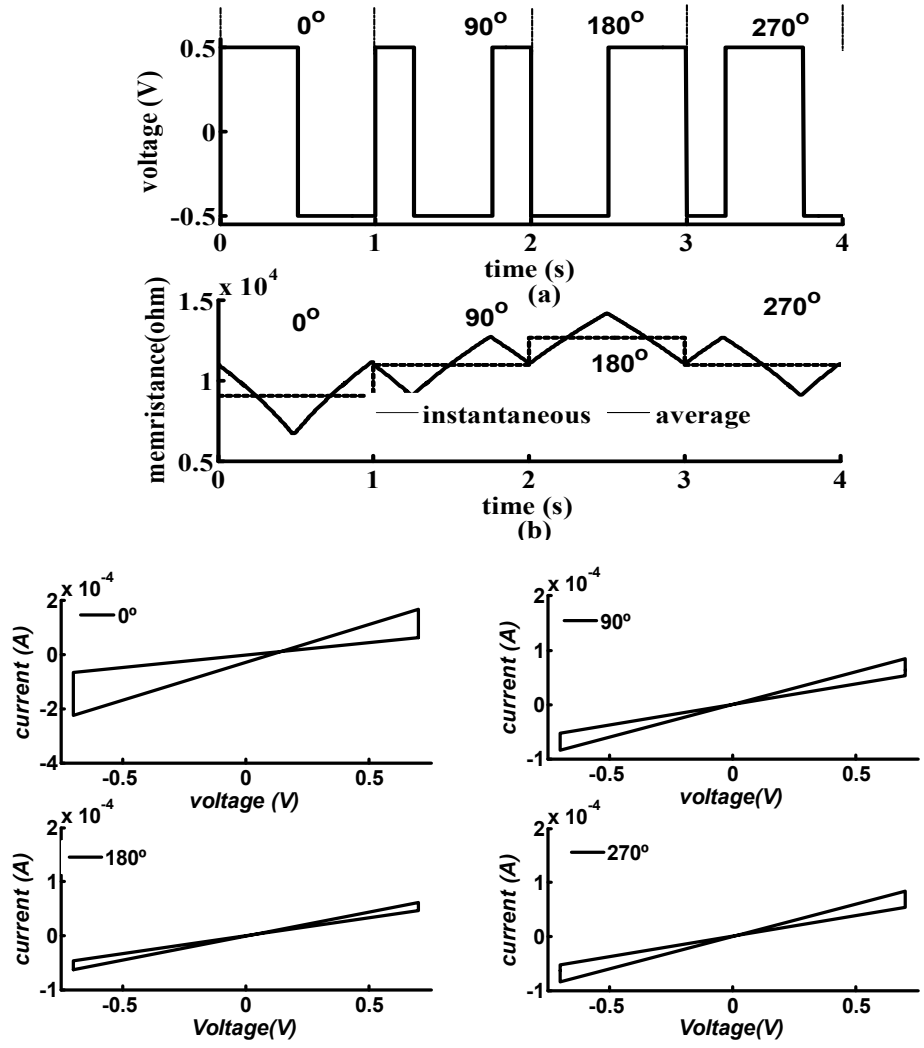



**Fig. 2-6 (a). Square input voltage versus time for 0$^o$ (0s-1s), 90$^o$ (1s-2s), 180$^o$ (2s-3s), and 270$^o$ (3s-4s) phase shift. (b). Mermistor resistance versus time for the shifted square input shown in (a). (c). Memristor current versus voltage for 0$^o$, 90$^o$, 180$^o$, and 270$^o$ shifted square input.**

**Table 2.2 The average max error between the simulated and analytical memristance for the 0$^o$, 90$^o$, 180$^o$ , and phase shifted square signal.**

| Average max error | Matlab | SPICE |
|---|---|---|
| P=1 | 4.5% | 3.9% |
| P=10 | 1.9% | 0.6% |

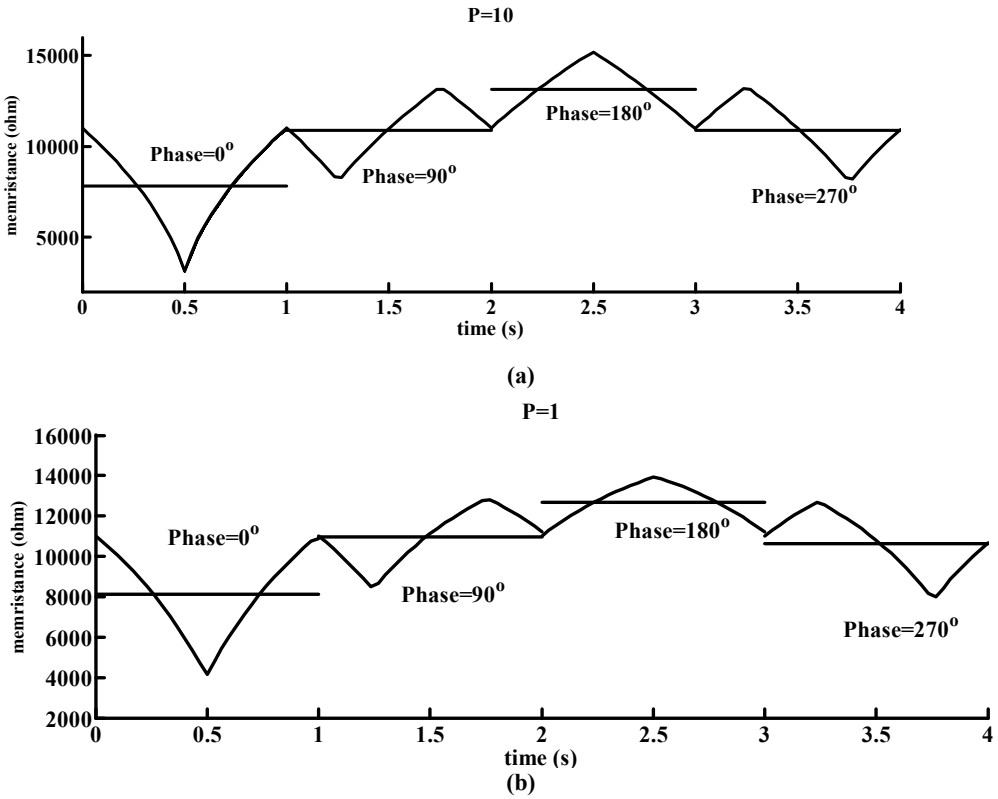



**Fig. 2-7. (a). Matlab simulated (p=10) memristance versus time for 0°, 90°, 180° , and 270° phase shift square input. (b). Matlab simulated (p=1) memristance versus time for 0°, 90°, 180° , and 270° phase shift square input.**

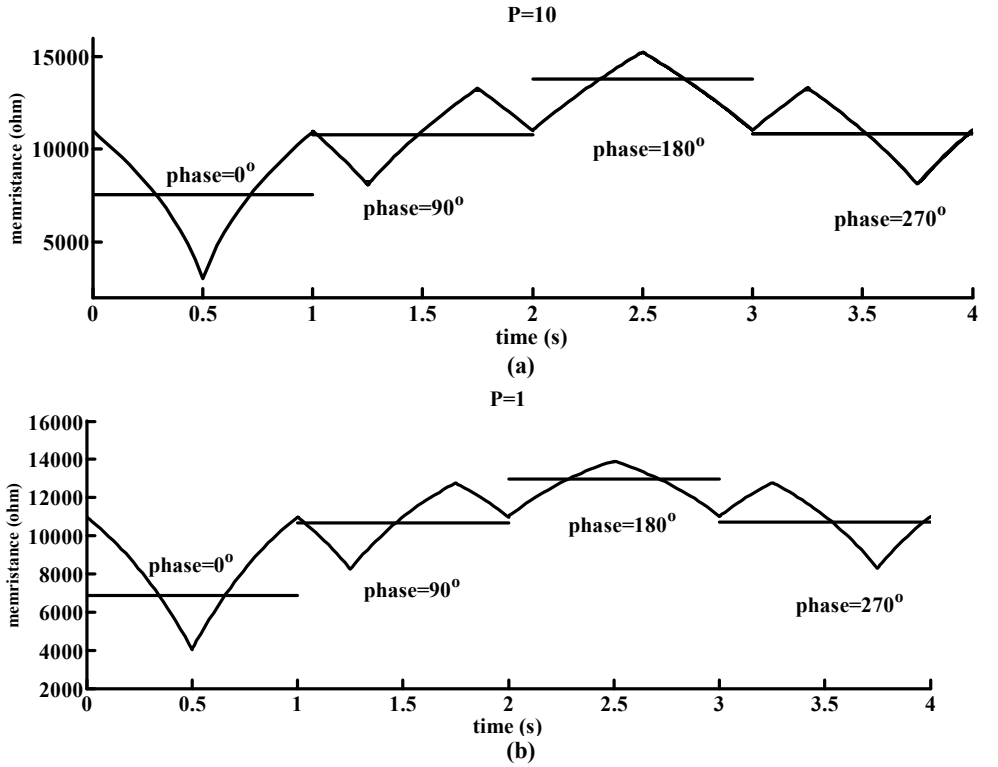



**Fig. 2-8. (a). SPICE simulated (p=10) memristance versus time for 0°, 90°, 180° , and 270° phase shift square input. (b). SPICE simulated (p=1) memristance versus time for 0°, 90°, 180° , and 270° phase shift square input.**

## 2.4 Memristor response for Triangle waveform input using the linear dopant drift models

The voltage with respect to time, for shifted symmetrical triangle waveform input, can be expressed using (2-11) for initial phase shift greater and less than $180^o$ [74].

For $\theta_0 \leq 180^o$

$$V(t) = \begin{cases} \frac{4V_0}{T}\left(t + \frac{\theta_0}{\omega_0}\right) - Vo & 0 \leq t \leq \frac{\pi - \theta_0}{\omega_0} \\ \frac{-4V_0}{T}\left(t + \frac{\theta_0}{\omega_0}\right) + 3Vo & \frac{\pi - \theta_0}{\omega_0} \leq t \leq \frac{2\pi - \theta_0}{\omega_0} \\ \frac{4V_0}{T}\left(t + \frac{\theta_0}{\omega_0}\right) - 5Vo & \frac{2\pi - \theta_0}{\omega_0} \leq t \leq \frac{2\pi}{\omega_0} \end{cases} \quad (2-11a)$$

For $\theta_0 \geq 180^0$

$$V(t) = \begin{cases} \frac{-4V_0}{T}\left(t + \frac{\theta_0}{\omega_0}\right) + 3Vo & 0 \leq t \leq \frac{2\pi - \theta_0}{\omega_0} \\ \frac{4V_0}{T}\left(t + \frac{\theta_0}{\omega_0}\right) - 5Vo & \frac{2\pi - \theta_0}{\omega_0} \leq t \leq \frac{3\pi - \theta_0}{\omega_0} \\ \frac{-4V_0}{T}\left(t + \frac{\theta_0}{\omega_0}\right) + 7Vo & \frac{3\pi - \theta_0}{\omega_0} \leq t \leq \frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}11b)$$

$\omega_0$ is radial frequency of the triangular signal and $2V_0$ is the peak to peak amplitude. At any instant during the cycle time, $\Phi(t) = \int_0^t v(t)dt$, is equal to the time integration of the applied memristor voltage, as illustrated by (2-13) [74].

For $\theta_0 \leq 180^o$,

$$\Phi(t) = \begin{cases} \frac{2Vo}{T}t^2 + \left(\frac{4V_0\theta_0}{T\omega_0} - V_0\right)t & 0 < t < \frac{\pi - \theta_0}{\omega_0} \\ \frac{-2Vo}{T}t^2 + \left(\frac{-4V_0\theta_0}{T\omega_0} + 3V_0\right)t + \frac{4V_0}{\omega_0}\left(\frac{\pi^2 - {\theta_0}^2}{T\omega_0} + \theta_0 - \pi\right) & \frac{\pi - \theta_0}{\omega_0} < t < \frac{2\pi - \theta_0}{\omega_0} \\ \frac{2Vo}{T}t^2 + \left(\frac{4V_0\theta_0}{T\omega_0} - 5V_0\right)t - \frac{12V_0\pi^2}{T{\omega_0}^2} - \frac{4V_0}{\omega_0}(\theta_0 - 3\pi) & \frac{2\pi - \theta_0}{\omega_0} < t < \frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}12a)$$

For $\theta_0 \geq 180^o$,

$$\Phi(t) = \begin{cases} \frac{-2Vo}{T}t^2 + \left(\frac{-4V_0\theta_0}{T\omega_0} + 3V_0\right)t & 0 < t < \frac{2\pi - \theta_0}{\omega_0} \\ \frac{2Vo}{T}t^2 + \left(\frac{4V_0\theta_0}{T\omega_0} - 5V_0\right)t - \frac{4V_0}{\omega_0}\left(\frac{4\pi^2 - {\theta_0}^2}{T\omega_0} + 2\theta_0 - 4\pi\right) & \frac{2\pi - \theta_0}{\omega_0} < t < \frac{3\pi - \theta_0}{\omega_0} \\ \frac{-2Vo}{T}t^2 + \left(\frac{-4V_0\theta_0}{T\omega_0} + 7V_0\right)t + \frac{20V_0\pi^2}{T{\omega_0}^2} + \frac{4V_0}{\omega_0}(\theta_0 - 5\pi) & \frac{3\pi - \theta_0}{\omega_0} < t < \frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}12b)$$

In the same way as the memristor resistance in cases of the sinusoidal and square excitations, from (1-6) and (2-12) the instantaneous memristor resistance is phase

dependent in case of symmetrical triangle input waveform too.
The memristor resistance is evaluated using (1-6) and (2-12) and its instantaneous equation is given by (2-13).

For $\theta_0 \leq 180^o$

$$R_m^2(t) = R_{init}^2 + \begin{cases} -2kR_dVo\left(\frac{2t^2}{T} + \left(\frac{4\theta_0}{T\omega_0} - 1\right)t\right) & 0 < t < \frac{\pi-\theta_0}{\omega_0} \\ 2kR_d\ Vo\left(\frac{2t^2}{T} + \left(\frac{4\theta_0}{T\omega_0} - 3\right)t - \frac{4}{\omega_0}\left(\frac{\pi^2-{\theta_0}^2}{T\omega_0} + \theta_0 - \pi\right)\right) & \frac{\pi-\theta_0}{\omega_0} < t < \frac{2\pi-\theta_0}{\omega_0} \\ -2kR_dVo\left(\frac{2t^2}{T} + \left(\frac{4\theta_0}{T\omega_0} - 5\right)t - \frac{12\pi^2}{T{\omega_0}^2} - \frac{4}{\omega_0}(\theta_0 - 3\pi)\right) & \frac{2\pi-\theta_0}{\omega_0} < t < \frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}13a)$$

For $\theta_0 \geq 180^o$

$$R_m^2(t) = R_{init}^2 - \begin{cases} 2kR_dVo\left(\frac{-2t^2}{T} + \left(\frac{-4\theta_0}{T\omega_0} + 3\right)t\right) & 0 < t < \frac{2\pi-\theta_0}{\omega_0} \\ 2kR_dVo\left(\frac{2t^2}{T} + \left(\frac{4\theta_0}{T\omega_0} - 5\right)t - 4\left(\frac{4\pi^2-{\theta_0}^2}{T{\omega_0}^2} + \frac{2\theta_0-4\pi}{\omega_0}\right)\right) & \frac{2\pi-\theta_0}{\omega_0} < t < \frac{3\pi-\theta_0}{\omega_0} \\ 2kR_dVo\left(\frac{-2t^2}{T} + \left(\frac{-4\theta_0}{T\omega_0} + 7\right)t + \frac{20\pi^2}{T{\omega_0}^2} + \frac{4}{\omega_0}(\theta_0 - 5\pi)\right) & \frac{3\pi-\theta_0}{\omega_0} < t < \frac{2\pi}{\omega_0} \end{cases} \quad (2\text{-}13b)$$

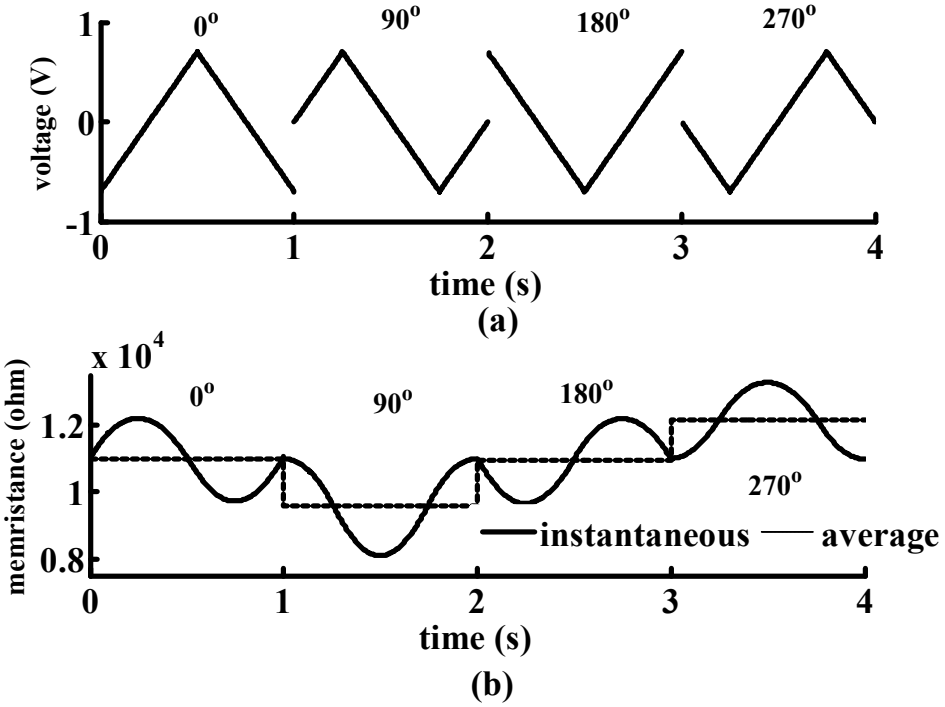
Obviously it can be noted from (2-13), that the instantaneous memristance and consequently its average throughout the cycle of applied signal is reliant on the initial phase of the triangle signal. Also $R_m$ returns to $R_{init}$ again at the cycle end as, at this moment, the flux for the zero net-area waveform is zero for any initial phase providing that the saturation threshold is not achieved [35], [38], [74]. Fig. 2-9(a) and 2-9(b) display the triangular waveforms input and the instantaneous resistance of the memristor according to each phase shift respectively.

In Fig. 2-9(c), the I-V characteristic curves are plotted for initial phase shifts of $180^o$, $90^o$, $0^o$, and $270^o$ [74].

Fig. 2-10 (a) and Fig. 2-10 (b) show simulated memristance using Matlab model [35] for four values, $0^o$, $90^o$, $180^o$, and $270^o$, of phase shifts in case of (p=10) and (p=1) respectively. While, Fig. 2-11 (a) and Fig. 2-11 (b) show simulated memristance using SPICE model [32] for four values, $0^o$, $90^o$, $180^o$, and $270^o$, of phase shifts in case of (p=10) and (p=1) respectively. The max error between the simulated and analytical memristance for $0^o$, $90^o$, $180^o$, and $270^o$ phase shifts is averaged and listed in Table 2-3 for the cases of Matlab (p=10), Matlab (p=1), SPICE (p=10), and SPICE (p=1). From Table 2-3 it is obvious that, the error between the calculated and simulation results in case of $p$=10 is smaller than that for $p$=1. Since the nonlinearity degree for $p$=10 is less than it for $p$=1.

**Table 2.3 The average max error between the simulated and analytical memristance for the $0^o$, $90^o$, $180^o$ , and phase shifted triangle signal.**

| Average max error | Matlab | SPICE |
|---|---|---|
| P=1 | 2.5% | 2.3% |
| P=10 | 0.18% | 0.16% |



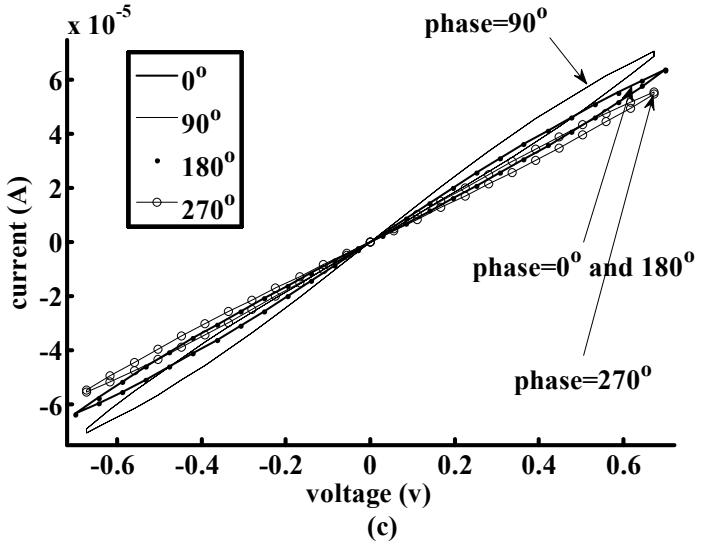




**Fig. 2-9 (a). Triangle input voltage versus time for $0^o$ (0s-1s), $90^o$ (1s-2s), $180^o$ (2s-3s), and $270^o$ (3s-4s) phase shift. (b). The mermistor resistance versus time for the applied triangle input with different phase shifts. (c). Memristor current versus voltage for $0^o$, $90^o$, $180^o$, and $270^o$ shifted triangle input. The signal has been assumed to have 0.7v amplitude voltage and frequency of 1 Hz (adapted from** [74]**).**

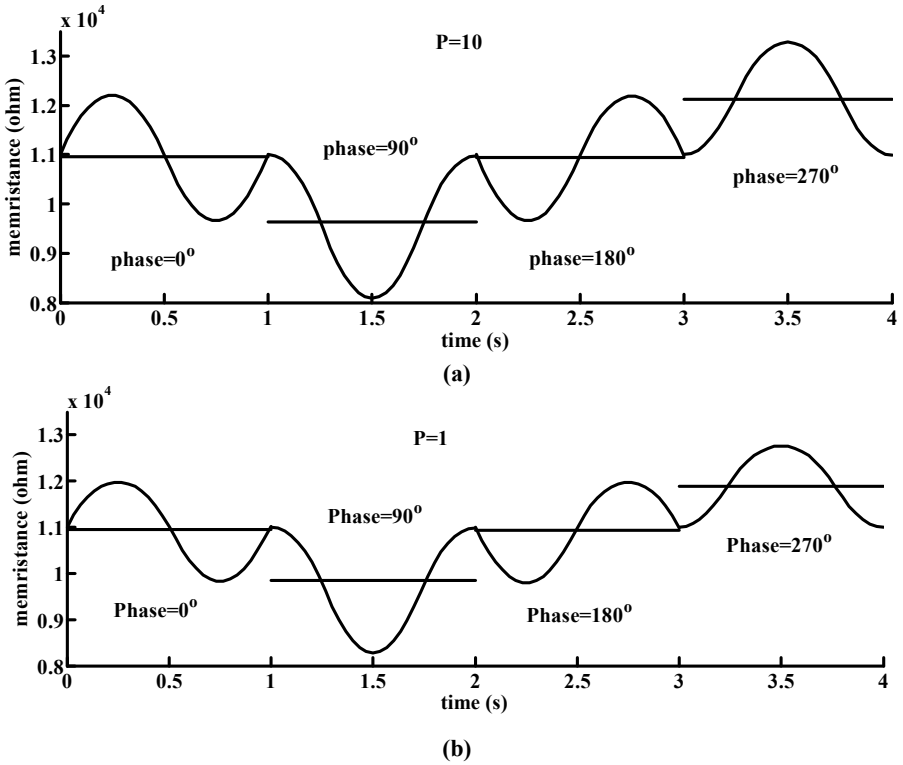



**Fig. 2-10. (a). Matlab simulated (p=10) memristance versus time for 0°, 90°, 180° , and 270° phase shift square input. (b). Matlab simulated (p=1) memristance versus time for 0°, 90°, 180° , and 270° phase shift triangle input (the signal parameters are same as the used in Fig. 2-9(a)).**

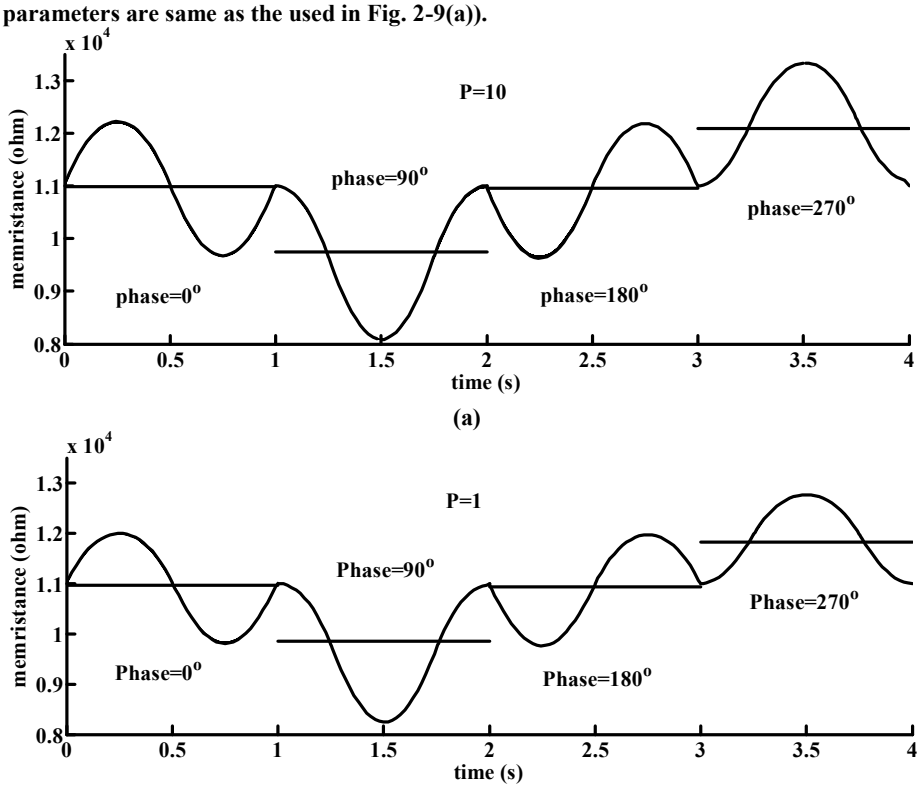



**Fig. 2-11. (a). SPICE simulated (p=10) memristance versus time for 0°, 90°, 180° , and 270° phase shift square input. (b). SPICE simulated (p=1) memristance versus time for 0°, 90°, 180° , and 270° phase shift triangle input (the signal parameters are same as the used in Fig. 2-9(a)).**

# Chapter Three

# MEMRISTOR BASED DIGITAL DEMODULATORS WITH NONLINEAR DOPANT DRIFT MODEL

## *3.1 The memristor based communication applications*

The memristor has a set of appealing attributes such as, nonlinearity features, high scalability, and non-volatility, beside manufacturability and electrical compatibility with the traditional CMOS technology. These attributes support the emergence of plentiful memristors applications both in new structured and traditional circuits.

Some of the features of memristive systems using memristor as nonlinear resistor for spectrum enhancing (frequency multipliers, modulators, mixers, etc.) are proposed in [25]. Several attempts for exploiting the memristor features profits in communication applications have been recently reported like the receiver for ultra-wide band signals [66] and the memristor-based modulators [25], [67], [68], [78], [79]. An Amplitude Modulation (AM) circuit based on the linear dopant drift model is suggested in [68]. Moreover, Frequency Shift Keying (FSK), Amplitude Modulation (AM), and Binary Phase Shift Keying (BPSK), and Amplitude Shift Keying (ASK) modulators have been proposed in [67]. A new emulator circuit for the memristor element has been experimentally investigated in [78] and used in setting new designs for FSK, ASK, and Phase Shift Keying (PSK) modulators.

Moreover, the memory and switching features of the memristor devices have been utilized, using memristor-based random modulators, in designing a new structural design of a compressive sensing system [79]. Lastly, an architecture for a memristor-based stored reference receiver has been introduced, where the operation was performed by calculating the correlation between the template waveform and a received signal [66].

Nevertheless, till now, a little effort was dedicated to the introduction of nonlinear memristive circuits in communication systems particularly for demodulators and detectors. Besides, in all aforementioned efforts, the linear dopant drift model has been adopted. Despite the fact that this model incorporates ideal memristor physical relations, it diverges considerably from the behavior of the described fabricated memristive devices [27].

Furthermore, many researchers reported their designs at very low frequency (1-100Hz) missing power evaluation. Hence, it is difficult to guess their actual behavior in the high frequency domain. On the other hand, during the past decades, research has progressed on the biomedical implantable electronic devices that require power and data communication through wireless inductive links [80]. Therefore, in this chapter, we present a set of novel memristor-based demodulators at 25MHz carrier frequency. The proposed demodulators are dedicated to implantable medical devices with wireless

inductive links. The proposed demodulators feature small integration area, low power consumption, and easy implementation.

In this work, the change of the average memristance with the phase shift of the input signal, a property developed in Chapter 2 and plotted in Fig. 2-5(c), is used to discriminate between different phases. Consequently, a straightforward phase detector can be implemented using a memristor-based circuit. Using this simple concept, a full demodulator can be built to demodulate BPSK modulated signals, as the data is represented by the phase of the carrier signal. The ***nonlinear*** dopant drift model is used to consider the non-ideal features of practically manufactured memristors. In the simple structured proposed circuits, there is no need for additional synchronization circuits, this makes them promising from the power consumption and area viewpoints. Additionally, this circuit will be expanded, later, to QPSK and QAM modulation schemes. A memristor based BFSK (Binary Frequency Shift Keying) demodulator is also reported by us, in this time the change of the average memristance with the frequency, instead of the phase, of the applying signal is used. The schematic, the operation, and the simulation results of the aforementioned demodulators are demonstrated in details in the following sections.

## *3.2 Memristor-based BPSK demodulator*

The BPSK is the simplest technique of the PSK (Phase Shift Keying), is a digital modulation scheme that expresses data by modifying the phase of the carrier signal. BPSK uses two distinct phases which are detached by 180° to represent '0' and '1'. It is proper for cheap passive transmitters and it has the highest immunity against corruption. Additionally, it is adopted by several wireless communications standards such as Bluetooth communication wireless, Radio-Frequency Identification (RFID), and Local Area Networks (LANs) [81].

Fig. 3-1 (a) and Fig. 3-1 (b) introduce, respectively, the block diagram and the schematic of the suggested BPSK demodulator circuit. At first, the BPSK demodulated signal is applied to a voltage divider. The voltage divider is between a resistor and a memristor element (as clear in Fig. 3-1 (b)). The voltage divider output is given by (3-1).

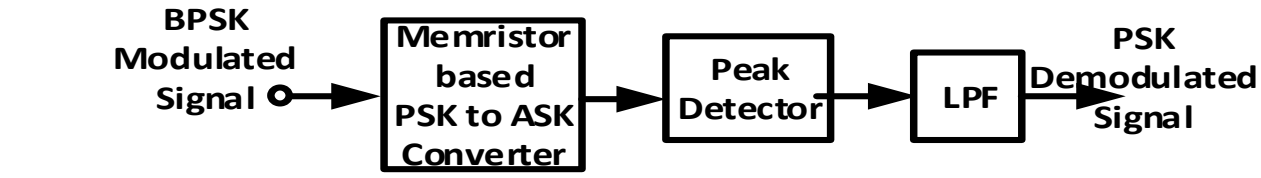
$$V_1 = V_{in} R_1/(R_1 + \mathrm{R_m}) \qquad (3-1)$$

As demonstrated in Chapter 2, the change of the average memristance of the memristor element $R_m$ is a direct function of the input signal phase. As $R_m$ alters with the input signal phase, the amplitude of $V_1$will change with the phase too. Thereby, this voltage divider transforms the change in the ***phase*** of the sinusoidal input into the change in the ***amplitude*** of the sinusoidal output, producing a memristor-based PSK to ASK converter. The peak detector block, cascading PSK to ASK converter in Fig. 3-1 (a), generates a DC voltage proportional to the amplitude of the ASK signal. This peak detector consists of a diode ($D$) followed by a parallel connection between a resistor ($R_2$) and a capacitor ($c_1$) as seen in Fig. 3-1 (b). The resistor $R_2$ provides a discharge path to regularly reset the output of the peak detector at the commencing of each bit, obviating the need for resetting circuit. By this way, the circuit produces one of two output levels relying on the phase of the input signal [75]. It is worth pointing out that, the same concept is applied in

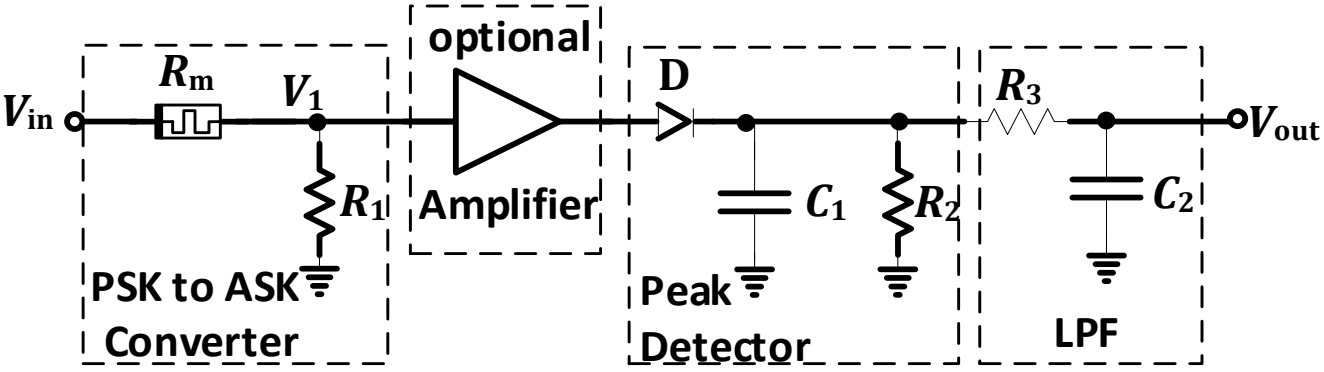
case of the modulated parameter is the frequency rather than the phase. As originally, it was demonstrated in [3] and shown in Fig. 2-2, the average memristance varies with the frequency of operation. As a result, this voltage divider can also be employed to transfer from variation in the frequency (not only the phase) of the sinusoidal input waveform to variation in the amplitude of sinusoidal output, generating a PSK to ASK or FSK to ASK converter in accordance with the modulation scheme. Thus, same structure can also be used to build a set of frequency shift keying demodulators as will be illustrated in details in section 3.4.

The dissipated power through the discharging path can be evaluated as the difference between the stored energy in the capacitor during high and low levels divided by the time of the discharging, i.e., $0.5\,C_1(V_h^2 - V_l^2)/t_d$, where $V_h$ is the voltage of the capacitor during bit '1' while $V_l$ is the voltage of the capacitor during bit '0' and $t_d$ is the time of the discharging. The only needed external circuit is a circuit for memristance initialization as introduced in [82], [83].

The suggested circuit gets rid of the need to any carrier recovery circuits, decreasing the associated overhead in other usual BPSK demodulators [84], that makes it proper to ultra-low power applications. Furthermore, the lower power, small size, and simple structure features make the designed demodulator more appropriate for the use in a single integrated chip design for an implantable wireless neural recording system[85].




(a)




**(b)**

**Fig. 3-1 (a). Block diagram of the suggested BPSK demodulator (adopted from** [75]**).**

**(b). Schematic of the suggested BPSK demodulator (adopted from** [75]**).**

### *3.2.1 Functionality of the proposed circuit*

Typically, bit '0' in BPSK is expressed by some sinusoidal cycles along with $180^o$ phase shift but bit '1' is represented by some cycles of $0^o$ phase shift sinusoidal signal. Accordingly and based on the results of Chapter 2, the consequent memristance for bit '0' is high for the duration of the bit time (as has been illustrated in Fig. 2-5(c)). Hence, the voltage drop across $R_1$, $V_1$ in Fig. 3-1(b), at this time is relatively small sinusoidal peak to peak amplitude. Thus the peak detector output is low denoting to logic '0' voltage level. Conversely, the case of a bit '1', when receiving sinusoidal waveforms with $0^o$ phase shift, the $R_m$ average is small (as clear in Fig. 2-5 (c)). Therefore, $V_1$ , the voltage drop across $R_1$ in Fig. 3-1(b) , is sinusoidal signal with reasonably large amplitude and the peak detector output is high pointing to the voltage level of the logic '1'.

Consequently, the suggested BPSK demodulator circuit shown in Fig. 3-1(b) begins with the resistor-memristor voltage divider. It converts the current of different magnitudes, proportional to different phases of the received signal, by using the series resistance ($R_1$), into different voltage amplitudes as illustrated above. Second, an arbitrary amplifier can be needed for magnifying the output of the voltage divider to overtake the forward voltage of the diode. The amplifier can be eliminated provided that the voltage level of the divider output is sufficiently high. Next, a simple and passive peak detector is used for identifying the signal peak. Then, a first order low pass filter (LPF) at the final stage is required for eliminating the ripples at the output.

Notwithstanding the fact that, this circuit introduces a very plain BPSK demodulator and requires neither carrier recovery circuits nor expensive hardware, but the selection of the values of $R_2$ and $c_1$ must be precisely carried out. The values should satisfy that the transition time (which is the necessary time needed by the peak detector for switching between the different levels) is enough smaller than the bit duration and also larger than the carrier period. These conditions are concluded in (3-2).

$$T_c \ll \tau \ll T_b, \qquad (3-2)$$

$\tau$ is the capacitor discharging time constant, $\tau = R_2 C_1$ . Whereas $T_b$ and $T_c$ are the bit duration and the carrier period respectively. From the above analysis and knowing that the maximum allowable carrier frequency is limited by the the advancement in memristor technologies, the ratio between the data rate and the carrier frequency is restricted by (3-2). Assuming that $\frac{T_b}{T_c} = 50$ is enough for satisfying (3-2) condition, so the maximum bit rate is limited at carrier frequency/50. On the other side the amplitude of the input modulated signal for all the proposed demodulators is restricted by the saturation and the threshold amplitude limits of the used memristor. Therefore, the modulated signal amplitude should be larger than the threshold voltage and less than the saturation voltage. Similarly, same restrictions constrain further proposed demodulators.

### *3.2.2 Circuit simulations*

Due to the restricted ability of having experimental measurements using physically

available memristors, many researchers depend on the behavioral and SPICE models of the HP memristor to prove the validity of their developed concepts. Furthermore, as shown in Chapter 1, the majority of the published memristor based applications in literature are accomplished with the simple memristor model, viz., the linear dopant drift model [32]. However, recent memristors reveal much more complex behavior. Subsequently, the influence of the practical devices non-idealities on the function of the proposed circuits should be examined. Accordingly, in this thesis a more realistic memristor model (nonlinear dopant drift model) is utilized in all simulations of the suggested circuits. The nonlinear model is established on fitting actual measured data integrating the most known nonlinear effects [26]. Memristor's parameters used in simulations using the non linear dopant drift model for all the proposed demodulated are same as in [26]. The circuit parameter values used in BPSK simulations are listed in Table 3-1.

**Table 3-1. The parameter values for the proposed BPSK demodulator.**

| Parameter | value |
|---|---|
| $R_1$ | 1kΩ |
| $C_1$ | 10nF |
| $R_2$ | 50Ω |
| $C_2$ | 1nF |
| $R_3$ | 50Ω |
| $V_{in}$ | 2V |
| $f_c$ (carrier frequency) | 25MHz |
| $T_b$ | 1.92μsec |

Fig. 3-2 displays the results of the transient simulation for the proposed circuit shown in Fig. 3-1 (b). The modulating data used in the simulation, drawn in Fig. 3-2 (a), are assumed to be a train of '1' and '0' alternatively. Fig. 3-2 (b) shows the BPSK modulated signal that is the input for the suggested demodulator circuit. In the assumed input two distinctive phases can be visibly observed at the multipliers of the bit time. After that, Fig. 3-2 (c) illustrates the voltage drop across $R_1$ (the signal amplitude is small in case of bit '0' and large in case of bit '1').

The peak detector output as soon as being smoothed by the first order LPF stands for the output of the suggested BPSK demodulator circuit and is identified in Fig. 3-2 (d). It is obvious that the circuit simulated output, shown in Fig. 3-2 (d), ultimately analogous to the data in Fig. 3-2 (a) which confirms the validity of the proposed scheme. In order to evaluate the sensitivity of the output for the input phase error, simulations have been performed. It resulted into a maximum error percentage equals 1.5% for a $5^o$ phase error for both of the voltage levels, while still having a reliable output. The simulation results of the proposed BPSK demodulator show a data transmission rate of 0.5 Mbps, less than 0.37 mW consumption under a supply voltage of 3.3 V, and an estimated silicon area of 0.01 $mm^2$ in the United Microelectronics Corporation (UMC) CMOS 0.13- μm technology.

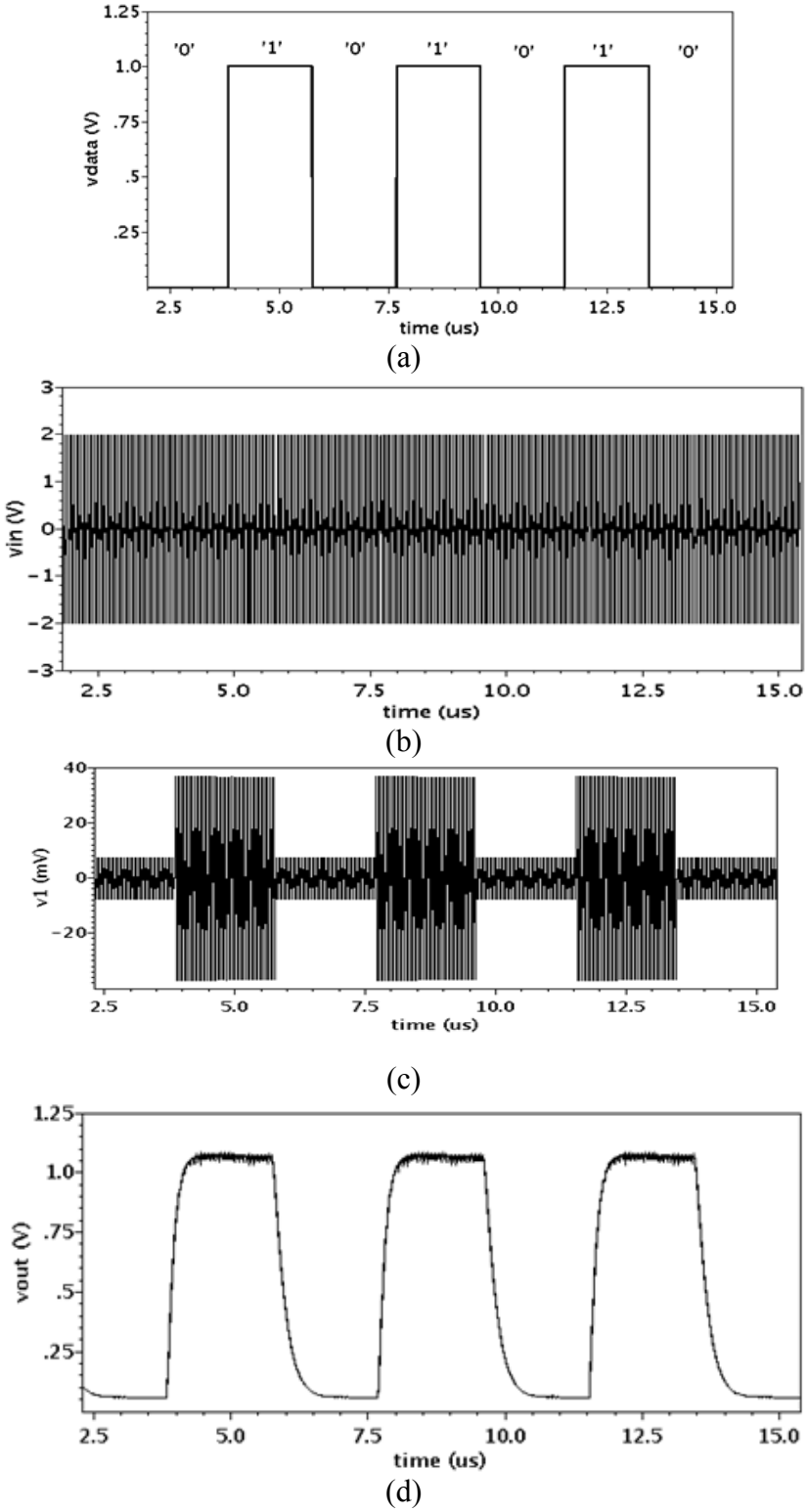



**Fig. 3-2 The simulation results of the proposed BPSK demodulator**
**(a). Modulating signal versus time.**
**(b). BPSK modulated signal.**
**(c).Voltage drop on $R_1$.**
**(d).The simulated output.**

The memristor area is calculated by multiplying its width by its length. The memristor dimensions, used for calculating the area of the proposed designs, are shown in Table 3.2. These dimensions were used for practically implementing memristors in [27]. Then, the empirical model suggested in [27] was investigated and improved to generate the adopted, nonlinear dopant drift memristor, model [26].

**Table 3-2. The memristor dimensions used for estimating the area of proposed designs.**

| | Length | Width | Thickness |
|---|---|---|---|
| Thin-film | 50 nm | 50 nm | 50 nm |

Compared to the other reported BPSK reported in [80] ,the proposed design has smaller area and smaller consumed power, in spite of the larger supply voltage. A comparison between the proposed memristor based BPSK demodulator circuit and the counterpart design in [80] is summarized in Table 3.3.

**Table 3-3. A comparison between the proposed BPSK demodulator and previous work in literature.**

| | Yamu Hu et al. [80] | Proposed design |
|---|---|---|
| Carrier Frequency | 13.56MHz | 25MHz |
| Data Rate | 1.12Mbps | 0.5Mbps |
| Supply Voltage | 1.8V | 3.3V |
| Power Consumption | 0.7mW | 0.37mW |
| CMOS Technology | TSMC 0.18- μm | UMC 0.13- μm |
| Silicon Area | $0.2mm^2$ | $0.01mm^2$ |

## *3.3 Memristor-based passive QPSK demodulator*

QPSK is an extended version from the BPSK in which a symbol comprising two bits is used. In this way, QPSK has four phases which are supposed to be $0^o$, $90^o$, $180^o$, and $270^o$. QPSK is employed so as to double the data rate relative to the BPSK while keeping same bandwidth [84]. It is the most popular modulation for digital TV signals.

Dissimilar to the proposed BPSK demodulator in which one memristor can discriminate between its phases, $180^o$ and $0^o$, in QPSK demodulator one memristor is not adequate for distinguishing between QPSK phases $0^o$, $90^o$, $180^o$, and $270^o$. Even if the memristor resistance in the state of $180^o$ and $0^o$ phases has unlike averages, but it factually has the identical average memristance in case of $270^o$ and $90^o$ as depicted in Fig. 2-5(c). Consequently, a design composed of two branches is suggested as QPSK demodulator with a schematic clarified in Fig. 3-3. In the top branch, the QPSK modulated signal, demonstrated in Fig. 3-4(a), is directly applied to the upper resistor-memristor voltage divider cascaded by the upper peak detector. However, in the bottom branch, an intended $-45^o$ phase shift (realized using $C_{shift}$ and $R_{shift}$) is firstly performed after that, the output of the phase shifter is applied to the lower branch peak detector. The resultant phase shifts of the QPSK modulated signal once going through the $-45^o$ phase

shifter circuit will be 315°, 45°, 135°, and 225° respectively. It is worth pointing out that, the memristor average resistance in case of 315° and 45° are equal, which is apparent in Fig. 2-4. The same is valid for 135° and 225° phase shifts as well. In other words, the top branch produces three discrete levels (shown in Fig. 3-4(b)): $L_1$ for 0°, $L_2$ for 180°, and $L_3$ for 270° and 90°. At the same time as, the lower branch produces two discrete levels (shown in Fig. 3-4(c)): $L_4$ for 0° (that is converted into 315° after -45° shifter), $L_4$ again (for 90° that becomes 45°), $L_5$ (for 180° that is converted into 135°), and $L_5$ also (for 270° which becomes 225°). The parameter values used in circuit simulations are listed in Table 3-4.

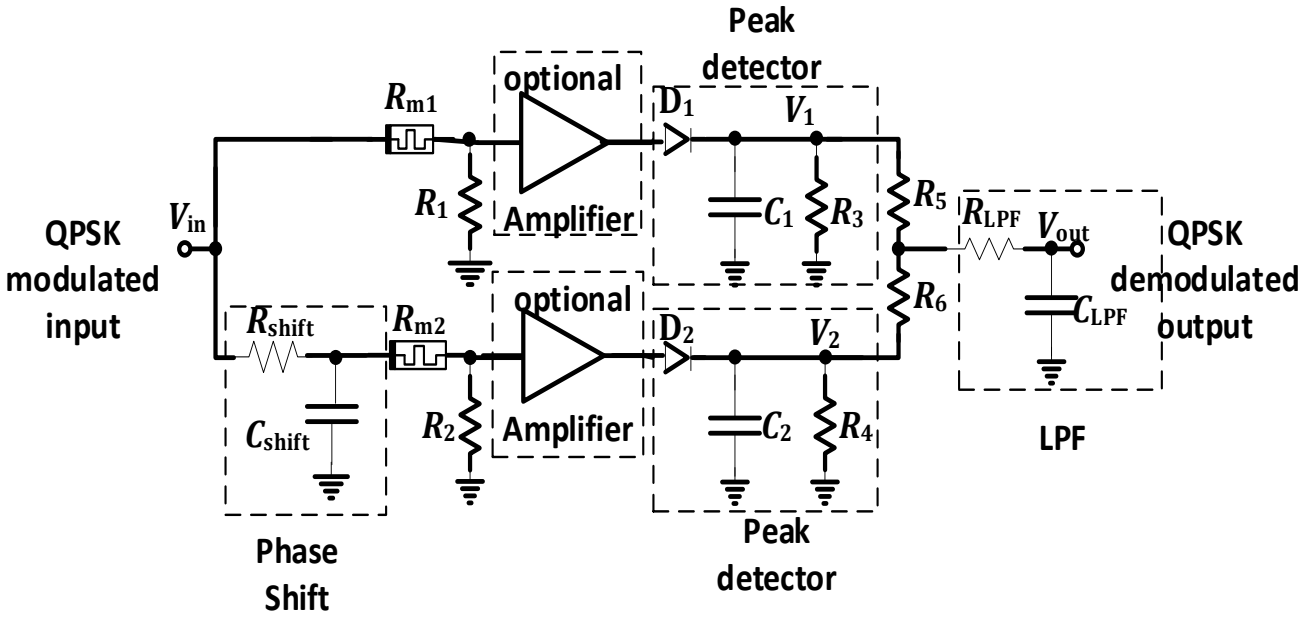
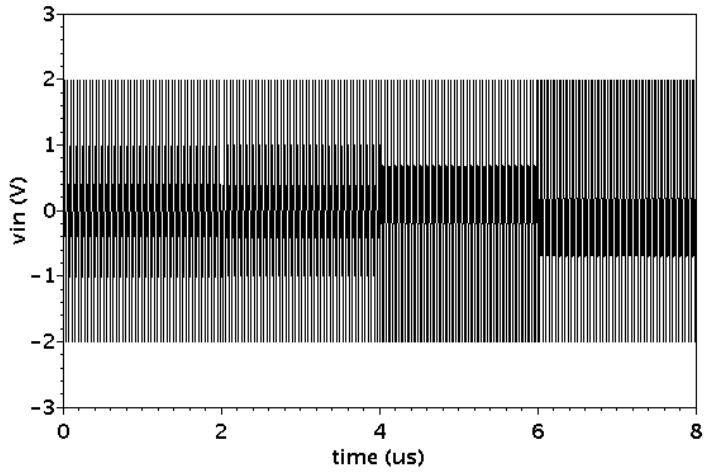


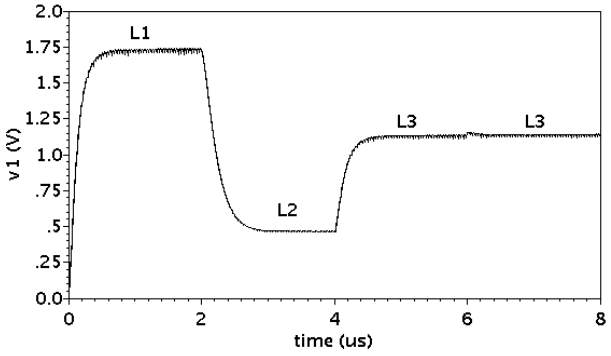

**Fig. 3-3 Schematic of the proposed QPSK demodulator.**

Taking the average for the upper and lower branches outputs mutually would result into four dissimilar voltage levels (clear in Fig. 3-4(d)): ($L_a$, $L_b$, $L_c$, and $L_d$) associating to the QPSK four states.

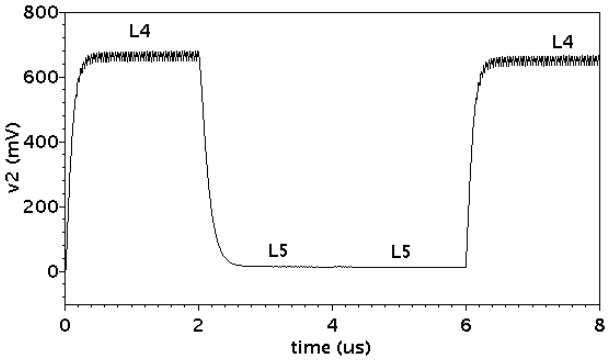
The figures show the suggested circuit simulation can be concluded as: Fig. 3-4(a) illustrates the Cadence transient simulation for the QPSK modulated signal, Fig. 3-4(b) demonstrates the output of the upper peak detector, while Fig. 3-4(c) clarifies the output of the lower peak detector, and Fig. 3-4(d) shows the final circuit output. The results show that the simulated final output comprises four diverse output levels which appear to be in approximate agreement with the expected performance. The voltage levels for the upper and lower peak detectors outputs and the resultant corresponding outputs are identified in Table 3-5. On the other hand, the simulations reveal an average of error approximately equals to 1.4% in the proposed QPSK demodulator output levels assuming a 5° phase error.



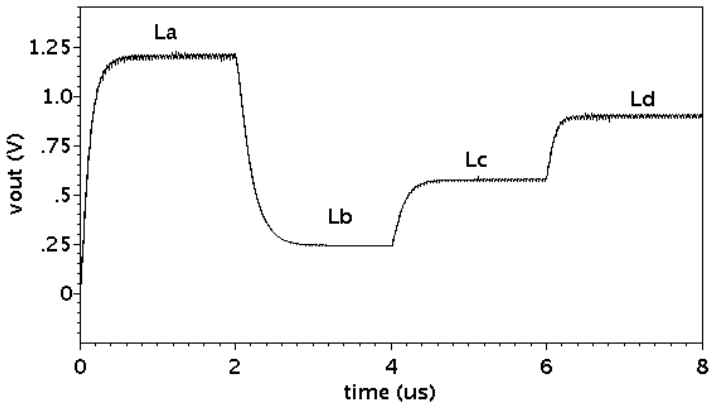

(a)




(b)




(c)




(d)

**Fig. 3-4 (a). QPSK modulated signal.**
**(b). Output of upper peak detector ($V_1$).**
**(c). Output of lower peak detector ($V_2$).**
**(d). The output of the proposed QPSK demodulator.**

**Table 3-4. The parameter values for the proposed QPSK demodulator.**

| Parameter | value |
|---|---|
| $R_1$ | 1 kΩ |
| $R_2$ | 1 kΩ |
| $R_{shift}$ | 6.366Ω |
| $R_3$ | 30Ω |
| $R_4$ | 30Ω |
| $R_5$ | 50Ω |
| $R_6$ | 50Ω |
| $C_1$ | 10nF |
| $C_2$ | 10nF |
| $C_{shift}$ | 1nF |
| $C_{LPF}$ | 1nF |
| $R_{LPF}$ | 50Ω |
| $V_{in}$ | 2V |
| $f_c$ (carrier frequency) | 25MHz |
| $T_b$ | 2μs |

As the proposed demodulator design is mainly based on a voltage divider, the error in input amplitude linearly changes the output amplitude [75]. The characteristics of the proposed QPSK demodulator are extracted from the circuit simulations and summarized in Table 3-6.

**Table 3-5. Details of the expected detected levels before, after the - 450 shifter and the final levels after averaging process (adopted from [75]).**

| Phase shift of input QPSK modulated signal | $0^o$ | $180^o$ | $270^o$ | $90^o$ |
|---|---|---|---|---|
| Detected levels by upper peak detector | $L_1$=1.738V | $L_2$=0.467V | $L_3$=1.133V | L=1.139V≈$L_3$ |
| Phase shift after -$45^o$ shifter | $315^o$ | $135^o$ | $225^o$ | $45^o$ |
| Detected levels by lower peak detector | $L_4$=0.667V | $L_5$=0.017V | L=0.016V≈$L_5$ | L5=0.642V≈$L_4$ |
| Output levels after average circuit and LPF | $L_a$=1.205V | $L_b$=0.240V | $L_c$=0.576V | $L_d$=0.891V |

**Table 3-6. The specifications of the proposed QPSK demodulator.**

| | |
|---|---|
| Carrier Frequency | 25MHz |
| Data Rate | 1Mbps |
| Supply Voltage | 3.3V |
| Power Consumption | 0.74mW |
| CMOS Technology | UMC 0.13- µm |
| Silicon Area | 0.02mm$^2$ |

## *3.4 All-Passive memristor based BFSK demodulator*

The binary FSK (BFSK) is the simplest modulation scheme for the frequency shift keying. BFSK makes use of two of distinct frequencies to convey binary information ('1' and '0' logic). This modulation scheme is used for caller ID, amateur radio, and emergency broadcasts communication systems [84]. As reported in Chapter Two (Fig 2-2 (a) and Fig 2-2 (b)), the memristor resistance dynamic range gets smaller and the I–V characteristics of the memristor changes towards a straight line as the frequency of the applied signal increases. Therefore it is foreseen that, the pre-mentioned memristance response to the change of signal frequency can be used to design memristor-based BFSK demodulator.

Fig. 3-5 shows the proposed demodulator; where Fig. 3-5 (a) demonstrates the demodulator conceptual block diagram, while Fig. 3-5 (b) shows the schematic of the suggested circuit realization. The demodulator circuit starts with a voltage divider arrangement between a resistor $R_1$ and a memristor element $R_m$. The voltage divider output can be evaluated using (3-3).

$$V_1 = V_{in} \frac{R_1}{R_1 + R_m} \qquad (3-3)$$

As $R_m$ varies with the frequency of the excitation, the amplitude of $V_1$ (the voltage drop on $R_1$) will also change with the frequency as clear in (3-3). By this means, this voltage divider translates the change in the frequency of the sinusoidal input into a change in the amplitude of the sinusoidal output, producing a memristor based FSK to ASK (Amplitude Shift Keying) converter. The peak detector, next to the voltage divider in Fig. 3-5 (b), is formed by a series connection of a diode (D) and a capacitor ($C_1$). DC voltage, proportional to the applied ASK modulated signal amplitude, is the output of this peak detector. The resistor $R_2$ offers a path for discharging the capacitor voltage. After the amplitude of the peak detector input goes down (i.e. a modulated signal with higher frequency is received), the capacitor voltage decreases by being discharged via a bleed resistor $R_2$, with no need for any reset circuit.

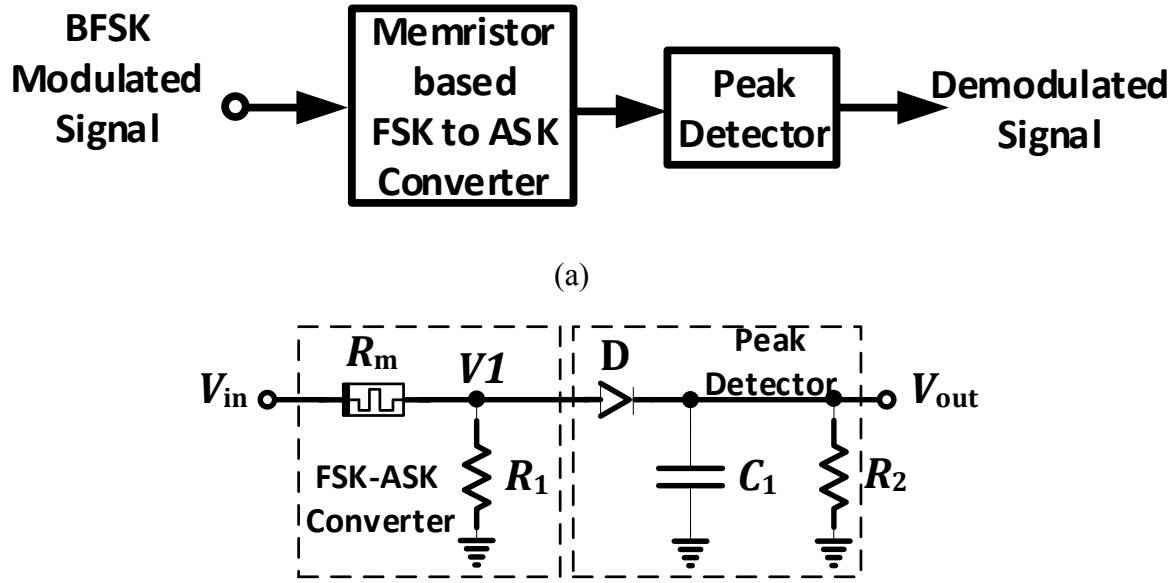



**Fig. 3-5 (a) Block diagram of the proposed memristor-based BFSK demodulator. (b) Schematic of the proposed memristor-based BFSK detector (adopted from** [77]**).**

Thereby, the output of this proposed demodulator is a multi-level DC output that proportionate to the frequency of the input modulated waveform. The parameter values used in circuit simulations using the linear dopant drift model are listed in Table 3-7. Fig. 3-6 (a) and (b) plot the results of transient simulation using linear dopant drift model [32] that validates the operation theory. The assumed input is a train of '1' and'0' alternatively. The alternative separated levels (L1 and L2) can be clearly noticed at the simulated output drawn in Fig. 3-6 (b) which coincides with the anticipated performance. Investigating the influence of the frequency error shows that, in case of a 5% frequency error, the simulations reveal a 0.06% error in the output signal levels [77].

The simulations were repeated using the nonlinear dopant drift model [26] with the results shown in Fig.3-7. The parameter values used in simulations using the nonlinear dopant drift model are listed in Table 3-8. It can be noted that, the value of $R_2$ and $C_1$ in the design using the nonlinear dopant drift model are smaller than them using the linear one (Table 3-7), this can be justified by the increasing of the operating frequency. While, the value of $R_1$ is expected to be larger in the nonlinear dopant drift model due to the increasing of the memristance value in the nonlinear model. t is worth pointing out that as $R_1$ is small relative to $R_m$ as $V_1$ is more sensitive to the change in $R_m$. This change results from the change of the modulation frequency in case of the BFSK modulation scheme. However, the further reduction of $R_1$value leads to very small amplitude levels of $V_1$which needs higher amplification gain to be detected by the peak detector. Therefore, a compromisation should be done.

**Table 3-7. The parameter values of the proposed BFSK demodulator using the linear dopant drift model.**

| Parameter | values |
|---|---|
| $R_{on}$ | 100Ω |
| $R_{off}$ | 38kΩ |
| $R_{init}$ | 5kΩ |
| $\mu_v$ | 10f $m^2s^{-1}v^{-1}$ |
| D | 10nm |
| Amplitude | 5V |
| Initial phase | $0^o$ |
| F1 | 3 Hz |
| F2 | 6 Hz |
| $R_1$ | 7kΩ |
| $R_2$ | 5MΩ |
| $C_1$ | 0.5μF |
| $T_b$ | 2s |

Moreover, in case of simulations using the nonlinear dopant drift model, an amplifier with voltage gain equals 10 is added before the peak detector and also first order LPF is used as the final stage. The need for amplification makes the proposed demodulator lose its "all passive" feature. This can be justified by the fact that, the threshold voltage decreases when using the nonlinear model compared to using the linear model. Thus, the amplitude limit of the input modulated signal and correspondingly the voltage divider output is smaller in the nonlinear model which explains the required amplification to overcome the forward voltage of the diode.

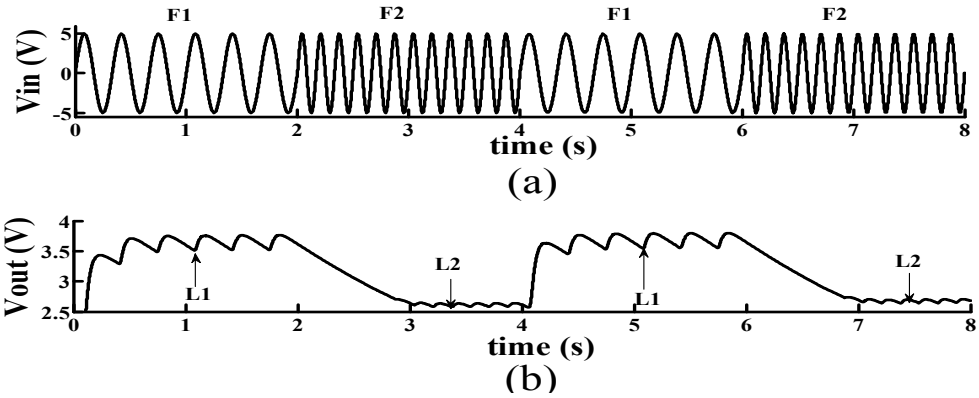



**Fig. 3-6 (a) input BFSK modulated signal. (b). The transient simulation output for the proposed memristor based BFSK demodulator using the linear dopant drift model.**

**Table 3-8. The parameter values of the proposed BFSK demodulator using the nonlinear dopant drift model.**

| | |
|---|---|
| Amplitude | 2V |
| Initial phase | $0^o$ |
| F1 | 11 MHz |
| F2 | 16 MHz |
| $R_1$ | 8kΩ |
| $R_2$ | 50Ω |
| $C_1$ | 10nF |
| $T_b$ | 2 µs |

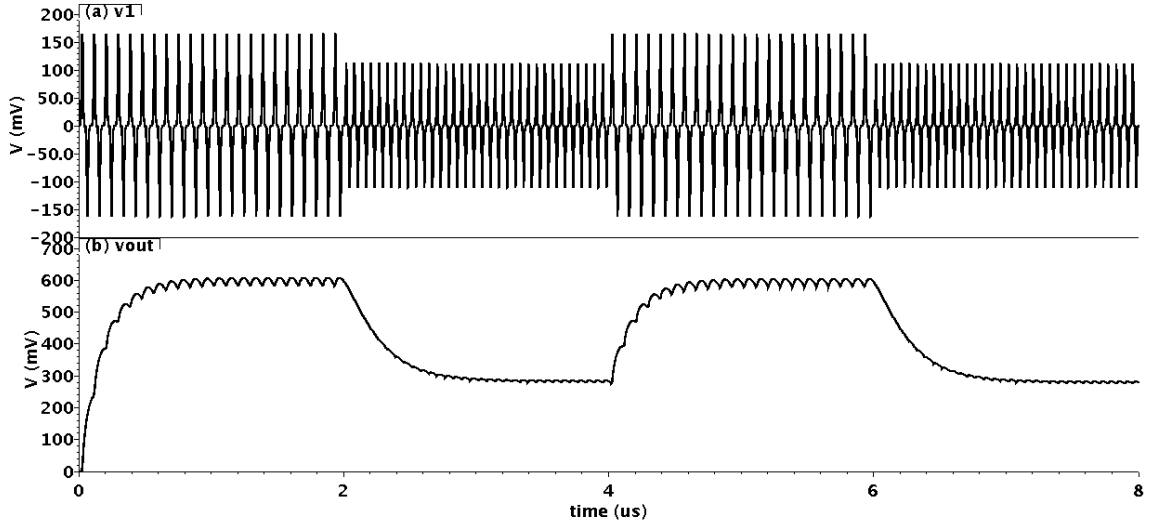



**Fig. 3-7 (a). Output of memristor-resistor voltage divider. (b). Final output of the proposed memristor based BFSK demodulator using the nonlinear dopant drift model.**

Moreover, the LPF used to reduce the fluctuation in the output is similar to that used in Fig. 3-1 (b) with $c_2 = 1\text{nF}$ and $R_3 = 50\Omega$. The characteristics of the proposed BFSK demodulator using the nonlinear dopant drift model are summarized in Table 3-9.

**Table 3-9. The specifications of the proposed BFSK demodulator using the nonlinear dopant drift model.**

| | |
|---|---|
| Carrier Frequency | 25MHz |
| Data Rate | 0.5Mbps |
| Supply Voltage | 3.3V |
| Power Consumption | 0.37mW |
| CMOS Technology | UMC 0.13- µm |
| Silicon Area | $0.01\text{mm}^2$ |

## *3.5 All-Passive memristor-based circular 8-QAM demodulator*

The final waveform of QAM modulated waveform is a combination of both ASK and PSK. The circular 8-QAM constellation diagram is presented in Fig. 3-8.

With respect to this the circular 8-QAM, the modulated signal has two probable amplitudes and eight possible phases. In Chapter 2 (Fig. 2-1(a)), it has been clarified that the fluctuation of the memristor resistance and accordingly its average during the carrier cycle are influenced by the amplitude and the initial phase of the applied sinusoidal voltage. This characteristic is exploited for generating eight different output levels for different eight amplitude- phase combinations.

### *3.5.1 The operation principle and simulation results*

It has been postulated that, the points of constellation for the feasible modulated signal are as drawn in Fig. 3-8 whereas S1, S2, S3, and S4 have equal amplitude and $45^o$, $135^o$, $225^o$, and $315^o$ phase shift respectively. Similarly, S5, S6, S7, and S8 have equal amplitude (which is different from S1, S2, S3, and S4 amplitude) and have respectively $0^o$, $90^o$, $180^o$, and $270^o$ phase shifts. Revising some previously derived properties, one memristor can discriminate between two states of different amplitude because the memristor has different average resistance for different amplitude values. However, it cannot easily differentiate between every two points of same amplitude. Added to this, the memristor basically has the same average memristance for the cases of ($90^o$, $270^o$), ($315^o$, $45^o$), and ($135^o$, $225^o$) as demonstrated earlier in Fig. 2-3(b) and Fig. 2-4. Nevertheless, if a phase shift of $-45^o$ is intentionally applied it guarantees that each two signals in apre-mentioned couples can be distinguished.

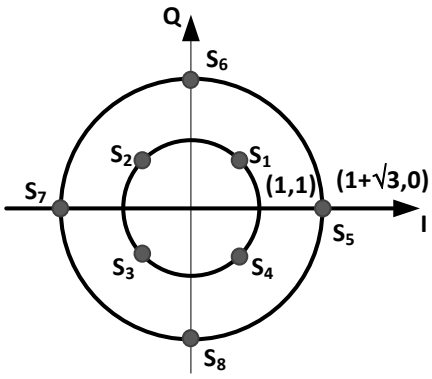



**Fig.3-8 The constellation diagram of the circular 8-QAM.**

Fig. 3-9 shows the schematic diagram of the suggested circular 8-QAM demodulator. It consists of two branches, the upper one commences with the basic memristor-based detector (utilized before in BFSK demodulator) with the direct 8-QAM modulated signal input. The lower branch commences also with the same basic memristor-based detector but for the $-45^o$ shifted version of 8-QAM modulated signal instead of the direct 8-QAM modulated signal. As a final step, the upper and lower detectors outputs are averaged then the result is applied to a first order low pass filter for reducing output fluctuations. The parameter values used in simulations using the linear dopant drift model are listed in Table 3-10. Fig. 3-10(a) and 3-10(b) display transient simulation for the proposed design input and output respectively using the linear dopant drift model. The output provides eight different levels (L1-L8) and the level voltage values are reported in Table 3-11. Correspondingly, the simulations reveal that a phase error of $5^o$ in the input phases would

lead to a 1.4% error in the output levels [77]. The simulation was repeated using the nonlinear dopant drift model with parameter values listed in Table 3-12 and Fig. 3-11 shows the simulated output. Similar to the proposed BFSK demodulator using the nonlinear model, the QAM demodulator using the nonlinear model would also need an amplification stage before the peak detection which is attributed to the decrease of the threshold voltage and the sensitivity to the change of the applied signal amplitude in the nonlinear model compared to the linear one. The output levels values are reported in Table 3-13. The characteristics of the proposed 8-QAM demodulator using the nonlinear dopant drift model are summarized in Table 3-14.

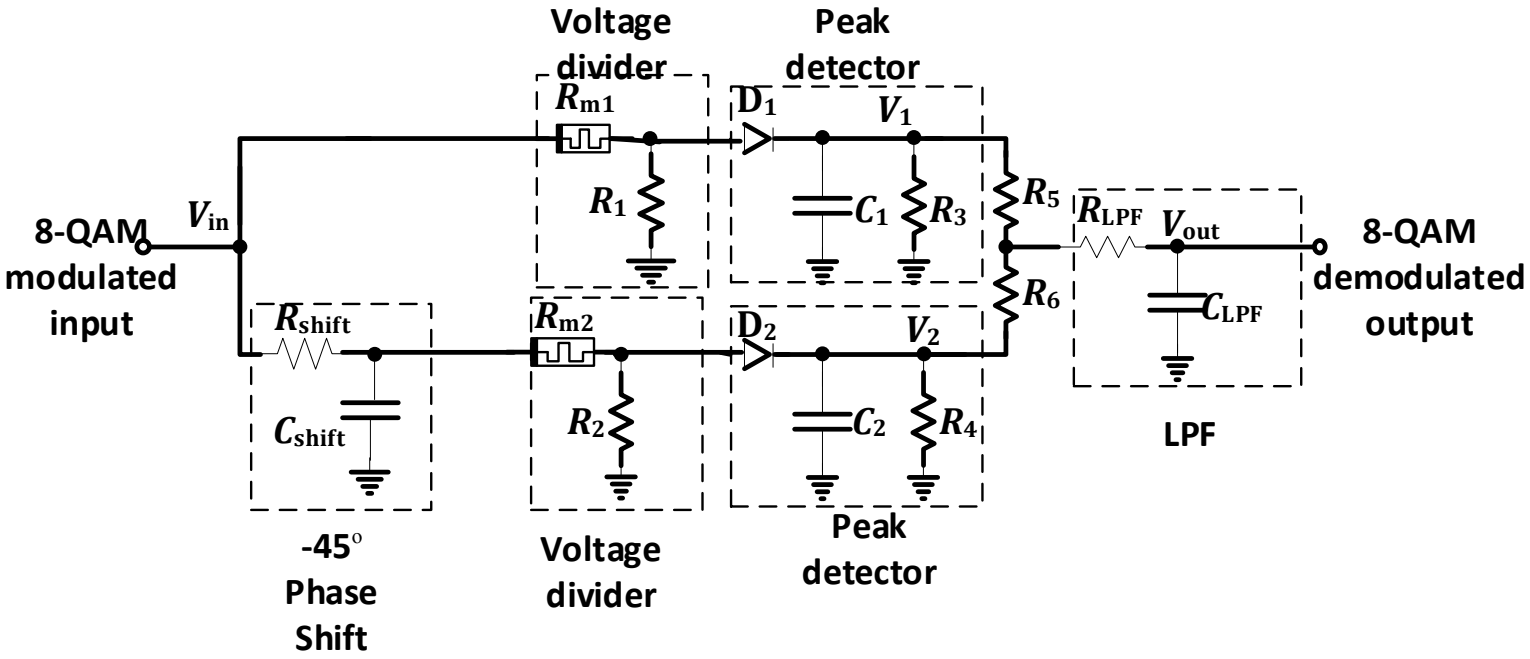
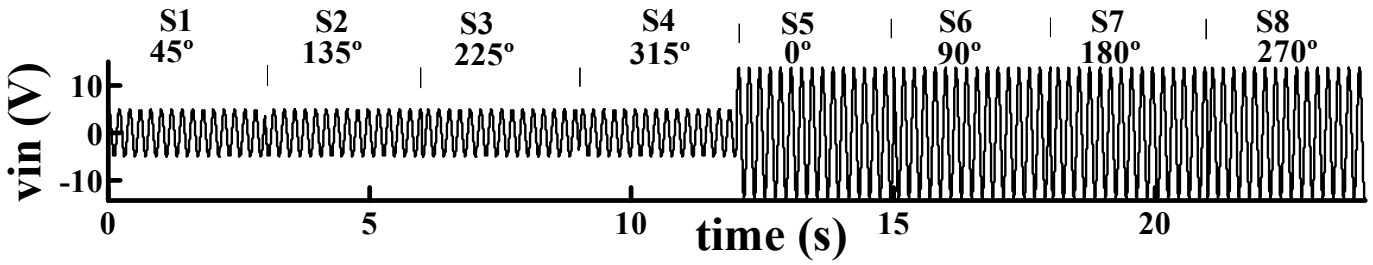


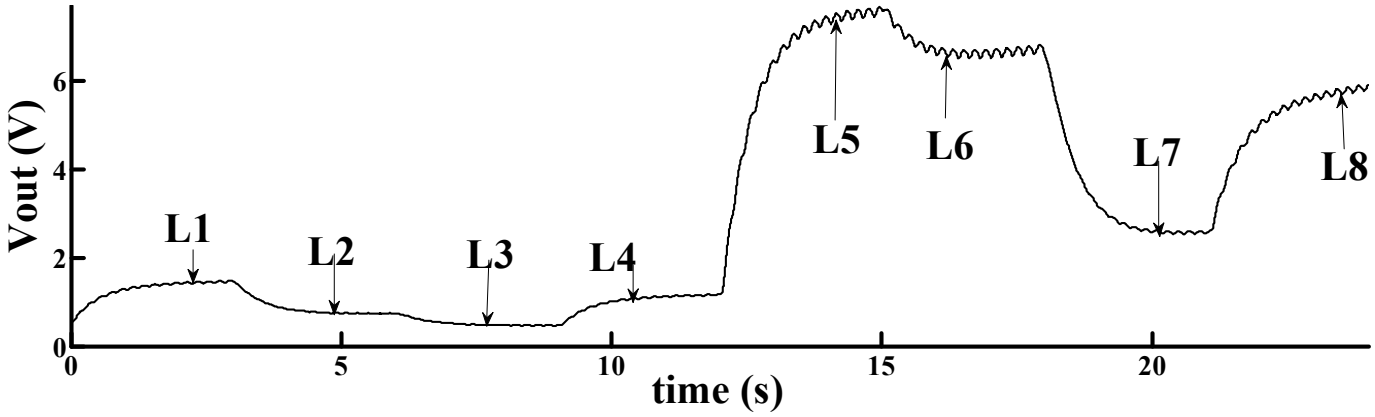

**Fig.3-9 schematic of the proposed 8-QAM demodulator.**

**Table 3-10. The parameter values of the proposed 8-QAM demodulator using the linear dopant drift model.**

| Parameter | value | Parameter | value |
|---|---|---|---|
| $R_{1on}$ | 100Ω | $R_2$ | 10 kΩ |
| $R_{1off}$ | 50kΩ | $R_{shift}$ | 1.591K Ω |
| $R_{1init}$ | 24kΩ | $R_3$ | 2M Ω |
| $\mu_{1v}$ | 10f $m^2s^{-1}v^{-1}$ | $R_4$ | 2M Ω |
| $D_1$ | 5nm | $R_5$ | 6M Ω |
| $R_{2on}$ | 100Ω | $R_6$ | 3M Ω |
| $R_{2off}$ | 50kΩ | $C_1$ | 0.1μ F |
| $R_{2init}$ | 20kΩ | $C_2$ | 0.1μ F |
| $\mu_{2v}$ | 10f $m^2s^{-1}v^{-1}$ | $C_{shift}$ | 0.1μ F |
| $D_2$ | 5nm | $C_{LPF}$ | 0.1μ F |
| $R_1$ | 6.5 kΩ | $R_{LPF}$ | 700K Ω |
| $V_{1in}$ | 5V | $f_c$ (carrier frequency) | 25MHz |
| $V_{2in}$ | 10V | $T_b$ | 2μs |




(a)




**(b)**

**Fig.3-10. (a) 8-QAM modulated input.**

**(b) The transient simulation output for the proposed memristor based circular 8-QAM demodulator using the linear dopant drift model.**

**Table 3-11. The final output levels of the 8-QAM demodulator using the linear dopant drift model.**

| Output level | Value (V) |
|---|---|
| L1 | 1.454 |
| L2 | 0.7363 |
| L3 | 0.4716 |
| L4 | 1.157 |
| L5 | 7.568 |
| L6 | 6.741 |
| L7 | 2.568 |
| L8 | 5.861 |

**Table 3-12. The parameter values of the proposed 8-QAM demodulator using the nonlinear dopant drift model.**

| Parameter | value | Parameter | value |
|---|---|---|---|
| $R_{1on}$ | 100Ω | $R_3$ | 30Ω |
| $R_{1off}$ | 50kΩ | $R_4$ | 30Ω |
| $R_{1init}$ | 24kΩ | $R_5$ | 50Ω |
| $\mu_{1v}$ | 10 $fm^2s^{-1}v^{-1}$ | $R_6$ | 50Ω |
| $D_1$ | 5nm | $C_1$ | 10nF |
| $R_{2on}$ | 100Ω | $C_2$ | 10nF |
| $R_{2off}$ | 50kΩ | $C_{shift}$ | 1nF |
| $R_{2init}$ | 20kΩ | $C_{LPF}$ | 1nF |
| $\mu_{2v}$ | 10 $fm^2s^{-1}v^{-1}$ | $R_{LPF}$ | 50Ω |
| $D_2$ | 5nm | $V_{1in}$ | 2V |
| $R_1$ | 1 kΩ | $V_{2in}$ | 2.35V |
| $R_2$ | 1 kΩ | $f_c$ (carrier frequency) | 25MHz |
| $R_{shift}$ | 6.366Ω | $T_b$ | 2μs |

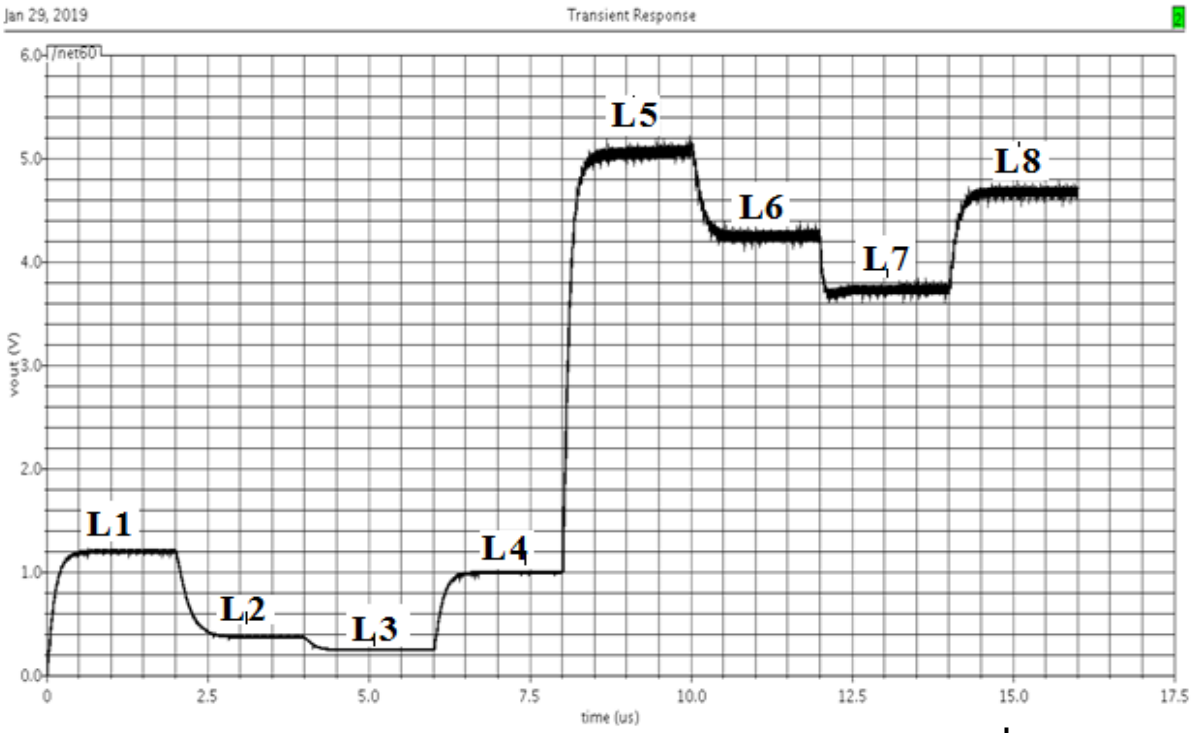



**Fig.3-11. The transient simulation output for the proposed memristor based circular 8-QAM demodulator using the nonlinear dopant drift model.**

**Table 3-13. The final output levels of the 8-QAM demodulator using the nonlinear dopant drift model.**

| Output level | Value (V) |
|---|---|
| L1 | 1.2 |
| L2 | 0.366 |
| L3 | 0.24 |
| L4 | 0.995 |
| L5 | 5 |
| L6 | 4.2 |
| L7 | 3.76 |
| L8 | 4.69 |

**Table 3-14. The specifications of the proposed 8-QAM demodulator using the nonlinear dopant drift model.**

| | |
|---|---|
| Carrier Frequency | 25MHz |
| Data Rate | 1.5Mbps |
| Supply Voltage | 3.3V |
| Power Consumption | 0.74mW |
| CMOS Technology | UMC 0.13- μm |
| Silicon Area | $0.02mm^2$ |

# Chapter Four

# MEMRISTOR BASED PHASE FREQUENCY DETECTOR AT 25MHZ WITH NONLINEAR DOPANT DRIFT MODEL FOR PHASE LOCKED LOOP APPLICATION

The phase detector is a basic and necessary element of the Phase Locked Loop (PLL) system. It is usually defined as a frequency mixer, analog multiplier or logic circuit that generates a voltage signal which represents the difference in phase between two signal inputs [86]. In this Chapter, a novel and simple phase frequency detection technique based on two memristor elements, is proposed and demonstrated. This technique is able to generate a DC signal that represents the difference in phase or frequency between two sinusoidal inputs. Therefore, the proposed technique eliminates the need for LPF block in the PLL structure which reduces the dissipated power and the area of the overall PLL system hence results in more efficiency when used in body implants. This PFD is based on the nonlinear dopant drift model [26]. Moreover, this Phase detector can be cascaded by a memristor based VCO to build the first ever reported memristor based PLL system, as demonstrated in the following Chapter.

## 4.1 Problem definition

The main objective of this chapter is to exploit the phenomena of the memristor resistance variation with the applied initial signal phase and the nano dimensions of the memristor device to develop an area-efficient memristor-based circuit configuration for phase frequency detector circuit. This circuit has two sinusoidal input signals with different frequency (phase) and the investigated circuit should provide a DC output which is proportional with the frequency (phase) difference between the two input signals. Additionally, the relationship between the DC output voltage and the phase difference should be anti-symmetric curve (positive for positive phase difference and negative for negative phase difference or vice versa) to provide the capability of using the sign of the output DC voltage for detecting the direction of the phase difference. The linear dopant drift model is used to get closed form analytical argument while simulations using the nonlinear dopant drift model are performed to confirm the validity of the used concept.

## 4.2 Proposed Phase detector basic structure response to phase shift difference

Let $v_1(t)$ and $v_2(t)$ be the two signals where the difference between their phases is to be measured. Assuming that $v_1(t)$ and $v_2(t)$ have same frequency, same amplitude, and different phase where $v_1(t) = sin(\omega t)$, $v_2(t) = cos(\omega t + \theta)$, $\omega = 2\pi f$ is the radial frequency, $f$ is their frequency, $T = 1/f$ is the signals period, and $\theta$ is the phase difference between the two signals. Apply the signal $v_2(t)$ to two memristors of opposite polarity as shown in Fig. 4-1. S1 and S2 are ON when $v_1(t) > 0$ and OFF when $v_1(t) < 0$.

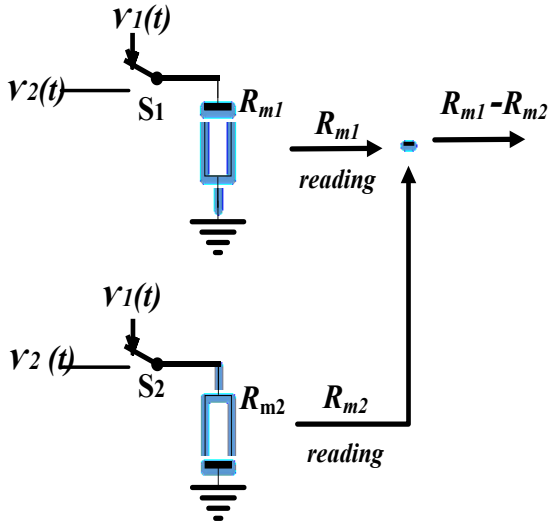



**Fig. 4-1. Basic structure of the proposed memristor based phase detector.**

### 4.2.1 Analytical analysis and simulated results using the linear dopant drift model

The final resistance value of upper memristor, $R_{m1}$, after one positive half cycle of $v_1(t)$ is calculated using (1-7) to be

$$R_{m1}\left(t = \frac{T}{2}\right) = \sqrt{R_{init}^2 - 2kR_d \int_0^{\frac{T}{2}} v_2(t)\, dt} = \sqrt{R_{init}^2 - \frac{2kR_d}{\omega}(-sin(\theta) - sin(\theta))}$$

$$= \sqrt{R_{init}^2 + \frac{4kR_d}{\omega} sin(\theta)} = R_{init}\sqrt{1 + \frac{4kR_d}{\omega R_{init}^2} sin(\theta)} \approx$$

$$R_{init}\left(1 + \frac{2kR_d}{\omega R_{init}^2} sin(\theta)\right), \text{ for } \frac{4kR_d}{\omega R_{init}^2} \ll 1 \qquad (4-1)$$

Similarly, the resistance of lower memristor, $R_{m2}$, after one positive half cycle of $v_1(t)$ is calculated using (1-7), taking into consideration its opposite alignment and assuming same initial resistance of upper one, to be

$$R_{m2}\left(t=\frac{T}{2}\right)=\sqrt{R_{init}^2-2kR_d\int_0^{\frac{T}{2}}-v_2(t)\,dt}$$

$$=\sqrt{R_{init}^2+\frac{2kR_d}{\omega}\left(sin\left(\omega\frac{T}{2}+\theta\right)-sin(\theta)\right)}=$$

$$\sqrt{R_{init}^2+\frac{2kR_d}{\omega}(-sin(\theta)-sin(\theta))}\quad=$$

$$\sqrt{R_{init}^2-\frac{4kR_d}{\omega}sin(\theta)}\;=\;R_{init}\sqrt{1-\frac{4kR_d}{\omega R_{init}^2}sin(\theta)}$$

$$\approx\;R_{init}\left(1-\frac{2kR_d}{\omega R_{init}^2}sin(\theta)\right),\qquad\text{for}\quad\frac{4kR_d}{\omega R_{init}^2}\ll 1 \qquad (4-2),$$

From (4-1) and (4-2)

$$(R_{m1}-R_{m2})|_{t=\frac{T}{2}}\;\approx\frac{4kR_d}{\omega R_{init}}sin(\theta)$$

$$\approx\frac{4kR_d}{\omega R_{init}}\theta,\qquad\text{for}\quad\theta<\frac{\pi}{12} \qquad (4\text{-}3)$$

The results of (4-3) show that the difference of the two memristors resistance in the proposed structure can be used for phase detection. It is also worth noting that, the approximations used in the above derivation are for simplifying the calculation in order to get a closed form expression that demonstrates the proportionality between $(R_{m1}-R_{m2})|_{t=\frac{T}{2}}$ and $\theta$. It is important to note also that the linear relation between the input phase shift and output voltage, or resistance in our case, of phase detector is not a necessary condition in typical PLL systems, if the relation between the DC input voltage and the VCO output frequency is not linear as demonstrated in Chapter 5. The only required relationship is the incremental change, as θ increases as $(R_{m1}-R_{m2})|_{t=\frac{T}{2}}$ increases and vice versa, and anti symmetric relation.

Simulations using Matlab using the linear dopant drift model are performed with the values of memristor parameters reported in Table 4-1. Firstly, the captured part of $v_2(t)$ through the positive half cycle of $v_1(t)$ is shown in Fig. 4-1. It is drawn for different phase shift angles. After that, the dynamic behavior of $R_{m1}$, $R_{m2}$, and $(R_{m1}-R_{m2})$ , during the positive half cycle of $v_1(t)$, are shown in Fig. 4-2

(a), (b), and (c) respectively for different phase shift angles. It is obvious from Fig. 4-1 that, the complete positive half cycle of $v_2(t)$ will be applied on the opposite aligned memristors in case of -90° phase shift, between $v_1$(t) and $v_2$(t), only. While, as the phase shift increases the applied positive part shrinks while the negative part expands.

Given the fact that, the memristance (in linear dopant drift model) decreases as the positive voltage is applied and vice versa. It is foreseen that $R_{m1}$ at $t=T/2$ (which is distinguished by black squares in Fig. 4-3 (a)) is minimum for -90° and increases as the phase difference increases.

**Table 4.1 The memristor parameters used for simulations using the linear dopant drift model**

| Parameter | value |
|---|---|
| $R_{on}$ | 100Ω |
| $R_{off}$ | 16kΩ |
| $R_{init}$ | 11kΩ |
| $\mu_v$ | 10f $m^2s^{-1}v^{-1}$ |
| $D$ | 10nm |
| $f$ | 1Hz |

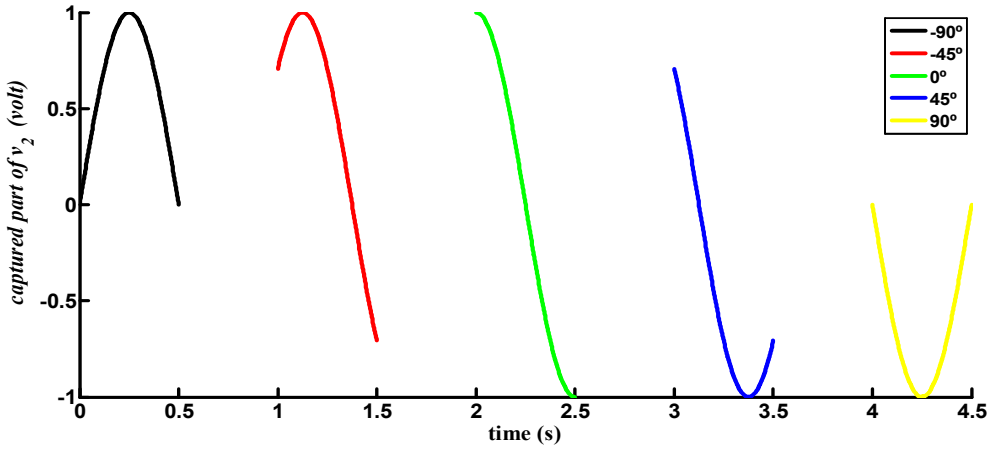
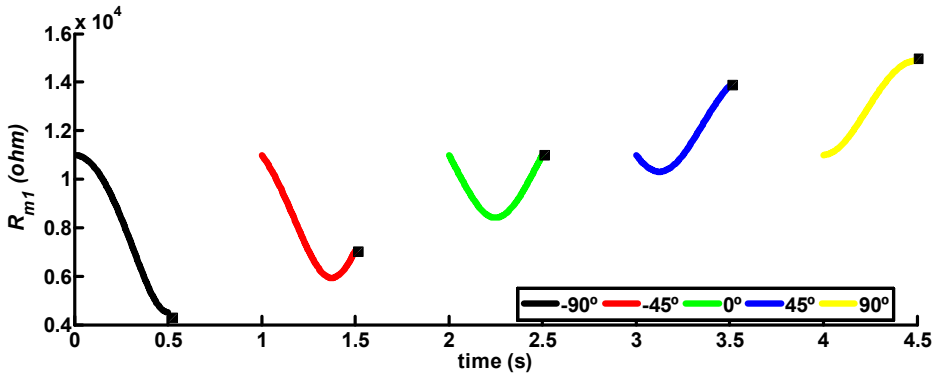
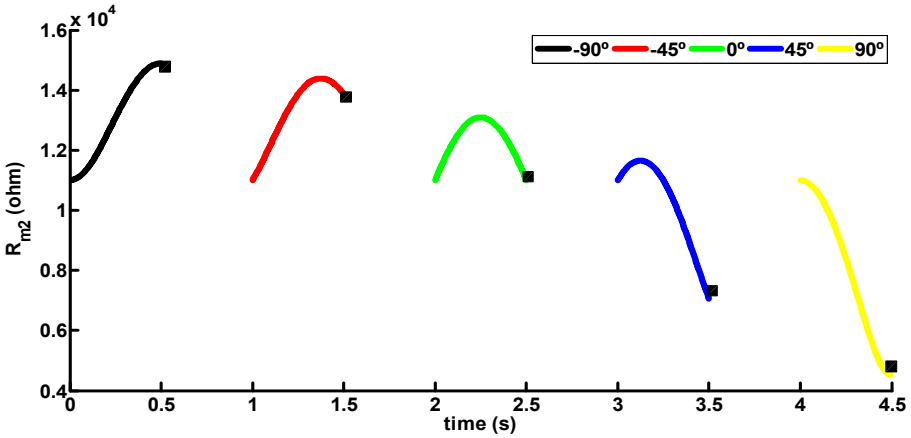



**Fig. 4-2. The captured part of $v_2$ through the positive cycle half of $v_1$ for different phase shift angles.**

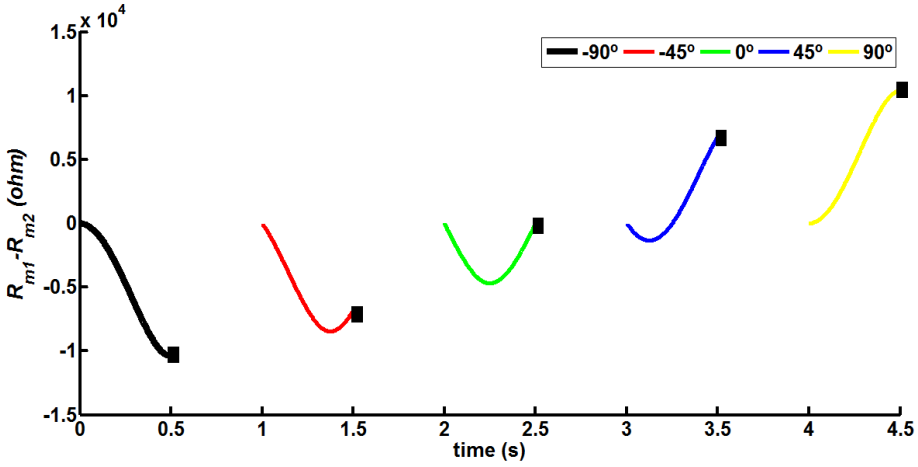
While, $R_{m2}$ at $t=T/2$ (which is distinguished by black squares in Fig. 4-3 (b)) is maximum for -90° and decreases as the phase difference increases due to its opposite polarity alignment. Subtracting the reached memristance of $R_{m1}$ and $R_{m2}$ at $t=T/2$ gives the values distinguished by black squares in Fig. 4-3 (c) for different phase shift angles. It is clear from Fig. 4-3 (c) that the resulting values of $R_{m1}$-$R_{m2}$ at $t=T/2$ are negative for negative phase shift, zero for zero phase shift, and positive for positive phase shift.




(a)




(b)




(c)

**Fig. 4-3 (a). $R_{m1}$ during the positive cycle half of $v_1(t)$ for different phase shift angles.**

**(b) $R_{m2}$ during the positive cycle half of $v_1(t)$ for different phase shift angles.**

**(c) $R_{m1}$ -$R_{m2}$ during the positive cycle half of $v_1(t)$ for different phase shift angles.**

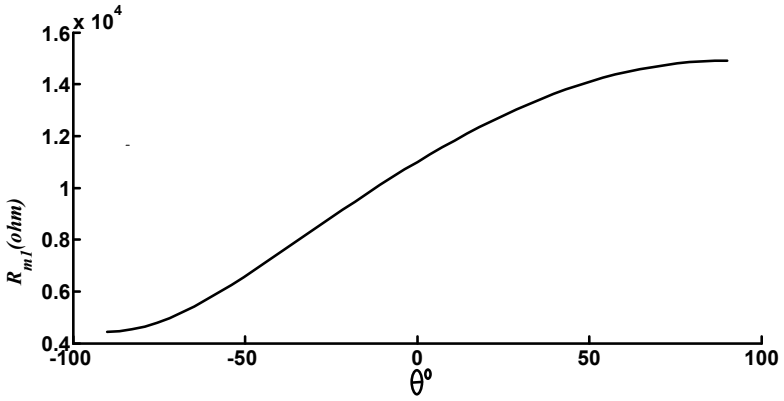
Accordingly, the value of $R_{m1}$-$R_{m2}$ at t=T/2 in the proposed structure can be a good indicator to the phase shift between the two sinusoidal input signals. Using the non-volatility feature of the memristor elements, we can read the value of $R_{m1}$ *and* $R_{m2}$ (at *t=T/2)* during the second cycle half of $v_1$ as discussed in the following subsections. On other hand, the curves of $R_{m1}$, $R_{m2}$, *and* $(R_{m1} - R_{m2})$ at *t*=T/2 versus phase shift angle are drawn in Fig. 4-4 (a), (b), and (c) respectively for angles in the range of [-90$^o$,90$^o$].

### 4.2.2 Verification using the nonlinear dopant drift model

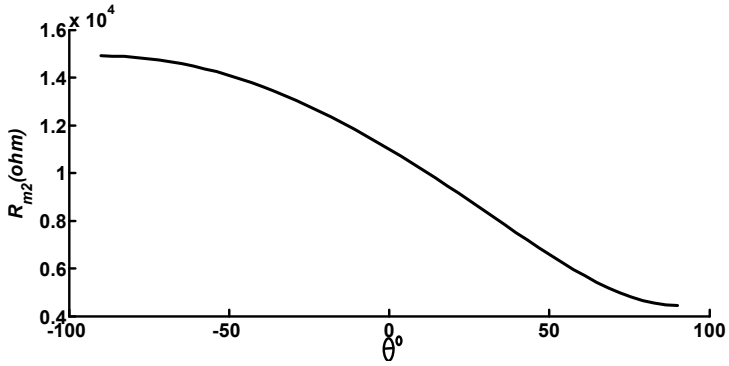
Achieving the goal of a memristor based phase detector design that operates in pragmatic frequency range and considers the non-ideal features of the practically implemented memristors, was the reason behind the adoption of the nonlinear dopant drift model. Matlab simulations using the nonlinear dopant drift models were performed to ensure the consistency with the predicted results. The resulting waveforms are presented in Fig. 4-5. In more detail, Fig. 4-5(a), Fig. 4-5(b), and Fig. 4-5(c) show the variation of $R_{m1}, R_{m2},$ and $(R_{m1} - R_{m2})$ respectively, at the end of captured period (*t=T/2*), with the phase difference between $v_1$ and $v_2$. The range between -90$^o$ and 90$^o$ is distinguished in Fig. 4-5(c) by dashed square. Apparently, the difference between the two memristances in this range satisfies the requirements of proportionality with the phase difference and sensitivity to the phase shift directions which is encouraging to design a memristor-based phase detector using the nonlinear dopant drift model and replacing the linear one. Noting that, the parameter values used in all simulations using the nonlinear model in this and next chapter are mentioned in Table 4-2.

**Table 4.2 The memristor parameters used for simulations using the nonlinear dopant drift model**

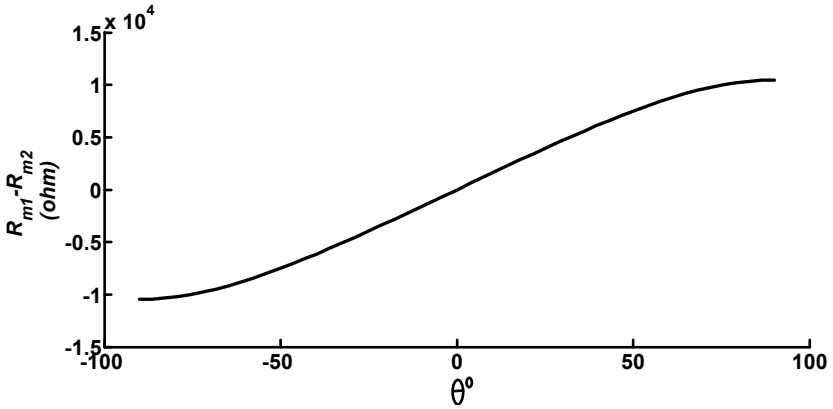
| Parameter | description | value |
|---|---|---|
| $w_o$ | Initial state | 0.95 |
| $f_1$ | Frequency of $v_1$ | 25MHz |
| A | Amplitude of $v_1$ and $v_2$ | 2V |
| $v_{th}$ | Threshold voltage | 0.1V |




(a)




(b)




(c)

**Fig. 4-4 (a). $R_{m1}$ reached at the end of the positive half cycle of $v_1$for different phase shift angles using linear dopant drift model.**

**(b). $R_{m2}$ reached at the end of the positive half cycle of $v_1$for different phase shift angles using linear dopant drift model.**

**(c). $R_{m1}$ -$R_{m2}$ reached at the end of the positive half cycle of $v_1$for different phase shift angles using linear dopant drift model.**

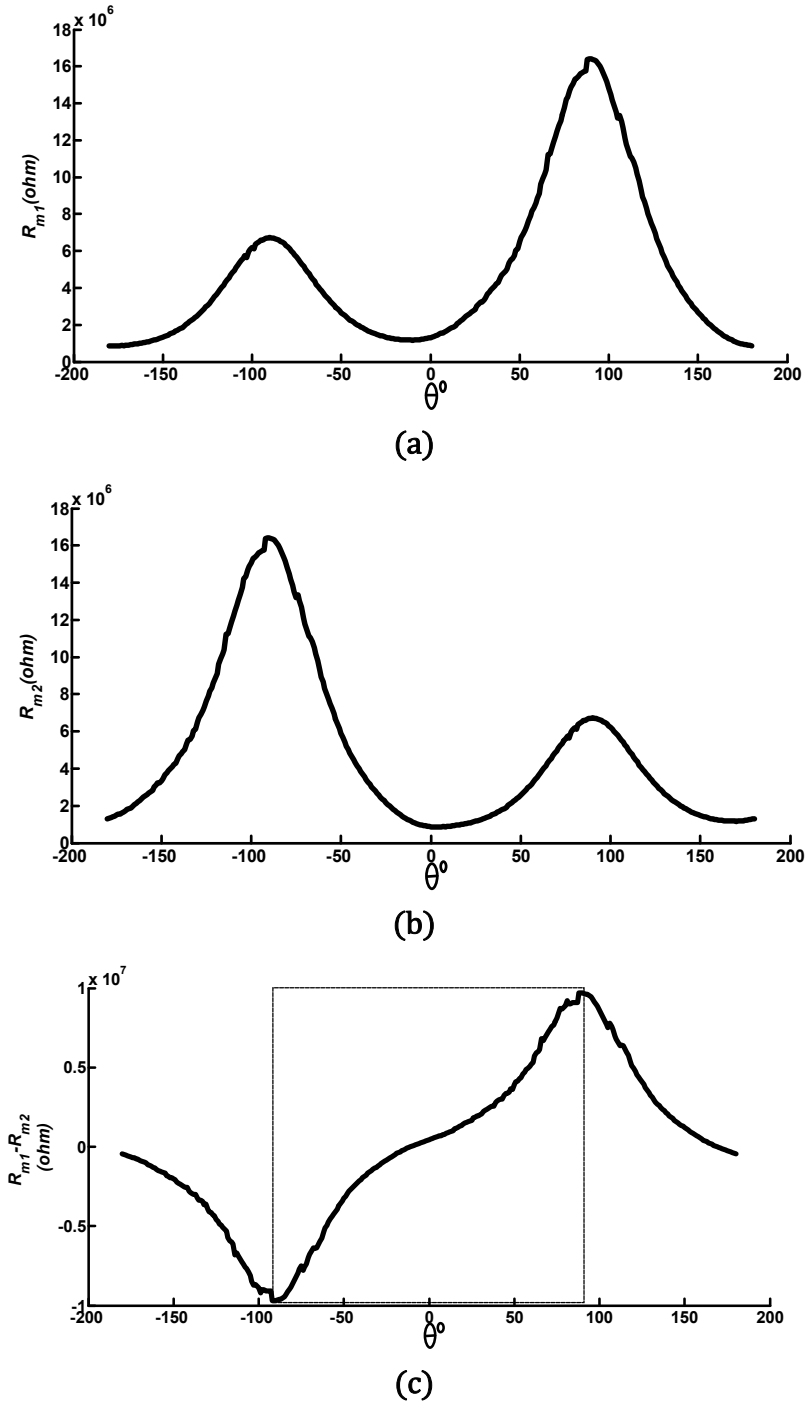



**Fig. 4-5 (a). $R_{m1}$ after the positive half cycle of $v_1$ for different phase shift angles using nonlinear dopant drift model. (b). $R_{m2}$ after the positive half cycle of $v_1$ for different phase shift angles using nonlinear dopant drift model. (c). $R_{m1}$ -$R_{m2}$ after the positive half cycle of $v_1$ for different phase shift angles using nonlinear dopant drift model.**

## 4.3 Response of proposed phase detector basic structure for frequency difference

The same memristor based phase detector is examined to determine the sensitivity to frequency difference. In the case of $v_1$ and $v_2$ have different frequencies $f_1$and $f_2$ respectively and zero phase shift where $v_1 = \sin(\omega_1 t)$ and $v_2 = \cos(\omega_2 t)$, where $\omega_1 = 2\pi\omega f_1$, $T_1 = \frac{1}{f_1}$, $\omega_2 = 2\pi\omega f_2$, and $f_2 = f_1 + \Delta f$, the resistance of $R_{m1}$ after one positive half cycle of $v_1$is calculated using (1-7) to be

$$R_{m1}\left(\mathrm{t}=\frac{\mathrm{T}}{2}\right) = \sqrt{R_{init}^2 - 2kR_d\int_0^{\frac{T_1}{2}}\cos(\omega_2 t)\,dt} =$$

$$\sqrt{R_{init}^2 - \frac{2kR_d}{\omega_2}\sin\left(\omega_2\frac{T_1}{2}\right)} = \sqrt{R_{init}^2 - \frac{2kR_d}{\omega_2}\sin\left(\pi\frac{f_2}{f_1}\right)} =$$

$$\sqrt{R_{init}^2 - \frac{2kR_d}{\omega_2}\sin\left(\pi\frac{(f_1+\Delta f)}{f_1}\right)} = \sqrt{R_{init}^2 + \frac{2kR_d}{\omega_2}\sin\left(\pi\frac{\Delta f}{f_1}\right)}$$

$$\approx R_{init} + \frac{kR_d}{\omega_2 R_{init}}\sin\left(\pi\frac{\Delta f}{f_1}\right), \text{for } \frac{2kR_d}{\omega_2 R_{init}^2} \ll 1$$

$$\approx R_{init} + \frac{kR_d}{\omega_2 R_{init}}\left(\pi\frac{\Delta f}{f_1}\right), \quad \text{for } \Delta f \ll f_1 \qquad (4\text{-}4)$$

Similarly, $R_{m2}$, after one positive half cycle of $\mathrm{v}_1$is calculated using (1-7) to be

$$R_{m2}\left(\mathrm{t}=\frac{\mathrm{T}}{2}\right) = \sqrt{R_{init}^2 + 2kR_d\int_0^{\frac{T_1}{2}}\cos(\omega_2 t)\,dt}$$

$$\approx R_{init} - \frac{kR_d}{\omega_2 R_{init}}\left(\pi\frac{\Delta f}{f_1}\right), for\ \frac{2kR_d}{\omega_2 R_{init}^2} \ll 1 \text{ and } \Delta f \ll f_1 \qquad (4\text{-}5)$$

Therefore, from (4-4) and (4-5)

$$(R_{m1} - R_{m2})|_{t=\frac{T}{2}} \approx \frac{2kR_d}{\omega_2 R_{init}}\left(\pi\frac{\Delta f}{f_1}\right), \quad \text{for } \left(\frac{2kR_d}{\omega_2 R_{init}^2} \ll 1\right) \text{and } (\Delta f \ll f_1) \qquad (4\text{-}6)$$

It is obvious from (4-6) that the resistance difference between the memristors used in proposed structure $(R_{m1} - R_{m2})$ can be exploited to detect the shift in frequency between the two sinusoidal input signals as well.

The curves for $R_{m1}$, $R_{m2}$, and $(R_{m1} - R_{m2})$ at $t$=T/2 versus frequency shift, for zero phase shift angles, are drawn in Fig. 4-6 (a), (b), and (c) respectively using the linear dopant drift model and in Fig. 4-7 (a), (b), and (c) respectively using the nonlinear dopant drift model.

## 4.4 Modes of operation for the phase detector's memristors

Let us define the expression of the "programming stage", in the scope of the thesis, means the event of memristors variations due to applying a controlled sample of one signal ($v_2$) where the controlling is done by the other signal ($v_1$). According to the analytical results of section 4.2 and 4.3, the difference of the two memristors in the proposed phase detector structure can represent the phase or the frequency shift between the two signals. However, the resistance of the memristors should be converted to DC voltages to be subtracted then the result is used later as input for the VCO circuit. Therefore, the expression of the "reading stage" will describe the process of converting the memristance values to DC voltages. Moreover, the memristors should be returned to their initial values, after the reading stages, to be ready for reprogramming again at the beginning of each cycle of $v_1$. Hence the expression of the "initialization stage" will be applied for the process of returning the memristors to their initial values. In doing so, a controller unit is implemented using the Verilog-A to organize the flow of the programming, reading, and initialization stages. The timing of each stage during a cycle of $v_1$ is demonstrated in Fig. 4-8. The detailed explanation of the reading and initialization stages is found in next subsections.

### 4.4.1 Reading stage

In this stage the memristance value reached by applying $v_2$ on the two opposite aligned memristors, during the positive half cycle of $v_1$, are converted to two DC voltages. This conversion or reading process is carried out in the beginning of negative cycle half of $v_1$ as soon as finishing the programming stage. These two DC values are subtracted to provide the phase detector DC output which represents the phase or frequency shift between $v_1$ and $v_2$.

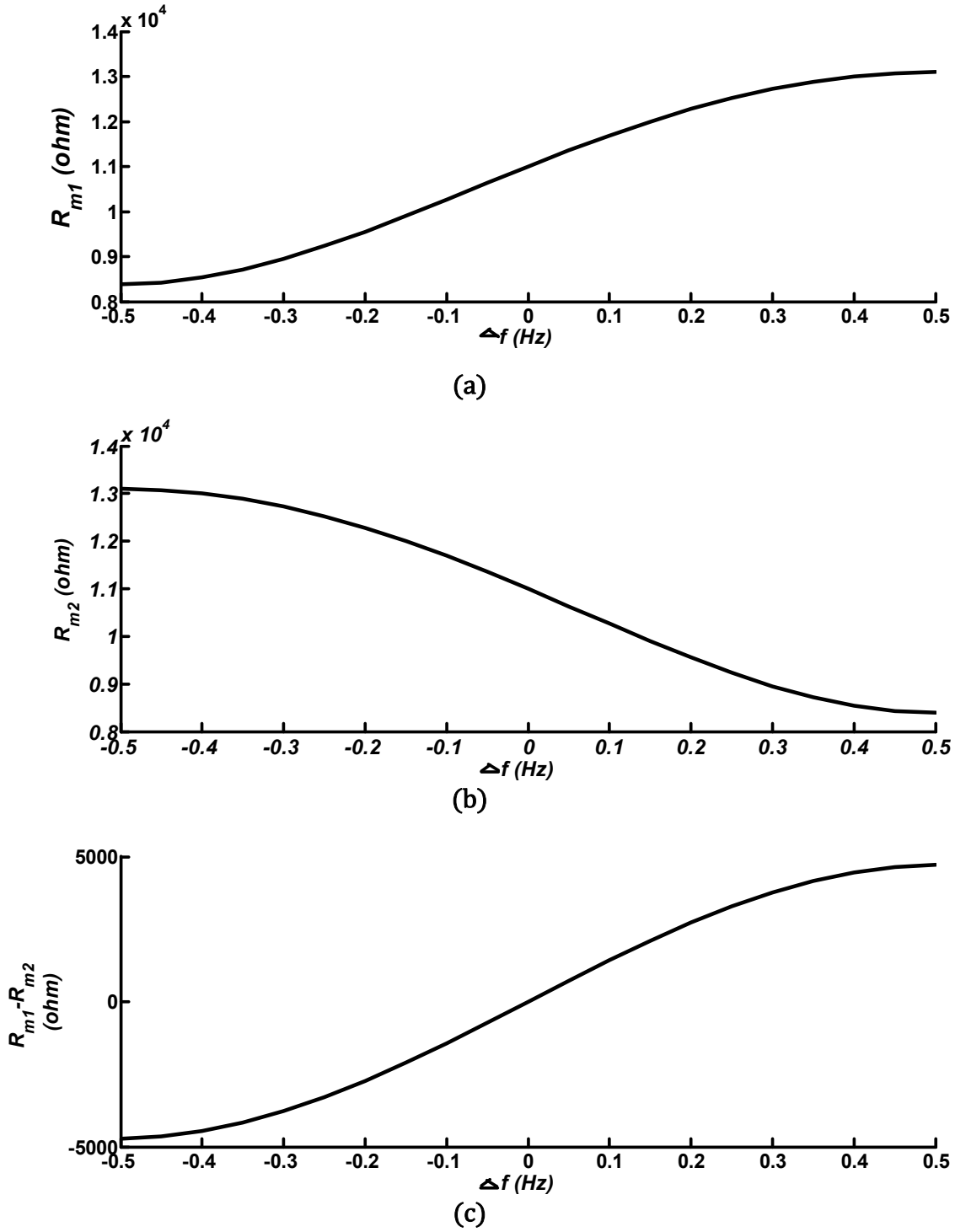
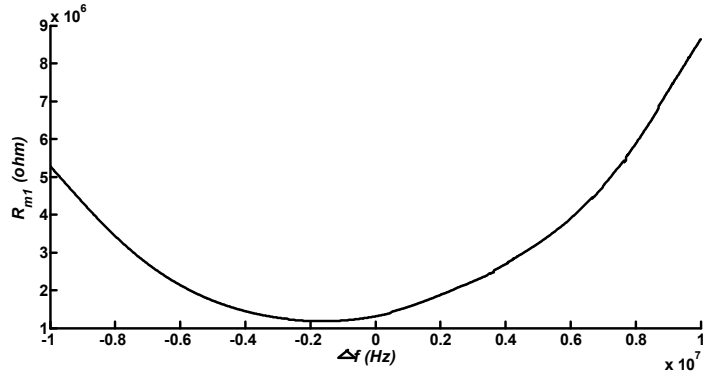
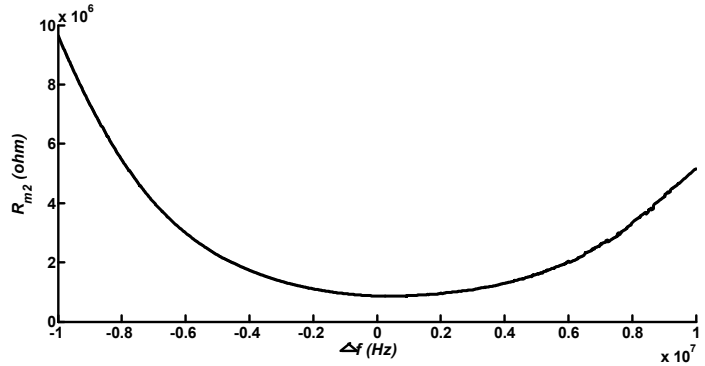


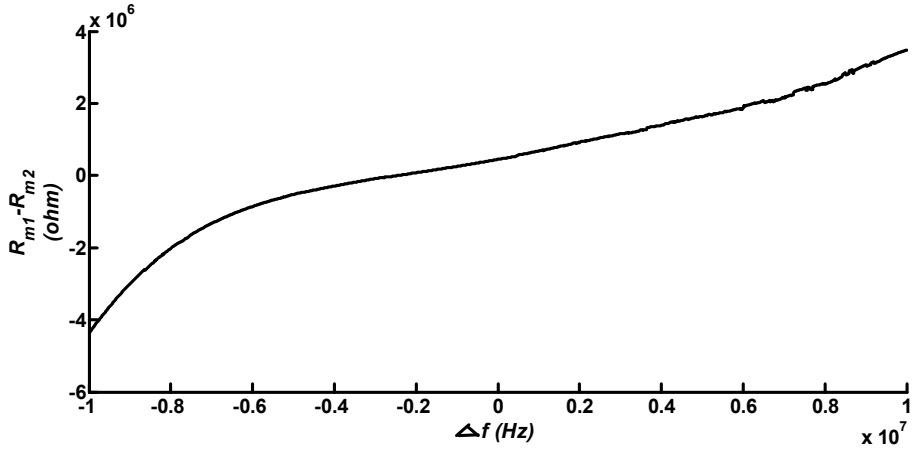

**Fig. 4-6 (a). $R_{m1}$ during the positive cycle half of $v_1$ for different frequency shift using the linear dopant drift model. (b). $R_{m2}$ during the positive cycle half of $v_1$ for different frequency shift using the linear dopant drift model. (c). $R_{m1}$ -$R_{m2}$ during the positive cycle half of $v_1$ for different frequency shift using the linear dopant drift model.**




(a)




(b)




(c)

**Fig. 4-7 (a). $R_{m1}$ during the positive cycle half of $v_1$ for different frequency shift using the nonlinear dopant drift model. (b). $R_{m2}$ during the positive cycle half of $v_1$ for different frequency shift using the nonlinear dopant drift model. (c). $R_{m1}$ -$R_{m2}$ during the positive cycle half of $v_1$ for different frequency shift using the nonlinear dopant drift model.**

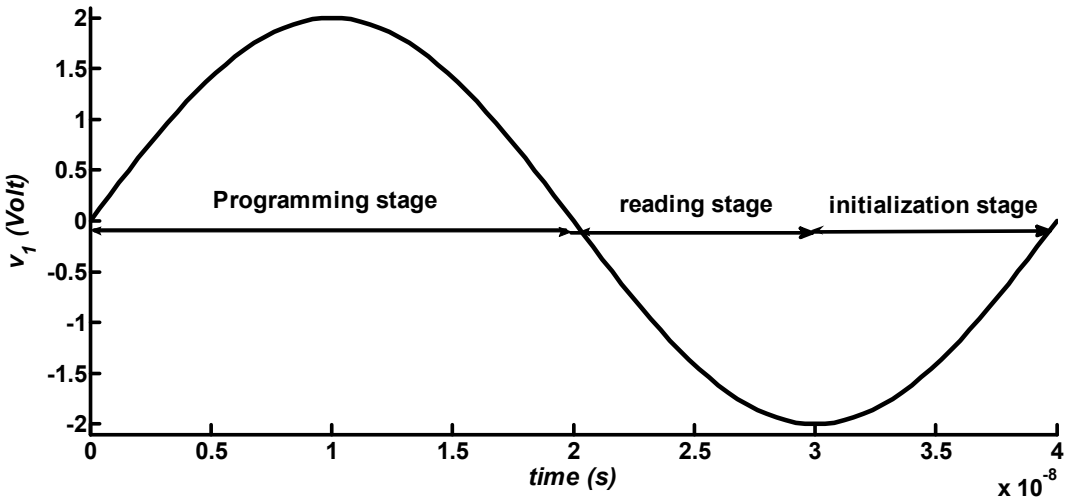



**Fig. 4-8. The timing of the programming, reading, and initialization stages during $v_1$cycle.**

The principle of voltage divider, with varying dividing ratio, is adopted as the reading technique. The schematic of reading circuit is shown in Fig. 4-9.

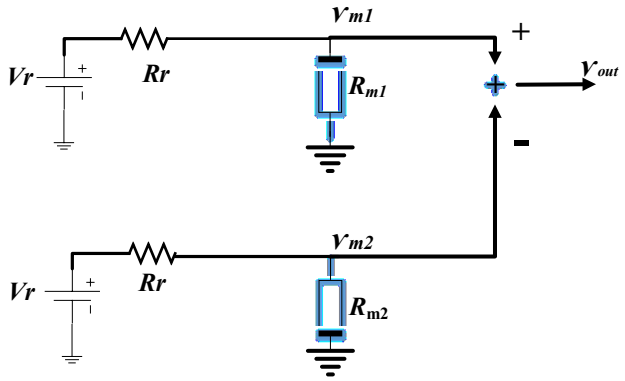



**Fig. 4-9. The schematic of the reading circuit.**

Where, $R_r$ is a series resistance and $V_r$ is the DC reading voltage which should be less than the threshold voltage of the used memristors to guarantee unchanging their values through the reading process. From Fig.4-9, $V_{m1}$ and $V_{m2}$ are the voltages across $R_{m1}$ and $R_{m2}$ respectively, and using the voltage divider concept, $V_{m1}$and $V_{m2}$ can be expressed as in (4-7) and (4-8) respectively. Finally, $V_{out}$=$V_{m1} - V_{m2}$ is the output of the reading process.

$$V_{m1} = V_r \cdot \frac{R_{m1}}{R_{m1}+R_r} \tag{4-7}$$

$$V_{m2} = V_r \cdot \frac{R_{m2}}{R_{m2}+R_r} \tag{4-8}$$

From (4-7), the maximum (minimum) of $V_{m1}$ value can be calculated by replacing $R_{m1}$by its maximum (minimum) value to be expressed as in (4-9) and (4-10) respectively.

$$max(V_{m1}) = V_r \cdot \frac{max(R_{m1})}{max(R_{m1})+R_r} \tag{4-9}$$

$$min(V_{m1}) = V_r \cdot \frac{min(R_{m1})}{min(R_{m1})+R_r} \tag{4-10}$$

Therefore, the dynamic range of $V_{m1}$can be evaluated by subtracted (4-9) and (4-10) as in (4-11)

$$\text{dynamic range}(V_{m1}) = \max(V_{m1}) - \min(V_{m1}) = V_r \cdot \frac{\max(R_{m1})}{\max(R_{m1})+R_r} - V_r \cdot \frac{\min(R_{m1})}{\min(R_{m1})+R_r} \tag{4-11}$$

Hence, the value of $R_r$ that satisfies the maximum dynamic range for $\mathrm{V_{m1}}$ can be derived using (4-12) to be expressed as in (4-13).

$$\frac{\partial \text{dynamic range}(V_{m1})}{\partial R_r} = 0 \tag{4-12}$$

$$R_r = \sqrt{\max(R_{m1})\min(R_{m1})} \tag{4-13}$$

Apparently, the value of $R_r$ that satisfies the max dynamic range for $V_{m1}$ is the approximately equal to which satisfies the max dynamic range for $V_{m2}$ where $\max(R_{m1})$ and $\min(R_{m1})$ are approximately equal to those for $R_{m2}$. It is foreseen that, the value of $(R_r)$ in (4-13) satisfies the max dynamic range for $V_{out}$, as well, where the change of $V_{m1}$ and $V_{m2}$, in the proposed structure, are always in opposite directions due to the opposite alignment of $R_{m1}$and $R_{m2}$. However, the maximum dynamic range of $V_{out}$ is not the only criteria for good performance, but also $V_{m1}, V_{m2}, \text{and } V_{out}$ should have same behaviour of $R_{m1}, R_{m2}, \text{and } R_{m1} - R_{m2}$ respectively to be good representations for them. In different words, $V_{m1}, V_{m2}, \text{and } V_{out}$ should have high degree of linearity with $R_{m1}, R_{m2}, \text{and } R_{m1} - R_{m2}$ respectively. Thereby, the condition of $R_r >> R_{m1}, R_{rm2}$ is the constraint for satisfying the result of $V_{m1} \alpha R_{m1}$, $V_{m2} \alpha R_{m2}$, and $V_{out} \alpha R_{m1}$-$R_{m2}$. Therefore in the proposed design, $R_r$ is selected to equal to $10 \cdot \sqrt{\max(R_{m1})\min(R_{m1})}$. Accordingly, using the selected value of $R_r$, the variation of $V_{m1}$with the phase shift is shown in Fig. 4-10 with the $R_{m1}$versus the phase shift in its inset. Similarly, $V_{m2}$ and $V_{out}$ versus the phase shift are drawn in Fig. 4-11, with $R_{m2}$ in its inset, and Fig. 4-12, with $R_{m1} - R_{m2}$ in its inset, respectively. Comparing each main curve by its inset in Fig. 4-10, Fig. 4-11, and Fig. 4-12, confirmes that $V_{m1}, V_{m2}, \text{and } V_{out}$ are very good representatives for $R_{m1}, R_{m2}, \text{and } R_{m1} - R_{m2}$ respectively and that the adopted approach is well worth considering. Additionally it is worth pointing out that, generating a DC signal proportional to the phase or the frequency shift between the two input signals of the phase detector circuit eliminates the need to

LPF block in the PLL system which optimizes the design from the power and the area point of views. Furthermore, circuit simulations using Cadence tool were performed to guarantee the performance validity for the programming and reading stages with replication the behavior of actual electronic devices. Fig. 4-13 shows the schematic used in the simulations, while Fig. 4-14 and 4-15 show the DC output voltage during the reading stage versus the phase and frequency respectively. Parametric simulations are utilized to run the simulations at different phase shift or different frequency shift values then averaging the resultant family curves to generate the curve between the output voltage versus the phase shift or versus the frequency shift. The results show direct proportionality between the DC output of the reading stage and the phase shift, between -80$^o$ to 80$^o$, and frequency shift, between –8MHz to 15MHz, with 25MHz as center frequency.

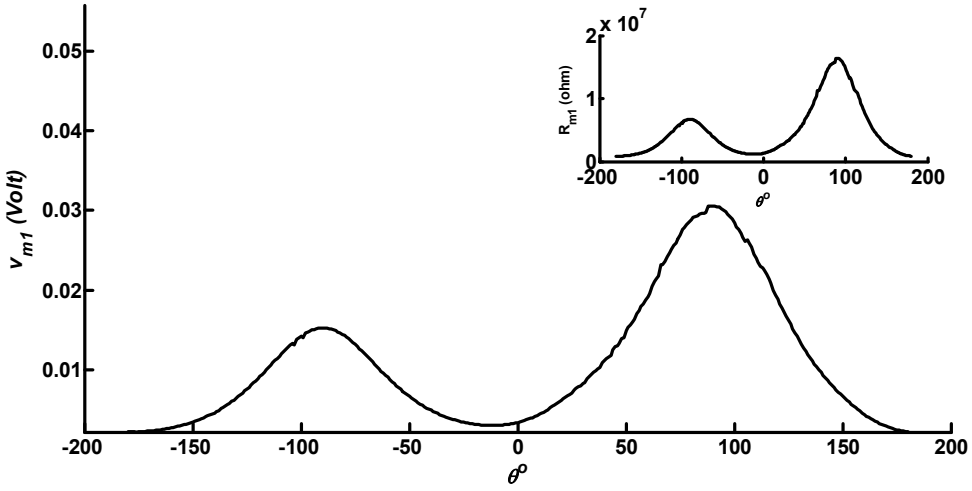



**Fig. 4-10. $V_{m1}$ versus the phase shift and $R_{m1}$ versus the phase shift in the inset**

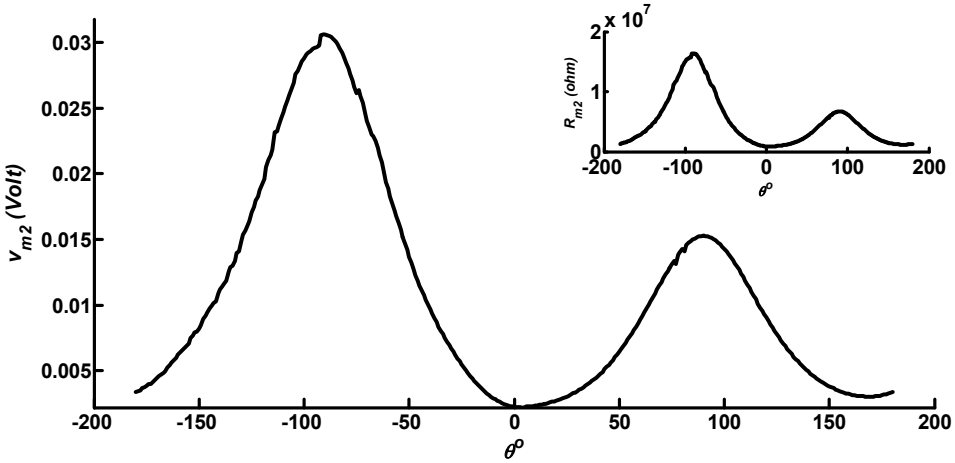



**Fig. 4-11. $V_{m2}$ versus the phase shift and $R_{m2}$ versus the phase shift in the inset**

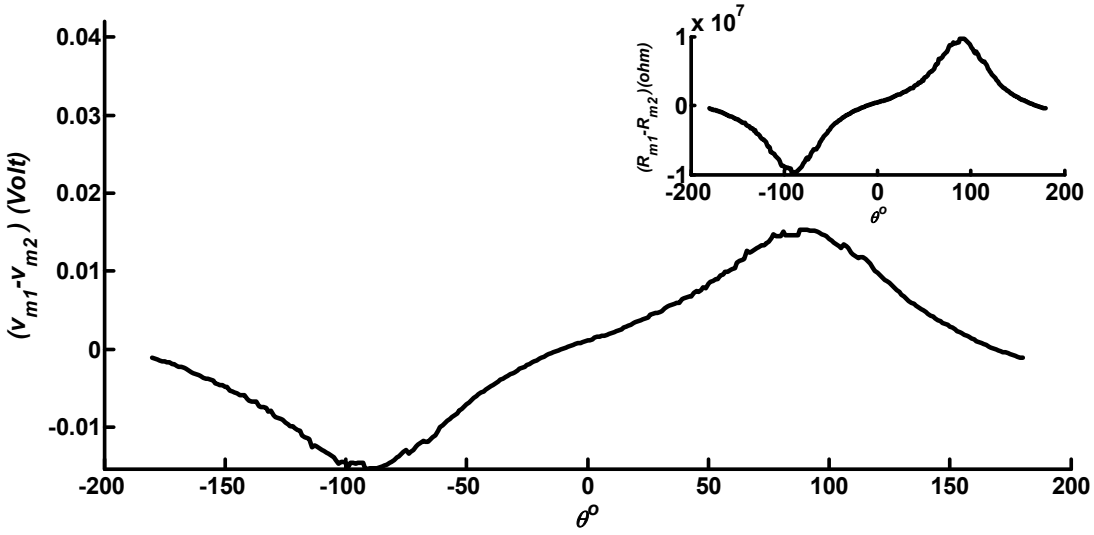



**Fig. 4-12. $V_{out}$ versus the phase shift and $R_{m1} - R_{m2}$ versus the phase shift in the inset.**

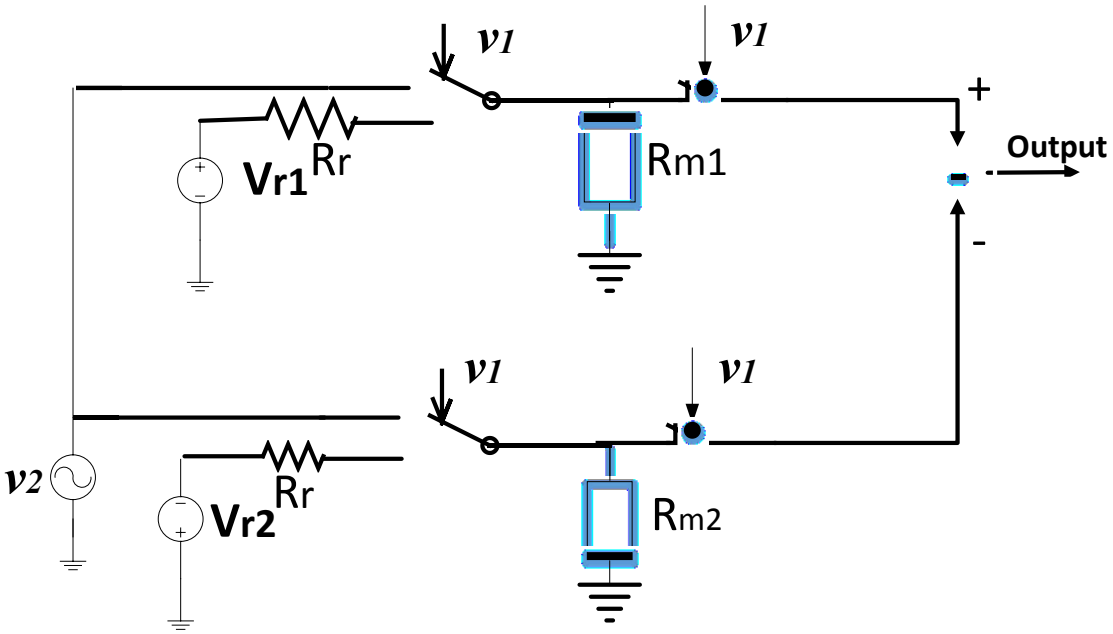
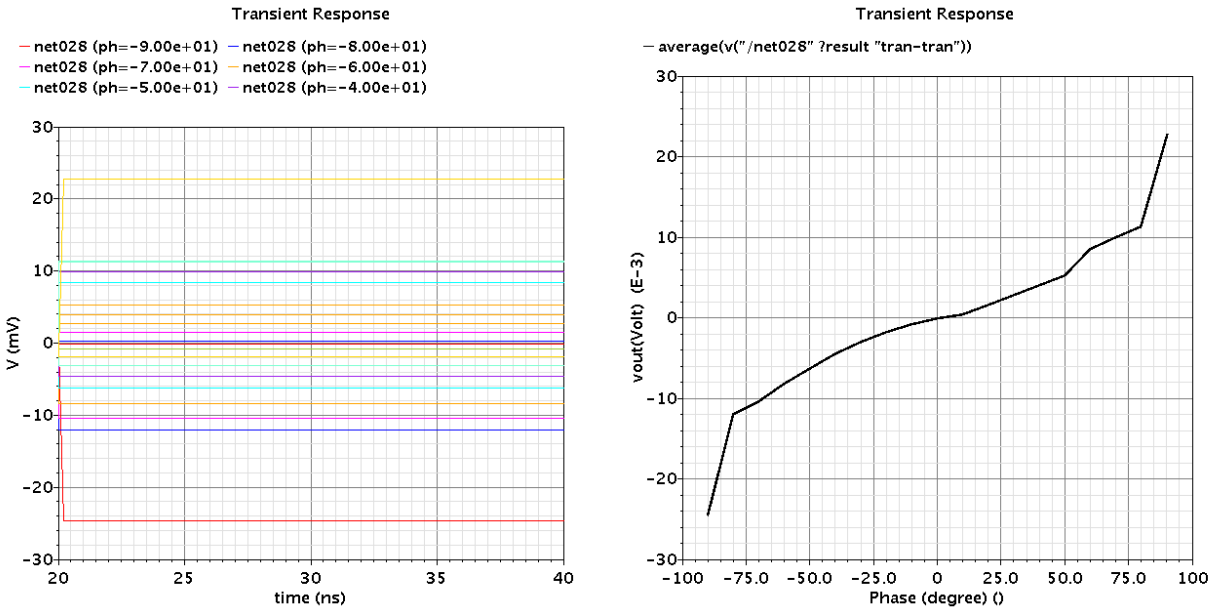
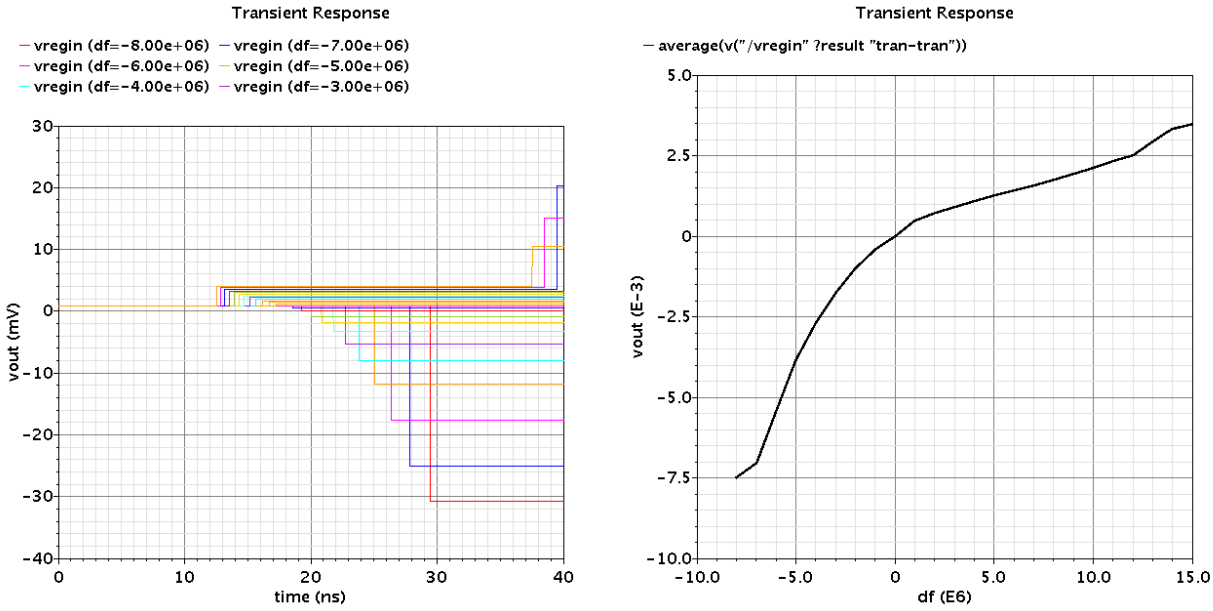



**Fig. 4-13. Phase detector used for circuit simulations including the programming and reading stages.**




(a) (b)

**Fig. 4-14 (a). The parametric simulation during the reading stage for different phase shift values (b). The simulated DC output versus the phase shift.**




(a) (b)

**Fig. 4-15 (a). The parametric simulation during the reading stage for different frequency shift values (b). The simulated DC output versus the frequency shift.**

## 4.4.2 Initialization stage

The initialization stage is necessary for the proposed phase detector in order to operate as a part of PLL or any closed loop system. At this stage, the two memristors used in the proposed phase detector should be reset again to their initial states for next cycle. The initialization process should push the memristors state to the initial value. For avoiding complex circuits, the two memristors are chosen to have same initial state value and for more simplicity, it is preferred to be at one of the two boundaries $w = 0.95$ or $w = 0.05$ [26]. Maximum initialization time, $t_{init}$, is chosen to be one fourth of the cycle period for a signal at the maximum predicted input frequency. The initialization is performed by applying DC input signal that pushes the memristor state value to the initial boundary [82], [83]. Therefore, Matlab simulations were carried out for determining which boundary has better performance, larger output dynamic range, and the maximum adequate DC voltage, and for determining $V_{init}$ value, the DC voltage needed for the initialization process. Noting that, the maximum adequate DC voltage is the voltage needed to drive the memristor state to the initial state value from its opposite boundary value. The simulations revealed that the larger dynamic range is satisfied when initial state value, $w_{init}$, equals 0.95. Additionally, the DC voltage required to initialize $R_{m1}$ is 2.1V while -2.1V is needed to initialize $R_{m2}$ due to its opposite alignment. Finally, the Matlab code used to evaluate $V_{init}$ is listed in Appendix-B also the relationship between the applied DC input voltage and the reached memristor state value after 10ns is presented in Fig. 4-16.

## 4.5 controller unit

A controller unit is needed to manage the sequence of the programming, reading, and initialization stages of the proposed phase detector circuit. The block diagram of the suggested controller unit is shown in Fig. 4-17. Additionally, the controller input and output terminals are defined in Table 4-3. Also, its flowchart is depicted in Fig.4-18.

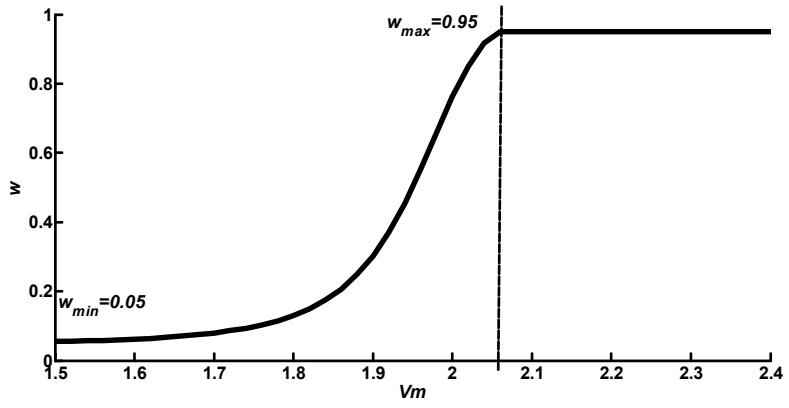



**Fig. 4-16. The reached memristor state value, $w$, after apply the DC voltage, $V_m$, for 10ns.**

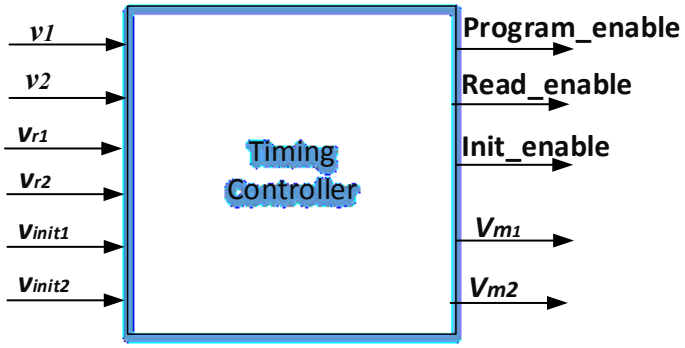



**Fig. 4-17. The block diagram of the controller unit.**

**Table 4.3. The terminals definition of the suggested controller unit.**

| terminal | direction | definition |
|---|---|---|
| $v_1$ | input | phase detector first AC input signal |
| $v_2$ | input | phase detector second AC input signal |
| $V_{r1}$ | input | DC first memristor reading signal |
| $V_{r2}$ | input | DC second memristor reading signal |
| $V_{init\,1}$ | input | DC first memristor initializing signal |
| $V_{init\,2}$ | input | DC second memristor initializing signal |
| $V_{m1}$ | output | voltage to be applied on the first memristor |
| $V_{m2}$ | output | voltage to be applied on the second memristor |
| Prog_enable | output | flag for the programming stage |
| Read_enable | output | flag for the reading stage |
| Init_enable | output | flag for the initializing stage |

Accordingly, the Verilog-A hardware description language is used for the controller implementation and its Verilog-A code is provided in Appendix-A. Briefly, the controller detects the positive cycle half of the reference signal, $v_1$, at this time the other phase detector input, $v_2$, is applied to program the two opposite aligned memristors and the program_enable flag is set on and other flags off. Then when the negative cycle half of $v_1$starts, the controller applies the reading DC voltage, $V_{r1}$, with a reading series resistance, $R_r$, to the first memristor, $R_{m1}$as previously explained in the reading stage subsection. Similarly, the reading DC voltage, $V_{r2}$, with a reading series resistance, $R_r$, is applied to the second memristor, $R_{m2}$. Noting that $V_{r1}$ and $V_{r2}$ are two equal DC voltages with a value less than the memristors threshold voltage and the controller sets the read_enable flag on and other flags off during the reading process. Finally after finishing the reading stage, the controller applies the initialization DC sources, $V_{init\,1}$ and $V_{init\,2}$ to, $R_{m1}$and $R_{m2}$respectively with setting the init_enable flag on and other flags off. The controller unit replaced the switches used in Fig. 4-13 and the schematic of the proposed phase frequency detector becomes as shown in Fig. 4-19. It is worth to note that, the flags

signals out from the phase detector controller unit can be used for switching the other PLL blocks ON and OFF, in case of the PLLs with non-continuous operation architecture as demonstrated in Chapter 5. These non-continuous architectures allow decreasing the phase noise and power consumption, more details about the PLLs with non-continuous operation architecture can be found in [87]. It is expected that the needed hardware to realize the suggested controlling circuit is mostly consists of a comparator or a zero crossing circuit, a slope polarity detector and some transmission gates. A comparator is needed to convert the received sinusoidal reference signal to the square waveform hence differentiating between its positive and negative half cycle. A slope polarity detector may be required to distinguish between the third and the fourth quarters of the incoming reference signal which are the timing of the reading and initialization stages respectively. While, the transmission gates will act as sinusoidal AC switching circuits to select the appropriate input at the memristors terminals according to the operation stage. In this case, the controlling circuit will not represent a huge overhead on the PFD simple architecture and small area.

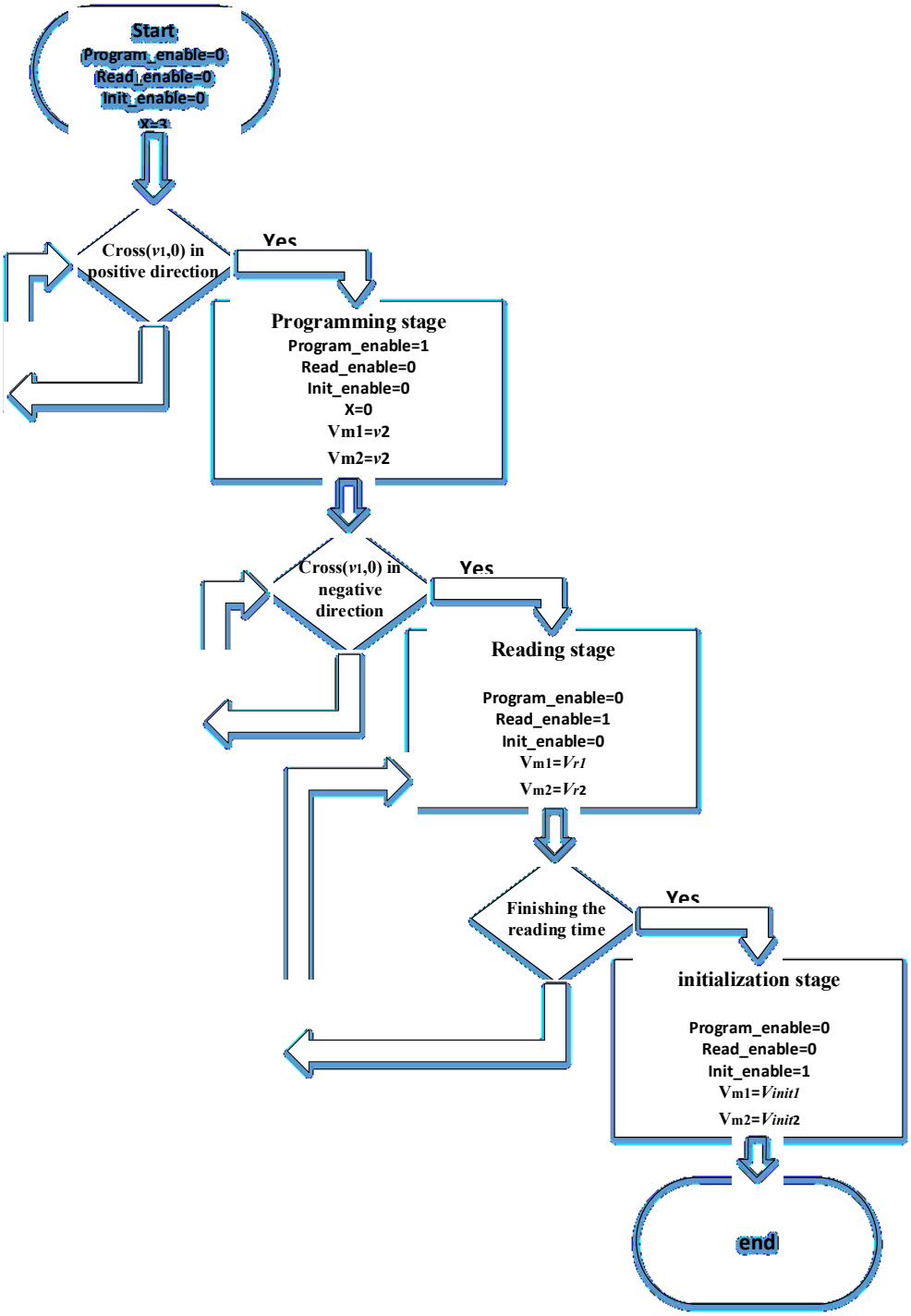



**Fig. 4-18. The flowchart of the controller unit.**

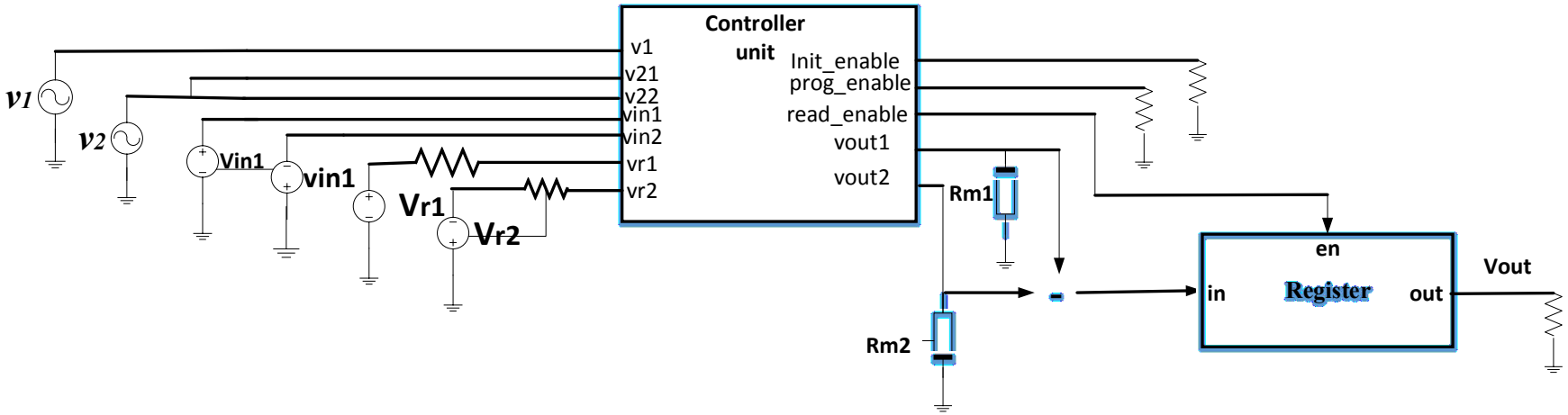



**Fig. 4-19. The phase frequency detector schematic after adding the controller unit.**

# Chapter Five

# A MEMRISTOR BASED VCO AND A NOVEL MEMRISTOR BASED SWITCHING MODE PLL SYSTEM

## *5.1 A memristor based VCO using a single dual current output OTA*

The voltage controlled oscillator (VCO) is an electronic oscillator whose instantaneous oscillation frequency is controlled by the applied input voltage. Consequently, a VCO can be used for Phase Modulation (PM) or Frequency Modulation (FM). A VCO is also an essential part of phase-locked loop (PLL) systems. VCOs can be usually classified into two categories based on the type of waveform created. The first category is the relaxation oscillators that generate a non-sinusoidal repetitive output signal, such as square, sawtooth or triangular waveforms. The second category is the harmonic or linear oscillators that produce a sinusoidal waveform. Harmonic oscillators generally consist of a resonator together with an amplifier. The amplifier compensates the resonator losses to prevent the amplitude from decaying. Besides it separates the load from the resonator hence the load does not influence the resonator. Some instances of harmonic oscillators are LC oscillators, crystal oscillators, and RC oscillator [88]. Many memristor-based relaxation oscillators were presented [89]–[93]. Also, it was demonstrated in [94] that, though the system poles oscillate in the memristor based oscillators, sustained oscillation is maintained due to the memristors properties. However till now, little effort was devoted to exploiting the memristor benefits in implementing memristor-based sinusoidal oscillators. In the previously introduced memristor-based sinusoidal oscillators, memristors were used to replace resistors in phase shift and Wien oscillators only [95], [96]. The amplifiers used in these publications were Operational Amplifiers (Op Amps) which, in general, limit the oscillation to 1MHz. Moreover, these publications neglected the dependence of the oscillation condition on the memristance value. This dependence means the necessity of replacing the other circuit elements values, to satisfy the oscillation condition, with each change in memristance value for obtaining adaptive oscillation frequency.

In this chapter, a sinusoidal oscillator using a single OTA (Operational Transconductance Amplifier) with dual current output [97] is adopted to be converted to a memristor based VCO. The design starts from replacing the single resistor in the design published in [97] by a memristor element. Hence, the schematic of the proposed circuit becomes as shown in Fig. 5-1.

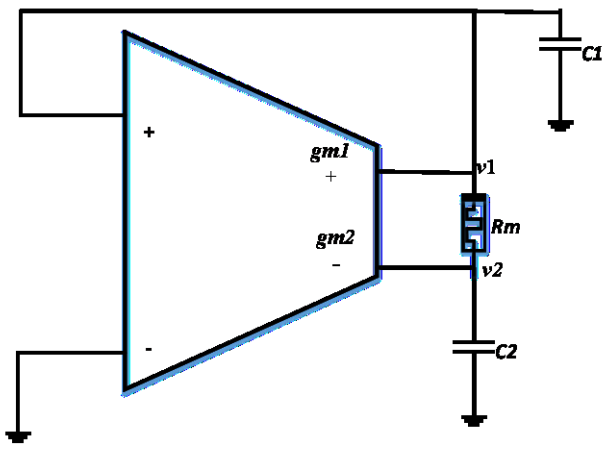



**Fig. 5-1. The schematic of the proposed memristor based VCO using a single dual current output OTA.**

### 5.1.1 Circuit illustration

The state matrix that can generally describe a second-order oscillator is expressed as

$$\begin{bmatrix} \frac{dV_1}{dt} \\ \frac{dV_2}{dt} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{5-1}$$

From (5-1), the characteristic equation is derived to be as in (5-2)

$$s^2 - (a_{11} + a_{22})s + (a_{11}a_{22} - a_{12}a_{21}) = 0, \tag{5-2}$$

so, the condition of oscillation (CO) and frequency of oscillation (FO) are extracted as in (5-3) and (5-4) respectively [97].

$$\text{CO: } a_{11} + a_{22} = 0 \tag{5-3}$$

$$\text{FO: } f_{out} = \frac{1}{2\pi}\sqrt{a_{11}a_{22} - a_{12}a_{21}} \tag{5-4}$$

Considering the schematic in Fig. 5-1, assuming an ideal opposite direction dual current output OTA with transconductance gains $g_{m1}$ and $g_{m2}$, plus output current $I_o^+ = g_{m1}(V_+ - V_-)$ and minus output current $I_o^- = g_{m2}(V_- - V_+)$, then writing the Kirchhoff's current law equations at the OTA output current nodes leads to the state matrix of the proposed VCO as presented in (5-5).

$$\begin{bmatrix} \frac{dV_1}{dt} \\ \frac{dV_2}{dt} \end{bmatrix} = \begin{bmatrix} \frac{g_{m1}}{c_1} - \frac{1}{R_m c_1} & \frac{1}{R_m c_1} \\ \frac{1}{R_m c_2} - \frac{g_{m2}}{c_2} & -\frac{1}{R_m c_2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{5-5}$$

From (5-3) and (5-5), the condition of oscillation for the proposed VCO is as expressed in (5-6)

$$\text{CO: } g_{m1}c_2 = \frac{c_1+c_2}{R_m} \quad , \tag{5-6}$$

,and from (5-4) and (5-5), the frequency of oscillation is as expressed in (5-7)

$$\text{FO: } f_{out} = \frac{1}{2\pi}\sqrt{\frac{g_{m2}-g_{m1}}{R_m c_1 c_2}} \tag{5-7}$$

### 5.1.2 Circuit analysis

The proposed circuit includes a single dual current output OTA and only four passive components (two memristor and two capacitors) as clear in Fig. 5-1. The two used capacitors in this oscillator circuit are grounded and it is preferred for integration. Moreover, the model of the transconductance amplifier that used in the simulation of the original circuit is the LT1228 OTA (Linear-Tech Company) model [97]. The LT1228 OTA is a commercially available fast transconductance amplifier with 75MHz bandwidth, which is very suitable for being used in designing the proposed VCO that operates in the range between 20 and 30MHz with center frequency equals 25MHz. The transconductances gains $g_{m1}$ and $g_{m2}$ are adjusted by the bias currents of the OTA model, where $g_{m1} = 10 * I_{bm1}$ and $g_{m2} = 10 * I_{bm2}$ for the LT1228 model. Besides, the frequency of oscillation is function in the memristor resistance, as obvious from (5-7), hence this oscillator is appropriate for being the base for a memristance tuning VCO, in which the output frequency is controlled by programming its memristor element using the VCO input DC voltage. However, the condition of oscillation for a memristance tuning VCO should not be dependent on the adapted parameter (the memristance value) which is not satisfied in the original oscillator, as clear from (5-6). Therefore, Resistance Controlled Gain (RCG) property of the OTA is used with its first transconductance gain , $g_{m1}$, as illustrated in Fig. 5-2 [98].

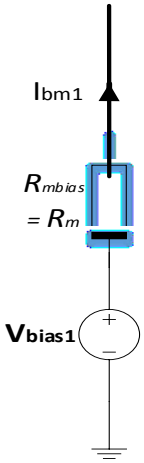



**Fig. 5-2. Setting of the OTA first bias current for obtaining a memristance controlled transconductance gain.**

This is done by setting the first bias current, $I_{bm1}$, to be varied with the memristance value using additional DC source, $V_{bias1}$, and additional memristor, $R_{mbias}$. The additional memristor is located between $V_{bias1}$ and the pin 6 (iset) of the LT1228 chip [98] and equals to the oscillator main memristor, which is shown in Fig 5-1. It is worth pointing out that the voltage drop on the additional memristor, ($V_{bias1}$ − voltage of pin 6) should remain in the range of the memristor threshold voltage to avoid changing the memristor value during the operation of the VCO. Also, the selected value of $V_{bias1}$ should guarantee that $g_{m1}$ will be in its allowable range, between 10$\Omega S$ and 10 mS [98], for the expected operating range of $R_m$. Hence, in the proposed design, $V_{bias1}$ is chosen to equal -3.5426V, (0.2V+ voltage of pin 6), which has a negligible effect on $R_{mbias}$. Thereby, the modified values for $I_{bm1}$ and $g_{m1}$ becomes $\frac{0.2}{R_m}$ and $\frac{2}{R_m}$ respectively. Additionally, the condition of oscillation is modified to be as expressed in (5-8) which is independent on the memristance value and the frequency of oscillations becomes as represented in (5-9).

$$\text{CO: } c_1 = c_2 = c \tag{5-8}$$

$$FO: f_{out} = \frac{1}{2\pi c}\sqrt{\frac{g_{m2} - \frac{2}{R_m}}{R_m}} \tag{5-9}$$

Apparently from (5-8) and (5-9), the proposed VCO has separate control of the oscillation condition and frequency oscillation.

### 5.1.3 Circuit simulation

The LT1228 OTA SPICE netlist model is used in all simulations of the proposed VCO using Cadence simulation environment and it is provided in Appendix-C. In the simulation, the dual current output OTA is constructed using two single-ended OTAs in parallel connections as shown in Fig. 5.3.

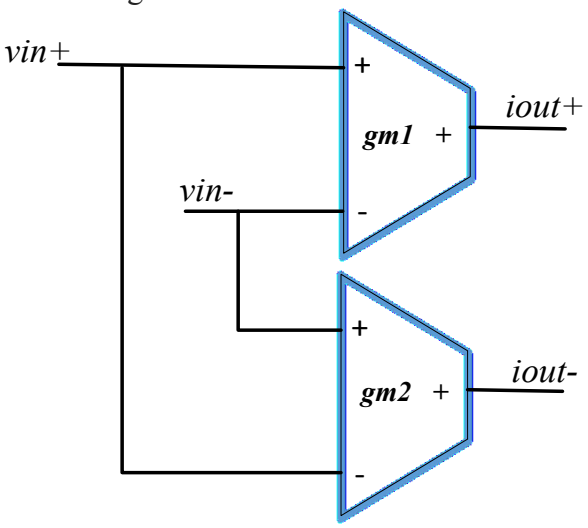



**Fig. 5-3. The parallel connection of two single output OTA to form an opposite directions dual output OTA.**

The values of the parameters used for designing the memristor based VCO circuit and used during the circuit simulations are listed in Table 5-1.

The simulation schematic of the proposed memristor based VCO via Cadence simulation tool is shown in Fig. 5-4 while the simulated output is shown in Fig. 5-5 and Fig. 5-6. The output sinusoidal signal shown in Fig. 5-5 has a cycle time equals 0.04μs which corresponding to 25MHz output frequency, this result is obtained using memristance at 3.2958KΩ. Fig. 5-6 shows the simulated output signal at 28MHz in time and frequency domains. The Fourier spectrum of the VCO output signal is generated to illustrate the signal in frequency domain. The Fourier spectrum shows a fundamental component at 28MHz with 16.9 dB greater level than the harmonic components.

**Table 5.1 The parameter values used for designing and simulation the proposed memristor based VCO.**

| parameter | definition | value |
|---|---|---|
| $V^+$ | Positive supply voltage | 5V |
| $V^-$ | negative supply voltage | -5V |
| $c_1$ | The first capacitance | 2pf |
| $c_2$ | The second capacitance | 2pf |
| $I_{bm1}$ | The set or bias current of the positive single-ended OTA | $\frac{0.2\text{V}}{R_m}$ |
| $I_{bm2}$ | The set or bias current of the negative single-ended OTA | 1mA |
| $g_{m1}$ | The transconductance gain of the positive single-ended OTA | $\frac{2}{R_m}$ |
| $g_{m2}$ | The transconductance gain of the negative single-ended OTA | 10mS |

From (5-9) the value of the memristance required for the VCO generates a sinusoidal signal with frequency $f_{out}$ can be extracted by solving the following second order binomial equation,

$$R_m^2 - \frac{g_{m2}}{(2\pi c f_{out})^2} R_m + \frac{2}{(2\pi c f_{out})^2} = 0. \quad (5\text{-}10)$$

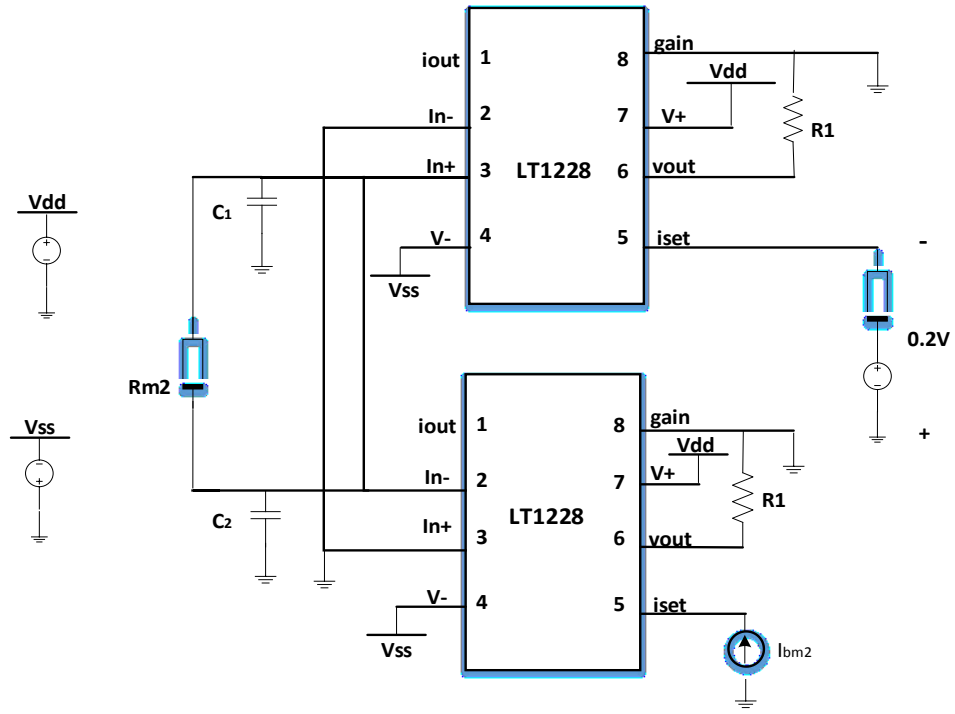



**Fig. 5-4. The simulation schematic of the proposed VCO in Cadence simulation environment.**

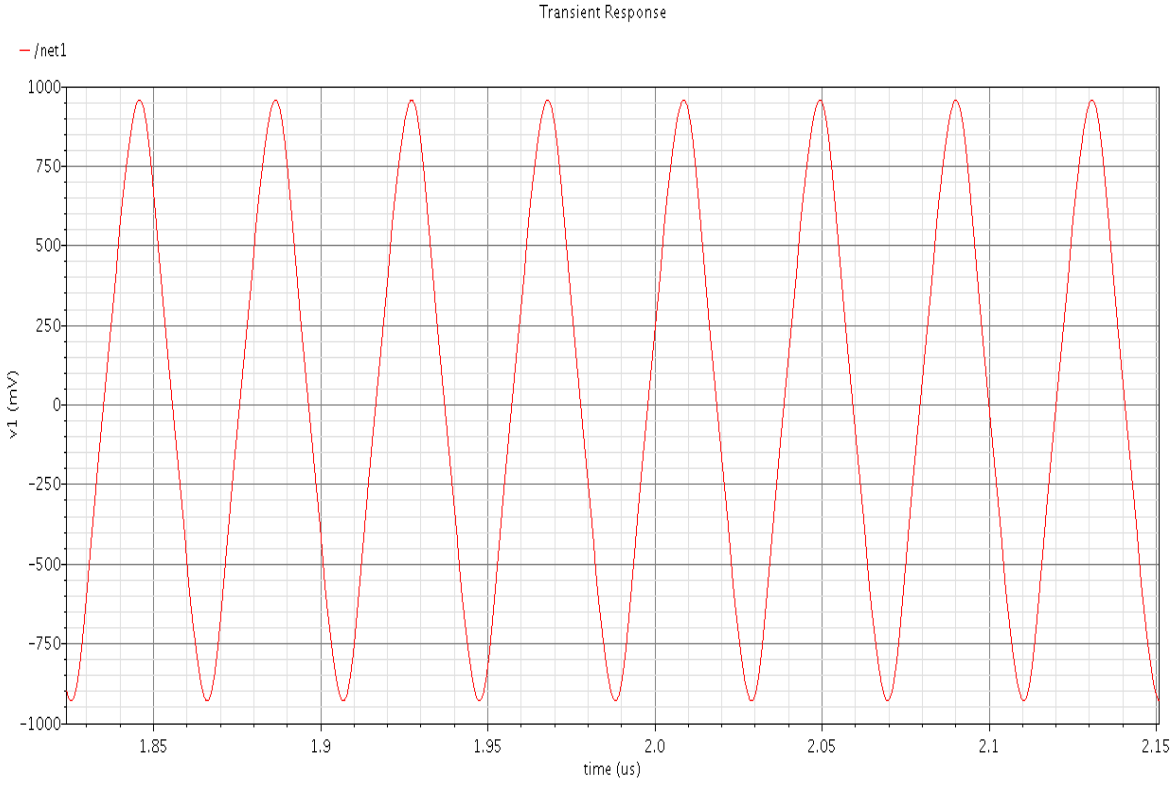



**Fig. 5-5. The simulated output waveform with $f_{out}$ =25MHz using $R_m$=3.2958KΩ.**

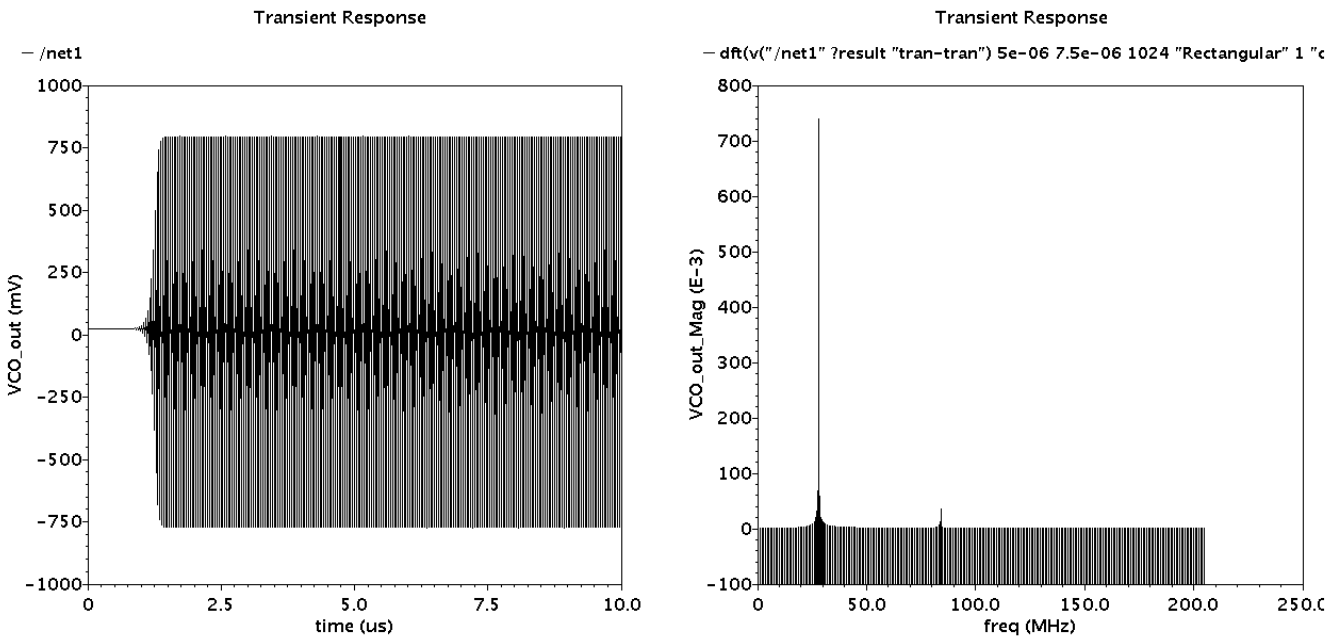



**Fig. 5-6. The simulated output waveform with $f_{out}$ =28MHz in time and frequency domains.**

The memristance values for generating a sinusoidal signal with frequency between 20 and 30MHz are obtained analytically using (5-10) and listed in Table 5-2. However, the memristance values obtained from the circuit simulation for the same range of frequencies are listed in Table 5-3 which deviated about the analytical results that assumed ideal dual current output OTA. A comparison between the analytical and simulated memristance values is shown in Fig.5-7. Here, we modified one of the nonlinear model fitting parameters (b) to give this relatively small memristance range (*KΩ instead of *MΩ). Giving that, this nonlinear model [26] is highly parameterized and has the flexibility to modify its parameters in accordance with the material properties. This parameters adjustment is justified by testing the main memristor devices fingerprint which is the pinched hysteresis I-V characteristic that is shown in Fig.5-8.

It is worth pointing out that, the two memristors needed in this circuit should pass usually through three stages in sequence. The first one is programming by the VCO DC input, the second one is operating in the VCO circuit to produce an output signal with frequency $f_{out}$, while the third one is resetting its memristance for retrieving its initial value and be ready for reprogrammed using new VCO DC input.

**Table 5-2 The analytical memristance values for generating a sinusoidal signal with frequency between 20 and 30MHz.**

| $f_{out}$ (MHz) | $R_m$ (KΩ) |
|---|---|
| 20 | 6.1258 |
| 21 | 5.563 |
| 22 | 5.0252 |
| 23 | 4.5792 |
| 24 | 4.1876 |
| 25 | 3.4819 |
| 26 | 3.5351 |
| 27 | 3.2616 |
| 28 | 3.0167 |
| 29 | 2.7965 |
| 30 | 2.5978 |

**Table 5-3 The simulated memristance values for generating a sinusoidal signal with frequency between 20 and 30MHz.**

| $f_{out}$ (MHz) | $R_m$ (KΩ) |
|---|---|
| 20 | 6.1558 |
| 21 | 5.5258 |
| 22 | 4.685 |
| 23 | 4.142 |
| 24 | 3.685 |
| 25 | 3.2958 |
| 26 | 2.96 |
| 27 | 2.675 |
| 28 | 2.428 |
| 29 | 2.2072 |
| 30 | 2.0152 |

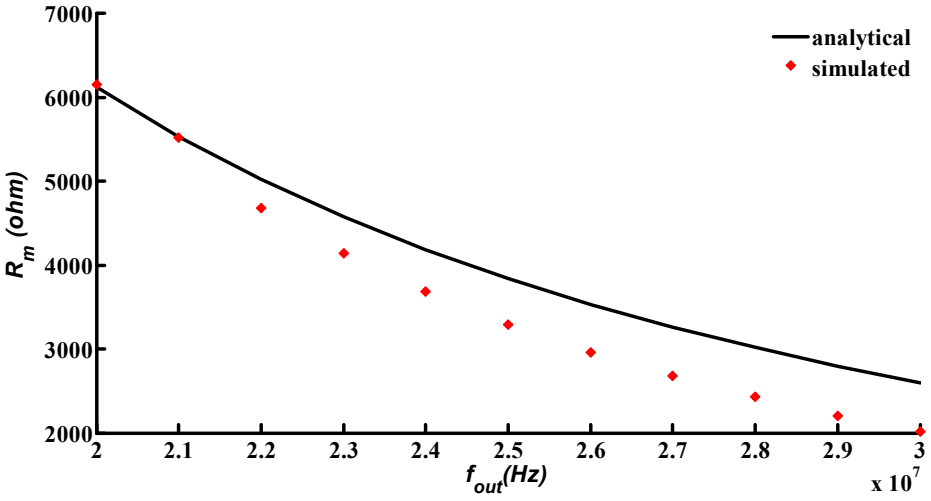



**Fig. 5-7. Comparison between the analytical and the simulated memristance values needed for generating an output signal with frequency between 20 and 30MHz.**

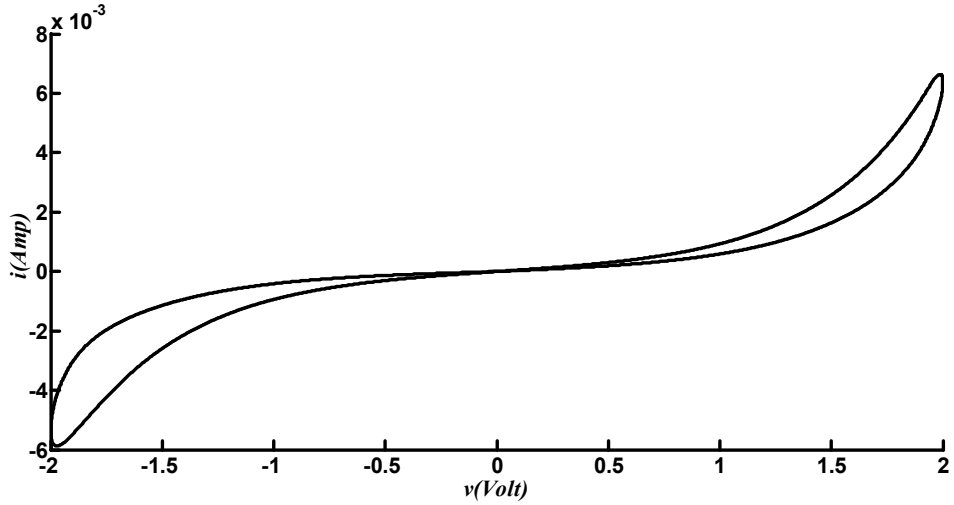



**Fig. 5-8. The I-V characteristic of the parameters modified nonlinear model with b= 30.5e3 and other parameters are same as those values used in [26] .**

## *5.2 A memristor based switching mode PLL system*

### 5.2.1 PLL basic concept

A PLL is a circuit that makes one signal to follow another one. It maintains the output signal synchronizing with the input reference signal in phase as well as in frequency. In more details, PLL manages the phase of its output signal such as the phase error between the reference signal phase and the output signal phase diminishes to a minimum. PLLs are commonly utilized in telecommunications, computers, radio and

other electronic applications. Wherein, they can be used to retrieve a signal from a noisy channel, demodulate a signal, or as frequency synthesis (produce a stable frequency at multiples of the input frequency). As one integrated circuit can present a whole PLL building block, the system is extensively exploited in modern electronic devices [99].

The conventional block diagram of a PLL system is illustrated in Fig. 5-9. It comprises a phase detector, a loop filter, and a voltage controlled oscillator circuits [86]. The key to the operation of a PLL is the phase difference between two signals (the reference input signal ($v_1$) and the feedback signal ($v_2$)) and the ability to detect it. The information about the phase difference between the two signals is then used to control the frequency of the loop. In doing so, the reference signal and the signal from the VCO connected to the two input ports of the phase detector. Here the phase of the two signals is compared and a resulting difference or error voltage is produced. This corresponds to the phase difference between the two signals. In the basic PLL, the output from the phase detector, which contains DC and high frequency components, is passed to the loop filter to remove any high frequency elements and then filtered signal is applied to the voltage controlled oscillator as its tuning voltage.

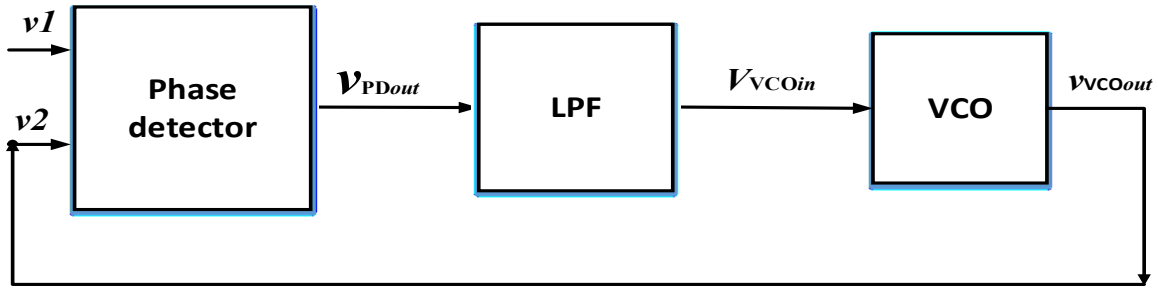



**Fig. 5-9. Conventional block diagram of a PLL system.**

Initially the loop will be out of lock, and then the error voltage will pull the frequency of the VCO output signal towards that of the reference signal, until it cannot reduce the error any further and the loop is locked.

### 5.2.2 Basic structure and applications of the proposed memristor based switching mode PLL system

The proposed memristor based PLL system consists of the memristor based phase frequency detector, pre-proposed in Chapter 4, cascaded by the proposed memristor based voltage controlled oscillator. Unlike the traditional phase detectors, the proposed phase detector produces a pure DC signal. Therefore, there is no need for any circuit in the PLL to get rid of the high frequency components of the PFD output. The distinction of the proposed PLL system is eliminating the need to low pass filter hence, decreasing the associated overhead in the other traditional PLL systems which make it appropriate for small area and low power applications. Moreover, the proposed memristor based PLL operates in noncontinuous approach which reduces the phase noise and over reduces the

dissipated power as explained latter. The basic block diagram of the proposed memristor based PLL system is shown in Fig.5-10.

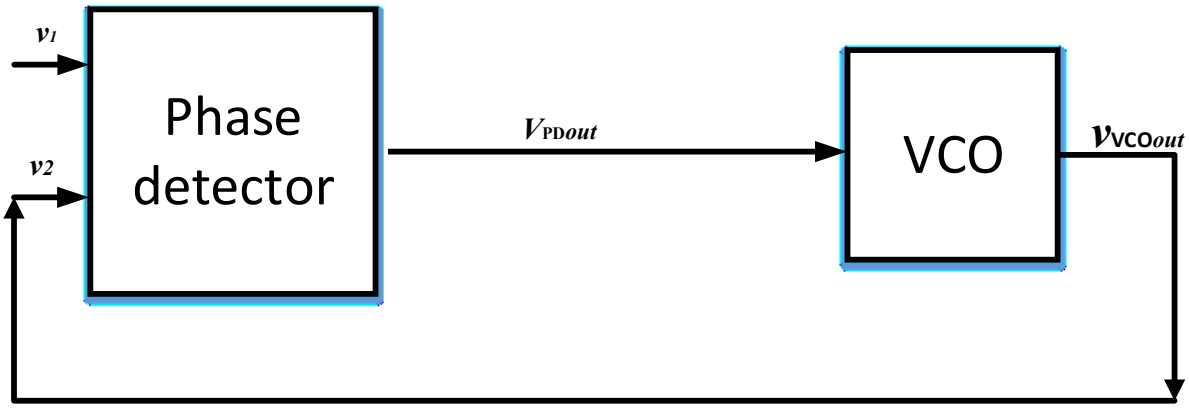



**Fig. 5-10. Basic block diagram of the proposed memristor based PLL system.**

The proposed memristor based PLL system has been tested in frequency range between 20 and 30MHz. This frequency range is needed for some important biomedical applications like measuring of blood flow in the retina and in the CO2 sensors [100]. Also, it is used in realizing a real-time detection circuit for Doppler optical coherence tomography [101] and generally in implantable medical sensors[87].

### 5.2.3 The operation of the memristor based switching mode PLL system

Both the memristor based phase detector and the memristor based VCO operate in three different stages during one cycle of the reference signal due to the need of their memristors for programming and reinitialized as mentioned before.

Fig.5-11 demonstrates the timing scheme for both the PD and the VCO while being integrated to form PLL system. During stage1, the positive half cycle of the reference signal, the VCO is in operation mode using its programmed memristors for producing the feedback signal and at the same time, the PD memristors are programmed using the feedback signal. While during stage 2 the PD memristors are read, its output is registered, and the VCO memristors are initialized. Finally, during stage 3 the VCO memristors are programmed by the registered DC output of the PD to be ready for the next VCO operation stage. It is worth noting that, the timing controller unit of the proposed phase detector, pre-illustrated in Section 4.5, can be used also after few modifications to timing control the VCO operation without the need to additional overhead. Simply, the needed modifications are adding control on the terminals of the VCO's memristors according to the timing stage at this moment. The Verilog-A code for the modified version of the timing controller is provided in Appendix-A.

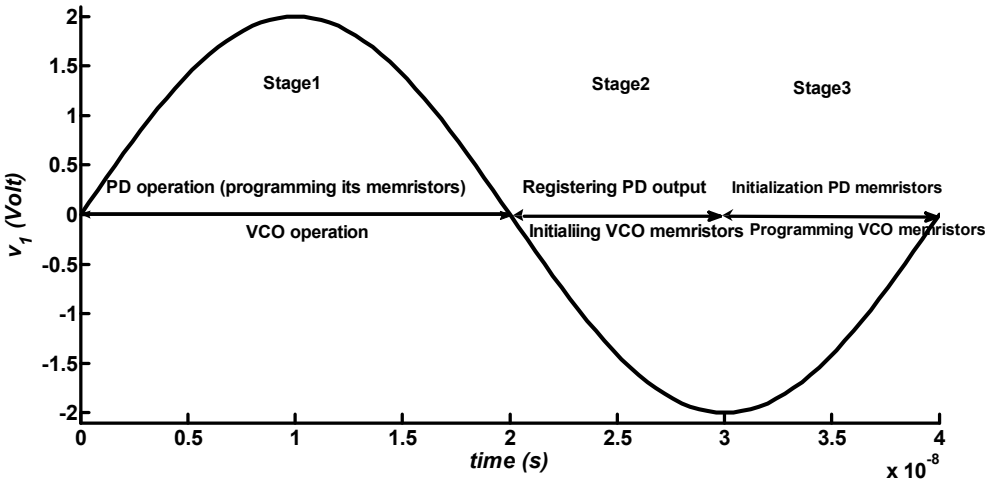



**Fig. 5-11. The timing scheme for the PD and the VCO in the proposed PLL system.**

Finally, a simple amplifier circuit is needed to work as a fitting stage between the phase detector and the VCO, as shown in Fig.5-12. Since, the DC output of the phase detector at certain frequency difference may be not exactly equal the needed DC input for the VCO to generate a signal that compensates this difference in frequency.

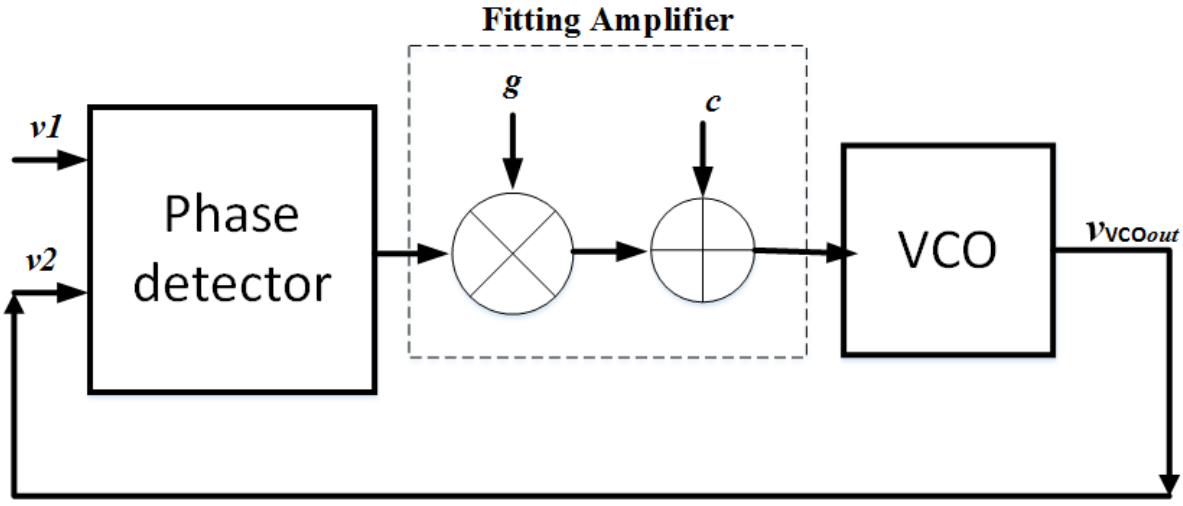



**Fig. 5-12. The block diagram of the proposed PLL after adding the fitting amplifier.**

Therefore an amplifier has gain, $g$, and a DC offset, $c$, is required. Accordingly, the values of the required gain and offset are extracted using Matlab program for fitting via optimization. For doing this, the following sequence is followed,

1- The DC outputs of the phase detectors, due to frequency differences, $\Delta f$, in the range -5 MHz to +4MHz with 1MHz separation are recorded using the phase detector simulation results, drawn in Fig. 4-14 (b).

2- The needed memristances for generating a signal with frequency equals the center frequency plus the frequency differences, $f_{out} = f_o + \Delta f$ are detected by the VCO simulation, as shown in Table 5-4.

3- The values of the DC input required for producing the detected VCO memristances are obtained by applying one of the interpolation techniques on the data of the curve between the DC input and the reached memristance, as shown in Fig.5-13. The extracted Voltages and their corresponding memristance value for each frequency are tabulated in Table 5-4. Noting that, the reached memristance is the final memristance resulted by applying this DC input for max programming time on the memristor at initial memristance.

4- The fitting is done between the phase detector DC outputs gotten from step1 and the VCO DC inputs gotten from step 3.

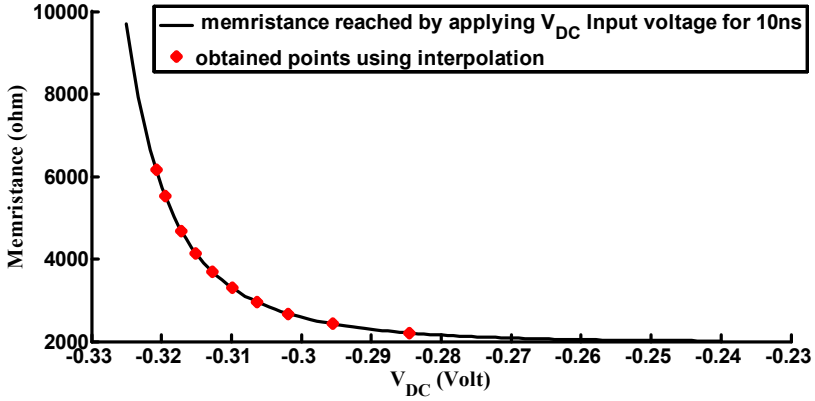



**Fig. 5-13. Extracting the required VCO input voltage for generating frequencies between 20 and 29 MHz.**

The Matlab program for calculating the fitting constants is reported in Appendix-B. Additionally, the accuracy of the fitting process is measured using the coefficient of determination, $r^2$. The expression of the accuracy measuring coefficient is mentioned in (5-11). The coefficient of determination ranges from 0 to 1 such that the fitting is more accurate as $r^2$ is closer to 1 [102]. The curves of the fitting processes for frequency ranges between (20 to 29MHz) and (22 to 27MHz) are illustrated in Fig. 5-14 and 5- 15 respectively. The obtaining gain, DC offset, and coefficient of determination are tabulated in Table 5-5 for both frequency ranges.

$$r^2 = 1 - \frac{sum\ of\ squared\ \ error\ \ between\ \ accurate\ \ and\ \ fitted\ \ data}{(n-1) * variance\ \ (accurate\ \ \ data\ )}, \qquad (5\text{-}11)$$

n= total number of points

**Table 5-4. Extracted Voltages and their corresponding memristance value for frequencies between 20 and 29MHz.**

| $f_{out}$ (MHz) | $R_m$ (KΩ) | $V_{VCO\ in}$ (Volt) |
|---|---|---|
| 20 | 6.1558 | -0.3208 |
| 21 | 5.5258 | -0.3195 |
| 22 | 4.685 | -0.3172 |
| 23 | 4.142 | -0.3151 |
| 24 | 3.685 | -0.3127 |
| 25 | 3.2958 | -0.3099 |
| 26 | 2.96 | -0.3064 |
| 27 | 2.675 | -0.3019 |
| 28 | 2.428 | -0.2955 |
| 29 | 2.2072 | -0.2845 |

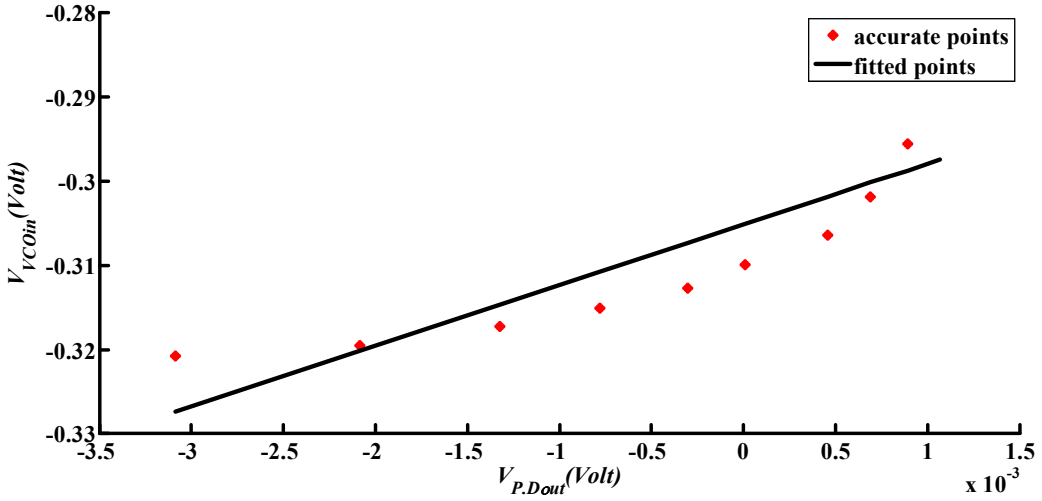



**Fig. 5-14. Fitting between the PD output and thr required VCO input for frequencies between 20 and 29MHz.**

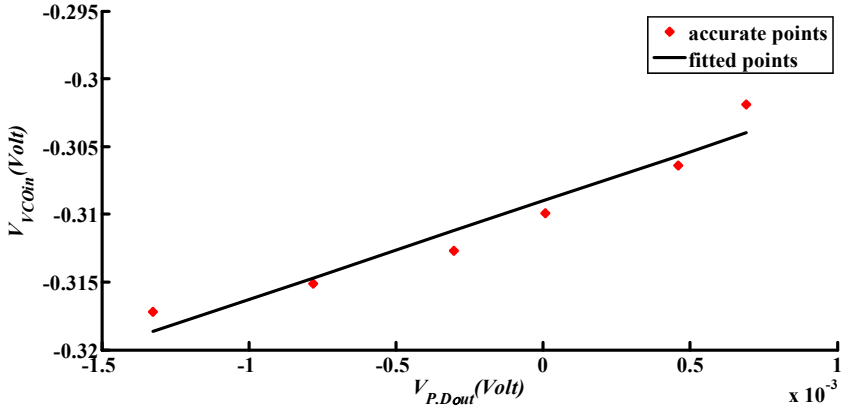



**Fig. 5-15. Fitting between the PD output and the required VCO input for frequencies between 22 and 27MHz.**

**Table 5-5. Calculated gain and DC offset for the fitting amplifier.**

| Frequency Range | 20 to 29MHz | 22 to 27MHz |
|---|---|---|
| Gain ($g$) | 7.2084 | 7.2515 |
| DC offset ($C$) | -0.3051(V) | -0.309(V) |
| coefficient of determination ( $r^2$) | 0.7319 | 0.9371 |

### 5.2.4 The Non-continuous Operation

Some researchers investigated the effect of the non-continues operation (switching mode) of the PLL components on its dissipated power and phase noise, then they proved the decreasing of the consumed power and the phase noise in the non-continues PLL than it in traditional PLL systems [87]. On other hand, this method is suitable to decrease power consumption in PLL when use in a body implants because the temperature is constant in body and therefore, frequency deviation is minimum and there is no need to continuous detection of the phase error and only 10 percent of total time is enough for operation of the phase frequency detector and its belonging circuits [87].

Thereby, to decrease the power consumption in the proposed PLL and to release the constrain of achievement the three stages in one cycle of the reference signal, the non-continuous operation is adopted. The phase frequency detector, the fitting amplifier and circuit controlling the three stages of the PLL blocks are switched on and off by a control signal for switching. The phase frequency detector, the fitting amplifier and controlling circuit are switched on for duration of one reference signal's cycle time. Then they are switched off for duration equal to nine times of reference signal's cycle time. While the control loop is switched on, the level of control voltage for VCO (output of the fitting amplifier) is sampled and hold by using a sample and hold circuit. After the control loop is switched is switched off, control voltage for VCO remains the same and is supplied by sample and hold circuit.

### 5.2.5 Simulation results

The final block diagram of the proposed PLL system, after modifying the PD controller to control the switching of both the PD and the VCO, is shown in Fig. 5-16. The design has simple structure compared to the counterpart PLL structure in [87]. Simulation is done using Cadence simulation environment. The schematic of the simulated design is shown in Fig. 5-17. The simulation results are shown in Fig. 5-18 (a), (b), (c), (d), and (e). Fig. 5-18 (a) shows the assumed reference sinusoidal input at 27 MHz, Fig. 5-18 (b) shows the input of the VCO block. It can be noted that the nonzero values of the drawn input represents the needed voltage to return the VCO memristors to its initial value (2.1 V) then the output of the PFD after passing through the fitting amplifier, which is needed to program the VCO memristors to the corresponding value for generating the proper frequency, (it is the negative different voltages in the drawn signal). Moreover, Fig. 5-18 (c) shows the VCO instantaneous output (the feedback signal). Fig. 5-18 (d) and (e) show the frequency of the VCO output versus time and cycle number respectively. It can be seen that the frequency of the VCO changed from 28.2MHz to 27.065 MHz after programmed by the PFD fitted output. The error between the feedback signal frequency and the reference frequency equals 0.24% which turns out a reliable design. This small error may be due to the error between the fitted voltage and the accurate voltage required by the VCO block.

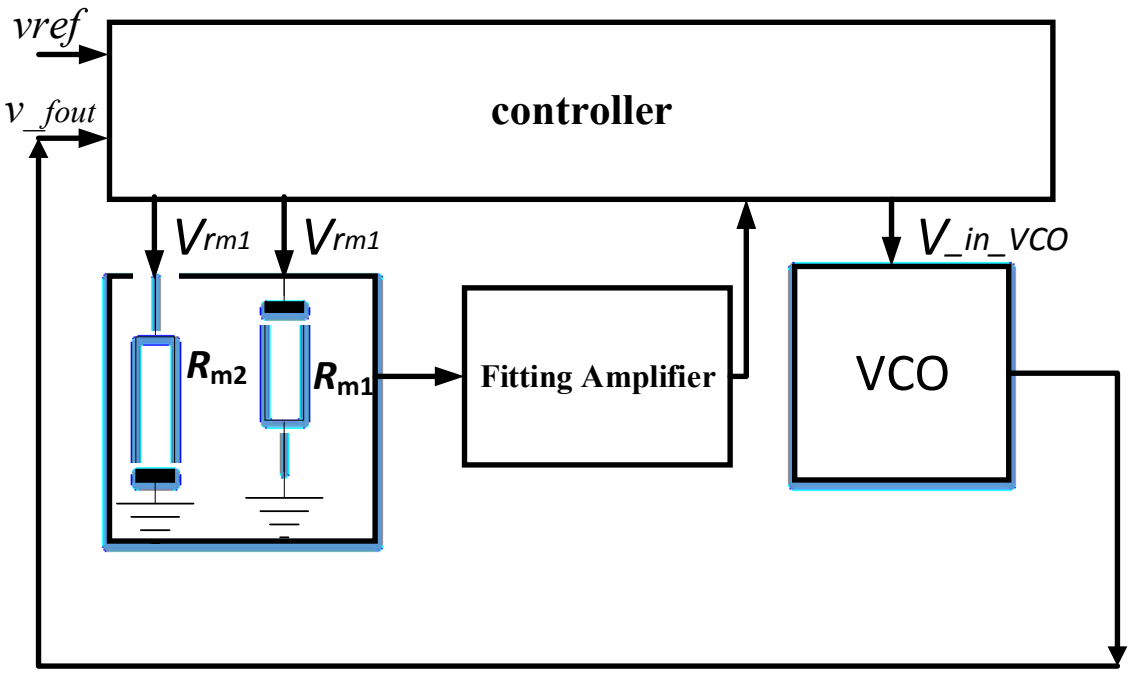



**Fig. 5-16. The final block diagram of the proposed PLL system.**

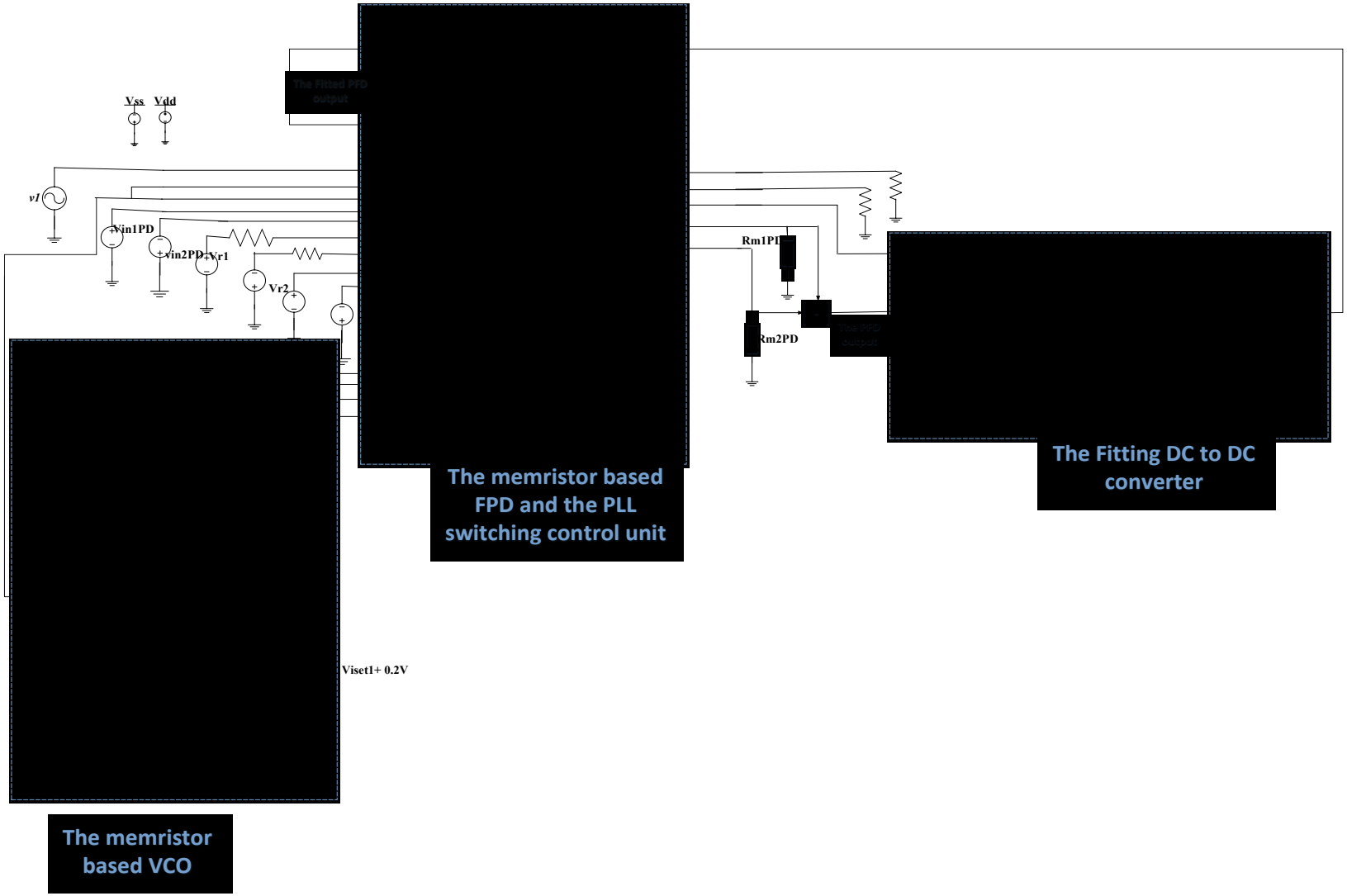



**Fig. 5-17. The schematic of the simulated PLL system.**

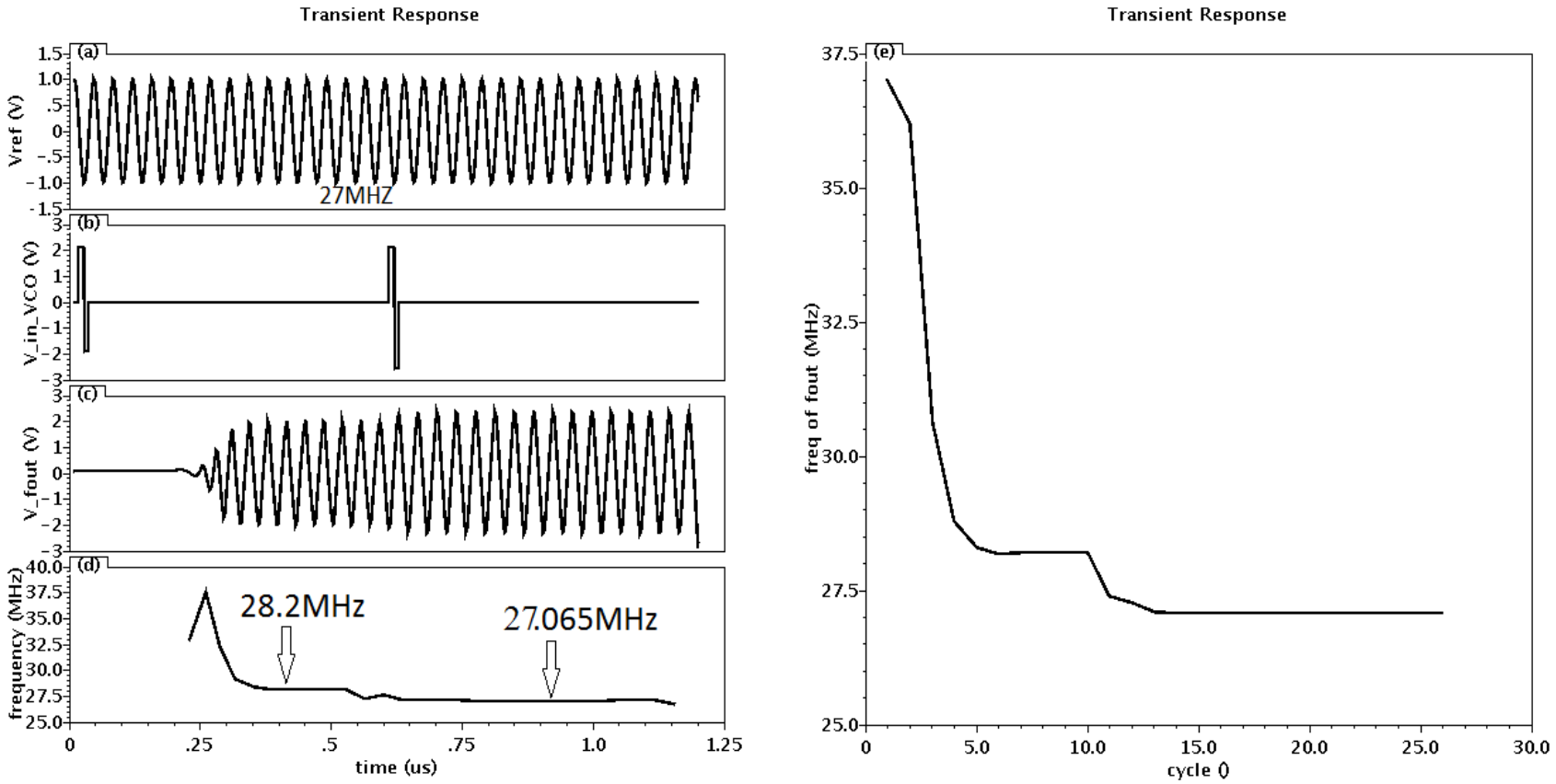



**Fig. 5-18. The simulation results of the proposed PLL system.**
**(a). The reference signal**
**(b).The input DC voltage of the VCO circuit**
**(c).The VCO output signal with frequency $f_{out}$**
**(d). The frequency of the VCO output signal versus time**
**(e). The frequency of the VCO output signal versus cycle**

**Chapter Six**

# Conclusion and Future Work

## 6.1Conclusion

A memristor is considered to be the fourth fundamental circuit element besides the resistor, capacitor, and inductor. The memristor features such as, nonlinearity nature, non-volatility, compatibility with conventional CMOS technology (electrically and with respect to manufacturing), and high scalability, encourage researches for coming up with numerous applications for memristors in traditional and new structure circuits. Furthermore, the emerging of more memristor-based designs enhances the chance of memristor technology to replace CMOS technology especially with the existence of several challenges that limit further CMOS scaling.

Accordingly, this thesis presents a detailed study for the effect of phase shift of sinusoidal, square, and triangular signals on the characteristics of the memristor. Based on linear dopant drift equations, the paper presents a mathematical analysis that shows a strong dependence of the average memristance as well as the memristor I-V characteristics with the phase of the periodic signal. This concept was verified by simulation using both linear dopant drift as well as experimentally proven nonlinear models of the memristor.

Consequently, a set of novel memristor-based demodulators, e.g. BPSK, QPSK, BFSK, 8-QAM demodulators are introduced, which do not need of any complementary circuit like clock recovery circuits, hence suitable for ultra-low power applications such as biomedical circuits.

Moreover, a novel and simple phase frequency detection technique based on two memristor elements, is proposed and demonstrated in this Chapter. This technique is able to generate a pure DC signal that represents the difference in phase or frequency between two sinusoidal inputs. Therefore, the proposed technique eliminates the need for LPF block in the PLL structure which reduces the dissipated power and the area of the overall PLL system hence results in more efficiency when used in body implants.

Additionally, A memristor-based Voltage Controlled Oscillator (VCO) using a single dual current output OTA (Operational Transconductance Amplifier) is presented. The proposed circuit includes a single dual current output OTA and only four passive components (two memristor and two capacitors). Resistance Controlled Gain (RCG) feature of the OTA is used for achieving memristance independent oscillation condition. The presented VCO operates at high frequency relative to its counterparts of memristor based oscillators.

Finally, the memristor-based phase frequency detector and the memristor-based VCO are integrated to build a memristor-based switching mode PLL system that suitable for some important biomedical applications that operate in same frequency range.

On the other hand, the suggested circuits and techniques are inclusive and can be extended to higher frequencies following the advancement in memristor technologies. Sensitivity to circuit parameters as well as to keying errors is very low. Power consumption of these circuits is limited to the signal path and is strongly related to the memristance technology.

## 6.2 Future Work

The lessons learnt from this work will help us enhance similar designs in the future. Some improvements that we now foresee are listed below:

1- Considering the noise immunity and reliability factors through the designing of the proposed circuits. It can be done by evaluating and improving the bit error rate versus the signal noise ratio performance.

2- Designing the building blocks, comparator and slope direction detector circuits, needed for constructing the control unit of the proposed phase frequency detector and the PLL systems. Study the effect of the control unit delay and area on the circuits' bandwidth and area respectively. Moreover, studying the capability of designing memristor-based control units for fully memristor-based phase frequency detector and PLL systems.

3- Study the capability of using memristor based switches [103], [104] instead of transmission gates for switching between the memristors' different applied input voltages through the different PFD and VCO operation modes.

4- employment of the proposed memristor based BPSK demodulator along with the memristor based modulation presented in literature [67] which allows constructing a full-duplex memristor based data communication system that may improve the controllability and area of the overall medical implanted systems (the external controller and the implantable device).

5- Adding an amplitude control loop to the PLL system to stabilize VCO output signal's amplitude. Where the feedback signal with variable

amplitude confuses the phase noise reading due to the effect of the signal amplitude on the memristors final resistance.

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# Appendix-A

## THE VERILOG-A CODES

*//A.1 The developed Verilog-A model of the nonlinear dopant drift //model* [26] *including the threshold effect*

```
//including the necessary libraries
`include "constants.vams"
`include "disciplines.vams"

//defining the module name and ports
module nonlinear_memristor_model(pos,neg);
inout pos, neg ;
electrical pos, neg ;

//defining the module variable parameters
parameter real a=2.0;//model parameter
parameter real b=9.0; //model parameter
parameter real c=0.01;//model parameter
parameter real g=4.0; //model parameter
parameter integer n=4; //model parameter
parameter integer q=13; //model parameter
parameter integer p=1; //model parameter
parameter real lim_max= 0.95; //model parameter
parameter real lim_min= 0.05; //model parameter
parameter real skalaa= 10e-9; //model parameter
parameter real rleak= 0.01; //model parameter
parameter real cap= 8e-5; //model parameter
parameter real w_init=0.95; //initial state
parameter real rm_init=7.1968e5; // initial memristance
parameter real rm_max=6.9719e7; //maximum memristance
parameter real rm_min=7.1968e5; //minimum memristance
parameter real v_th=0.1; //threshold voltage

//defining the variables
real w, dw, fx, x1, x2, x3, x4,vp,w_last,rm_last,rm,assert,w0;

//Sign function
analog function integer sign;
real arg; input arg;
sign = (arg > 0 ? 1 : -1 );
```

```
endfunction

analog begin

//defining the initial conditions
@(initial_step or initial_step("dc")) begin
w_last=w_init;
rm_last=rm_init;
w=w_init;
w0=w_init;
rm=rm_init;
end
// dividing the dynamical memristor equations to terms for simplification
fx=1-pow((2*w-1),2*p);
x4=(1+sign(V(neg,pos)))/2;
x1=(1+sign(lim_max-w))/2;
x2=(1+sign(V(pos,neg)))/2;
x3=(1+sign(w-lim_min))/2;
vp=pow(V(pos,neg),q);

//evaluating the dynamical memristor equation
dw=(x1*x2+x3*x4)*vp*fx/cap;

// the threshold effect
if (abs(V(pos, neg)) <=v_th)
begin
w=w_last;
w0=w_last;
rm=rm_last;
I(pos,neg)<+V(pos,neg)/rm;
assert=1;// to prevent the state integration process (stat change)
end
//limiting the state at its maximum
else if ((w>=lim_max)&&(V(pos,neg)>=0))
begin
w=lim_max;
rm=rm_min;
I(pos,neg)<+V(pos,neg)/rm;
assert=2;
w0=lim_max;
end

//limiting the state at its minimum
else if ((w<=lim_min)&&(V(pos,neg)<=0))
begin //i add dw==0
```

```
w=lim_min;
rm=rm_max;
I(pos,neg)<+V(pos,neg)/rm;
assert=3; // to prevent the state integration process (stat change)
w0=lim_min;
end

else begin

//memristor quasi-static equation
I(pos,neg)<+((pow(w,n)+rleak)*b*sinh(a*V(pos,neg))+c*(exp(g*V(pos,neg))-
1))*skalaa;
//calculating the memristance
rm=V(pos,neg)/I(pos,neg);

//limiting the memristance between its maximum and minimum
 rm = min( rm_max , max(V(pos,neg)/I(pos,neg),rm_min ) );
assert=0; // allow the state integration (state change)
end
// state integration
w=w0+idt(dw,0,assert,1);
//modify the previous state by the present one
w_last=w;
rm_last=rm;

end // end analog
endmodule
```

## *//A.2the developed Verilog-A code for the Phase detector controller*

```
//including the necessary libraries
`include "constants.vams"
`include "disciplines.vams"

//defining the module name and ports

module phase_detector_controller (vref, vfb, vr1, vr2, vin1, vin2, read_enable,
init_enable, prog_enable, vout1, vout2);

//vref is the reference input signal, vfb is the feedback signal, vr is the reading voltage in
series to //the reading resistance, vin is the initializing dc voltage, vout is the voltage
applied on the //memristor. The subscript '1' is indication for the firs tmemristor input
```

and outputs while //subscript '2' for the second memristor. read, init, and prog_enable are flags to indicate the //current stage.

```
input vref,vfb,vr1,vr2,vin1,vin2;
output prog_enable, read_enable, init_enable, vout1,vout2;
electrical vref,vfb,vr1,vr2,vin1,vin2,read_enable,init_enable,prog_enable,vout1,vout2;


//defining the module variable parameters
parameter real td = 10n; //time needed for initialization of the phase detector's memristors
parameter real vth= 0; //threshold voltage

//defining the variables
real x, read_par,tend;
analog begin

//defining the initial condition
@ (initial_step)
begin
x=3;
V(prog_enable)<+0;
V(read_enable)<+0;
V(init_enable)<+0;
end
//stage of detecting the phase shift (programming stage)
@(cross(V(vref),1))
begin
V(vfb,vout1)<+0;//short
V(prog_enable)<+1;
V(read_enable)<+0;
V(init_enable)<+0;
I(vref,vout1)<+0;//open
I(vr1,vout1)<+0;//open
I(vr2,vout1)<+0;//open
I(vin1,vout1)<+0;//open
I(vin2,vout1)<+0;//open
I(vref,vout2)<+0;//open
I(vfb,vout2)<+0;//open
I(vr1,vout2)<+0;//open
I(vr2,vout2)<+0;//open
I(vin1,vout2)<+0;//open
I(vin2,vout2)<+0;//open
x=0;
end
```

```
// stage of reading the phase detector's memristors
@(cross(V(vref)-x,-1))
begin
   read_par=1;

   tend = $abstime + td;//return simulation time + td
end

@(timer(tend))
read_par=0;

V(read_enable) <+read_par;

if (V(vref)<0 && read_par==1)
begin
V(vout1,vr1)<+0;//short
V(vr2,vout2)<+0;//short
I(vref,vout1)<+0;//open
I(vr2,vout1)<+0;//open
I(vr1,vout2)<+0;//open
I(vfb,vout1)<+0;//open
I(vin1,vout1)<+0;//open
I(vin2,vout1)<+0;//open
I(vref,vout2)<+0;//open
I(vfb,vout2)<+0;//open
I(vin1,vout2)<+0;//open
I(vin2,vout2)<+0;//open
V(init_enable)<+0;
V(prog_enable)<+0;
end
//initialization stage
if ( V(vref)<0 && x==0 && read_par==0)
begin
V(vout1,vin1)<+0;//short
V(vout2,vin2)<+0;//short
I(vref,vout1)<+0;//open
I(vfb,vout1)<+0;//open
I(vr1,vout1)<+0;//open
I(vr2,vout1)<+0;//open
I(vin2,vout1)<+0;//open
I(vref,vout2)<+0;//open
I(vfb,vout2)<+0;//open
I(vr1,vout2)<+0;//open
I(vr2,vout2)<+0;//open
```

```
I(vin1,vout2)<+0;//open
V(prog_enable)<+0;
V(init_enable)<+1;
end
end// end analog
end module
```

# Appendix-B

## MATLAB CODE

*%B.1 Matlab code for evaluating the dc voltage for memristor initialization*

```
clear;
clc;

% the model constants
a=2;
b=9;
c=0.01;
g=4;
n=4;
q=13;
p=1;
cap=8e-5;
lim_max=0.95;
lim_min=0.05;
skalaa=10e-9;
rleak=0.01;
wo=0.05;  %the worst case of the state value
tmin=0;
tmax=10e-9;  %assumed initialization  time
n1=100; %no of steps
cnt=1;
vinit=1;%initial value of tested voltage
vfinal=3; %final value of tested voltage
step=(vfinal-vinit)/100;
for v=vinit:step:vfinal
   varray(cnt)=v %array of the tested voltage values
   cnt=cnt+1;
   wo=0.05;
   w(1)=wo;
   count=1;
   tstep=(tmax-tmin)/n1;
   for osat=tmin:(tmax-tmin)/n1:tmax; %testing each element of the tested voltage array
```

```
        count=count+1;
        fx=(1-(2*wo-1)^(2*p));
        dw=(((1+sign(lim_max-wo))/2)*((1+sign(v))/2)*(v^q)*fx+((1+sign(wo-
        lim_min))/2)*((1+sign(-1*v))/2)*(v^q)*fx)/cap;  %the memristor dynamical
equation
        w(count)=w(count-1)+tstep*dw;
        if(w(count)>lim_max) %limit the state at its max
           w(count)=lim_max;
        elseif(w(count)<lim_min) %limit the state at its min
           w(count)=lim_min;
        end
        wo=w(count);
  end
  w_array(cnt-1)=w(count) %array of the final state
end
figure(1)
plot (varray,w_array,'k') %drawing the final state versus the tested voltage values
```

## *%B.2 Matlab code for evaluating the fitting constants*

```
function fitting_calculation
clear
clc
function [estimates, model] = fitcurvedemo(vpd, vco_in)

% Call fminsearch with a random starting point.
start_point = rand(1,2);
model = @expfun;
estimates = fminsearch(model, start_point);
function [sse, FittedCurve] = expfun(params)
    g = params(1);%the gain of the fitting amplifier
    c = params(2); %the dc offset of the fitting amplifier
    FittedCurve = g*vpd+c;
    ErrorVector = FittedCurve - vco_in;%error between the fitted values and the required
values
    sse = sum(ErrorVector .^ 2);%sum of squared error
   end
end %for the range between 20 to 28MHz
% the output of the phase detector unit for the frequency difference between 20 to
28MHz vpddata=
[-3.086e-3
   -2.085e-3
```

```
   -1.325e-3
   -781.7e-6
   -303.5e-6
   7.332e-6
   459.2e-6
   691.8e-6
   890.4e-6
  ];

vpddata=vpddata';
vco_in_data=% the required input of the VCO unit for the frequency output between 20
                %to 28MHz
[-1.928
-1.922
-1.916
-1.909
-1.903
-1.892
-1.88
-1.868
-1.856
];
vco_in_data= vco_in_data';
[estimate1, model1]=fitcurvedemo(vpddata, vco_in_data)
figure(2)
plot(vpddata, vco_in_data, '*')%drawing the accurate required curve
hold on
[sse, FittedCurve] = model1(estimate1);
 plot(vpddata, FittedCurve, 'r') %drawing the fitted curve
 hold on
%calculating the coefficient of determination
yresid = vco_in_data- FittedCurve;
SSresid = sum(yresid.^2);
SStotal = (length(myfdata)-1) * var(vco_in_data);
rsq = 1 - SSresid/SStotal
end
```

# Appendix C

## LT1228 OTA SPICE MODEL

```
* LT1228 OTA and CFA
* SUBCIRCUIT CONNECTIONS MATCH DATASHEET PINOUT FOR 8-PIN DIP
*1=IOUT OTA/+IN CFA
*2=-IN OTA
*3=+IN OTA
*4=V-
*5=ISET CFA
*6=OUTPUT CFA
*7=V+
*8=-IN CFA
*
simulator lang=spice
.SUBCKT LT1228 1 2 3 4 5 6 7 8
*
* THE OTA
Q11 5 5 21 QN 10
Q12 21 21 22 QN 10
VC 22 4 DC 0
F1 26 4 VC 0.375
F2 27 4 VC 0.25
F3 28 4 VC 0.375
F4 7 23 VC 1.6
F5 7 24 VC 1.6
VB 7 25 DC 1.4
CE1 23 7 11PF
CE2 24 7 11PF
RE13 23 32 120
RE14 24 33 120
Q13 29 25 32 QPI
Q14 1 25 33 QPI
Q15 23 3 28 QNI 9
Q16 23 3 27 QNI
Q17 23 3 26 QNI
Q18 24 2 26 QNI 9
Q19 24 2 27 QNI
Q20 24 2 28 QNI
VM 29 4 DC 1.4
FM 1 4 VM 1
DM 29 1 DC
```

```
C1 1 7 5PF
*
* THE CFA
Q2A 4 1 10 QP 0.5
Q3A 11 10 200 QN
Q4A 11 11 7 QP
Q5A 9 11 7 QP
Q6A 12 11 7 QP
Q7A 4 9 12 QP
Q8A 7 12 13 QN 10
RSCA 13 6 10
IBA 7 10 DC 300U
*
Q2B 7 1 110 QN 0.5
Q3B 111 110 200 QP
Q4B 111 111 4 QN
*
Q5B 9 111 4 QN
Q6B 112 111 4 QN
Q7B 7 9 112 QN
Q8B 4 112 113 QP 10
RSCB 6 113 10
IBB 110 4 DC 300U
*
RC 8 200 20
R9 9 0 201600
D1 9 6 DC
D2 6 9 DC
*
.MODEL DC D
.MODEL QNI NPN
.MODEL QN NPN(IS=168E-18 BF=150 ISC=40E-18 NC=1 RB=250 RE=8 RC=100
+CJE=0.37P VJE=0.65 MJE=0.33 FC=0.7 CJC=0.8P VJC=0.62 MJC=0.44
+TF=300P
.MODEL QPI PNP
.MODEL QP PNP(IS=230E-18 BF=150 ISC=113E-18 NC=1 RB=250 RE=8 RC=100
+CJE=0.34P VJE=0.75 MJE=0.40 FC=0.7 CJC=0.8P VJC=0.5 MJC=0.36
+TF=300P
*
.ENDS LT1228
```

# ملخص البحث


من المتوقع أن يصل الت صغير المستمر للترانزستورات من فئه شبه موصل اكسيد معدني المكمله ( SOMC) إلي نهايته. حيث تحد التحديات المادية والتكنولوجية والاقتصادية والحرارية وتحديات خاصه بالقدره المبدده مزيد من التصغير.

تتميز أجهزه المقاومه ذات الذاكره بأن لها مقاومه غير متطايره وإنخفاض القدره المبدده بها وتناهي صغر أبعادها وتوافقها مع تكنولوجيا ا لشبه موصل اكسيد معدني المكمله ( SOMC) مما جعلها مكمل أو بديل حقيقي لها. وعلاوة على ذلك ، فإن ظهور المزيد من التصاميم القائمة على أجهزه المقاومه ذات الذاكره للدوائر التقليدية الأساسية أو الدوائر ذات الهياكل الجديدة يعزز فرصة إستبدال تكنولوجيا تقنية الشبه موصل اكسيد معدني المكمله ( SOMC) بتكنولوجيا المقاومه ذات الذاكره.

بشكل عام ، تم اقتراح الكثير من التطبيقات القائمة على أجهزه المقاومه ذات الذاكره خلال السنوات العشر الأخيرة وقد تضمنت هذه الإ كتشافات تنفيذ الذاكرة غير المتطايرة ، والأنظمة العصبية ، ومكبرات الصوت التكيفية ، والمرشحات. في هذه التطبيقات ، تم استغلال تكيف قيمه المقاومة ذات الذاكره وفقًا لسعة الإشارة المطبقة أو ترددها. ومع ذلك ، حتى الآن ، تم تكريس القليل من الجهود لاستخدام الدوائر غير الخطية في نظم الاتصالات.

ويلاحظ أن في معظم التطبيقات المذكورة سابقا ، تم إعتماد نموذج إنحراف الشوائب الخطي. وعلى الرغم من أن هذا النموذج يلبي المعادلات الأساسية ل لأنظمه ذات الذاكره ، فإنه ينحرف بشكل كبير عن سلوك أجهزة المقاومه ذات الذاكره المصنعة. بالإضافة إلى ذلك ، فإن هذا النموذج قابل للتطبيق على تردد منخفض جداً لذلك تم التحقق من معظم التصاميم المقترحة التي اعتمدت هذا النموذج على تردد منخفض (1- 100Hz) مما يحد من إستخدامه في التطبيقات الفعلية.
وبناءً على ذلك فإن الهدف الرئيسي من هذه الأطروحة هو دراسة إعتماد المقاومة ذات الذاكره على زاويه الطور الأوليه للإشارة الدورية المطبقة. ،وقد تم تصميم مجموعة من الوحدات البنائيه لتطبيقات الاتصالات.

أولاً ، تم تدارس و إقتراح مستخلصات جديدة للإتصالات الرقمية مبنية على المقاومة ذات الذاكره . المستخلصات المقترحة مخصصة للتقنيات الأتيه: مفتاح إزاحة الطور الثنائي ( BPSK) ، ومفتاح إزاحة الطور التربيعي ( QPSK) ، و تعديل سعة الاشاره التعامدي (8-QAM)، و مفتاح ازاحة الذبذبة الثنائي (BFSK).

وبما أن جميع دوائر المستخلصات المقترحة غير متزامنة ، فإن المستخلصات المقترحة لا تحتاج إلى أي دوائر لاستعادة الموجة الحاملة.

ثانيا ، يتم تقديم كاشف التردد وإزاحه الطور للإشاره الجيبية قائم على المقاومه ذات الذاكره للمرة الأولى على الإطلاق. الكاشف المقترح يمكنه توليد إشارة من التيار المستمر(DC) تمثل الفرق في الطور أو التردد بين المدخلين الجيبيين. لذلك ، فإنه يلغي الحاجة إلى دائره مرشح التمرير منخفض ( LPF) في بنية حلقه تثبيت الطور التقليدية (PLL) مما يقلل من المساحة والقدره المبدده لنظام ال PLL الكلي.

ثالثا، يتم إقتراح مذبذب محكوم بالجهد قائم على المقاومه ذات الذاكره (VCO) باستخدام عدد واحد مواصلة تبادلية تشغيلي مكبره (OTA) ذات تيار مزدوج واحد. تتضمن الدارة المقترحة وحدة (OTA) ذات تيار

مزدوج واحد ، وأربعة مكونات سلبية فقط ( مقاومتان ذات الذاكره ومكثفان). المكثفات في دائرة المذبذب مؤرضه، وبذلك تكون مفضلة للدمج. يتم استخدام خاصية الكسب المحكوم بالمقاومه (RCG) الخاصة بـال( OTA) لتحقيق شرط تذبذب غير معتمد علي قيمه المقاومه ذات الذاكره.

وأخيرًا ، يتم دمج كاشف التردد والطور القائم على المقاومه ذات الذاكره مع المذبذب م حكوم بالجهد (VCO) القائم على المقاومه ذات الذاكره لتكوين نظام حلقه تثبيت الطور (PLL) بنظام التشغيل والإيقاف قائم على المقاومه ذات الذاكره ، وهو مناسب لبعض التطبيقات الطبية الحيوية المهمة التي تعمل في نفس نطاق التردد للنظام المقترح.

وتجدر الإشارة إلى أنه ،تم إستخدام نموذج إنحراف الشوائب "اللاخطي" المستند علي نتائج التجارب في تصميم الدوائر المقترحة مما يتيح دمج تأثير جميع الخصائص الغير مثالية للمقاومات ذات الذاكره المحققة عمليًا والحصول على تردد تشغيل مرتفع.

وقد نظمت الأطروحة على النحو التالي: يقدم الفصل الأول لمحة عامة عن المقاومه ذات الذاكره كجهاز متناهي الصغر . تتضمن هذه النظرة العامة تاريخ المقاومه ذات الذاكره والتنفيذات الفعلية لها ونماذج الوصف واشهر التطبيقات. بعد ذلك ، يدرس الفصل الثاني تأثير السعة ، والتكرار ، و زاويه الطور للإشارة الجيبية والمثلثية والمربعة على المقاومه ذات الذاكره من حيث تغيرات المقاومه ذات الذاكره مع الزمن والعلاقه بين الجهد المطبق عليها والتيار المار بها باستخدام نماذج إنحراف الشوائب الخطية وغير الخطية. بينما يعرض الفصل الثالث المستخلصات المقترحة القائمه علي المقاومه ذات الذاكره لبعض مخططات التعديل الرقمي. و يتم تقديم كاشف التردد والطور القائم على المقاومه ذات الذاكره المصمم عند ٢٥ ميجا هرتز في الفصل الرابع. ويتم عرض المذبذب المحكوم بالجهد (VCO) المقترح و القائم على المقاومه ذات الذاكره ونظام حلقه تثبيت الطور (PLL) بنظام التشغيل والإيقاف في الفصل الخامس . وأخيراً ، تتم مناقشة استنتاجات الأطروحه والأعمال المستقبليه المقترحة في الفصل السادس.

مهنـــــــــــــــــــــــدس: نهلة العزب عبد اللطيف الأشقر
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تاريخ التسجيل: 1/ 3 / 2011
تـــــاريخ المنـــــح: / /
القســـــــــــــــــــــم: الالكترونيات واللاتصالات الكهربيه
الدرجـــــــــــــــــــــة: دكتوراه
المشرفون : أ.د.أحمد حسين محمد خليل
أ.د حسام علي حسن فهمي
د. محمد مصطفي ابو دينه
د.غاده حمدي ابراهيم مدرس بمعهد بحوث الالكترونيات
الممتحنـــــــــون : أ.د.أحمد حسين محمد خليل
د. حسن مصطفي
أ.د السيد مصطفي سعد استاذ بهندسه حلوان

عنـــــوان الرسالـــة : **وحدات مبتكرة للإتصالات اللاسلكيه القائمة علي المقاومة ذات الذاكرة**

الكلمات الدالة : - (المقاومه ذات الذاكره - زاويه الطور للإشارة الدورية - مفتاح إزاحة الطور الثنائي - مفتاح إزاحة الطور التربيعي - تعديل سعة الاشاره التعامدي- مفتاح ازاحة الذبذبة الثنائي- كاشف التردد وإزاحه الطور للإشاره الجيبية- مذبذب محكوم بالجهد- نظام حلقه تثبيت الطور)

ملـخـــــــص البحـــــــث : تتميز أجهزه المقاومه ذات الذاكره بأن لها مقاومه غير متطايره وإنخفاض القدره المبدده بها وتناهي صغرها وتوافقها مع تكنولوجيا الشبه موصل اكسيد معدني المكمله مما جعلها مكمل أو بديل لها. الهدف الرئيسي من هذه الأطروحة هو دراسة إعتماد المقاومة ذات الذاكره على زاويه الطور للإشارة الدورية المطبقة. ،وقد تم تصميم مجموعة من الوحدات البنائيه لتطبيقات الاتصالات و إقتراح مستخلصات جديدة للإتصالات الرقمية مبنية على المقاومة ذات الذاكره . مثل مفتاح إزاحة الطور الثنائي، ومفتاح إزاحة الطور التربيعي و تعديل سعة الاشاره التعامدي و مفتاح ازاحة الذبذبة الثنائي. و يتم تقديم كاشف التردد وإزاحه الطور للإشاره الجيبية و مذبذب محكوم بالجهد و نظام حلقه تثبيت الطور قائمبين على المقاومه ذات الذاكره.

# وحدات مبتكرة للإتصالات اللاسلكيه القائمة علي المقاومة ذات الذاكرة


إعداد

**نـهلة العزب عبد اللطيف الأشقر**


رسالة مقدمة إلى كلية الهندسة,جامعة القاهرة
كجزء من متطلبات الحصول على **درجة دكتوراه الفلسفه**
فى
**هندسة الإلكترونيات والإتصالات الكهربية**

يعتمد من لجنة الممتحنين:

الأستاذ الدكتور: **أحمد حسين خليل** المشرف رئيسى

الأستاذ المساعد الدكتور: **حسن مصطفي** الممتحن الداخلي

الأستاذ الدكتور:**السيد مصطفي سعد** الممتحن الخارجي
أستاذ بكليه الهندسه جامعه حلوان


كلية الهندسة,جامعة القاهرة
الجيزة- جمهورية مصر العربية
2019

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**معهد بحوث الالكترونيات**



كلية الهندسة,جامعة القاهرة
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