Project Title: Fully-Integrated Frequency-Hopping Manpack Transceiver

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Project Information

- Duration: 2 years
- Estimated budget:
    - Equipment: 179,300 EGP
    - Fabrication: 350,00 EGP
    - Salaries: 851,000 EGP
- Proposal type: small-scale
- Research Area: Other- Telecommunication Transceiver Design

1 Executive Summary

Manpack devices are one of the important modules that are used in different military situations. Frequency hopping has been the main modulation scheme that is used in such devices due to the benefits it provides for security purposes. The first Egyptian Frequency Hopping Manpack system was developed in our department in collaboration with the Egyptian military. The system was designed and assembled using commercial components on printed circuits boards.

The prototype has been sampled, and field tested and is going through a first production phase. This prototype has a few drawbacks that need to be addressed for future generations. Size, weight, power consumption, frequency ranges and hopping rate are among these issues. In this proposal, we are planning to implement enhancements to this system in order to provide solutions for these issues that can serve as the core of the second generation Frequency Hopping Manpack System.

This proposal focuses only on the transceiver side and its implementation. New specifications include frequency range of 30MHz-500MHz and hopping rate of 300 hop/sec. In this proposal, a fully integrated transceiver is planned to improve the system from all aspects. On-chip integration reduces the size drastically and in case of mass production, cost per unit also reduces dramatically. On-chip techniques provide solutions for many problems and provide innovative techniques that are mostly not possible in the discrete-component implementation.

In this proposal we are targeting a 10x reduction in cost for mass production, which is not possible in the first prototype since all components are off the shelf and their cost cannot be reduced unless they are combined together or integrated as is the case in this work. This proposal describes the issues facing the current solution and proposes solutions on different levels of the design. Power consumption reduction is based on improving the power amplifier's power efficiency as well as improving reflection behavior with the antenna on both directions. A power reduction of 5x is targeted.

This is a challenging task but achievable by changing the power amplifier architecture and customizing it to the system's need. Widening the frequency range (30MHz-500MHz) in this proposal compared to the original design poses more challenges to the circuit design. Hence, a new architecture has been introduced in this proposal that relaxes the different block-level specifications. Extensive programmability is used. Frequency planning is modified to accommodate for the new frequency requirements and at the same time to optimize the total power consumption as well as the complexity of the circuit design.

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3 Background

3.1 Introduction

Telecommunications is one of the major factors in raising the standard of living. During the past few decades, great advances occurred in the telecommunications field. That is because phenomenal advances both in research and applications have been made. As a result of that, internet services, cellular technology, and many more gave new dimension to telecommunications. These changes are also producing challenges for privacy and communications security. In cases such as military security, this creates an urgent need for advancing the state-of-the-art in communication channel security. Wireless military communication systems have been developed to account for ever-increasing sophistication in electronic warfare (EW), ECM (Electronic counter measure), and ECCM (Electronic counter counter measure). Military systems have been developed to counteract jamming, spoofing, and detection using anti-jam, anti-spoofing, and low-probability-of-intercept methods[1]. This proposal is intended to introduce developing a telecommunications transceiver device that can face such challenges. Transceiver is by definition: "A device that can both transmit and receive communications, in particular a combined radio transmitter and receiver". Further explanation according to the Wikipedia: "A transceiver is a device comprising both a transmitter and a receiver which are combined and share common circuitry or a single housing. When no circuitry is common between transmit and receive functions, the device is a transmitter-receiver. The term originated in the early 1920s. Technically, transceivers must combine a significant amount of the transmitter and receiver handling circuitry". So, as it appears from the definitions, transceiver is the main building block of the telecommunications system.

3.2 Problem Identification

One of the main specifications that classify transceivers is the frequency range within which it operates. A transceiver operates within a certain band of frequencies that are classified within the electromagnetic spectrum according to the Egyptian National Regulatory Authority (NTRA) as shown in Figure 1 [2].

Consequently, this proposal topic frequency range of interest: Very High Frequency (VHF) - Frequency Hopping (FH) transceiver is, by definition, a transceiver capable of constructing its link in the VHF range of frequencies. The VHF range is supposed to be between 30 MHz – 300 MHz according to the NTRA chart as shown previously. Such ranges are used originally to provide vast coverage range for a single transceiver for relatively lower power when compared with transceivers using higher frequency ranges. This aim makes such transceiver viable to be used in battlefield. So, we are talking here about a minimal power and size transceiver device of maximum encryption, band, and coverage. The reason for coverage is inherent in the military nature of the device so that users could enhance their deployment areas which, in turn, improve their tactics. Typical acceptable range is a five-km one. Others range up to 200 km that are used in unmanned aircrafts control [3]. Wider bandwidth means more data to be loaded on the link which leads to more applications for the transceiver other than man-to-man communication. An example for other ways of communication in the battlefield is the base-to-vehicle communication through which any military vehicle can be controlled remotely from the nearest safe military base [4]. In such a way, human losses are minimized. This unmanned vehicle control approach is practically implemented in the Crusher vehicle of Carnegie Mellon institute in association with DARPA [5]. In addition to that, VHF-FH transceiver uses Frequency Hopping technique in its communication link so that it could avoid jamming and have the rest of spread spectrum security and faster data rate advantages [6, 7].

Talking in military standards, power consumption minimization is a must to enable longer

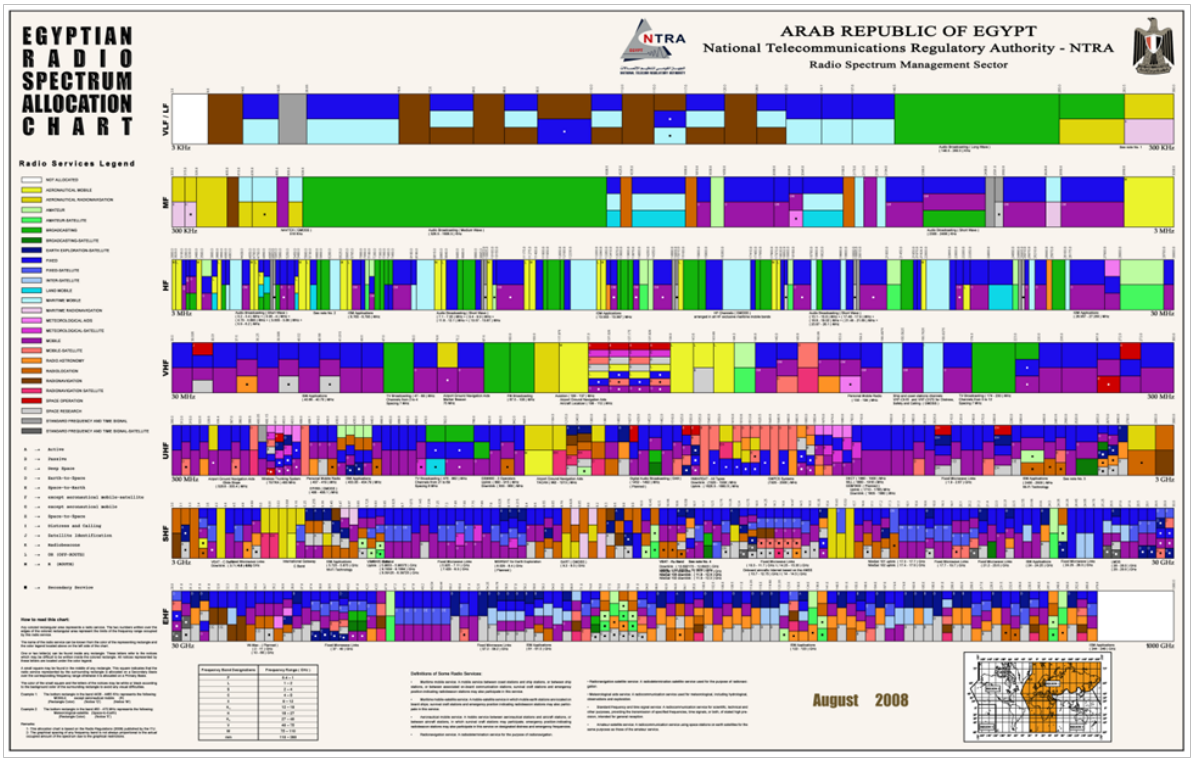

Figure 1: Egyptian Radio Spectrum Allocation Chart

usage period without the need to recharge it. Size miniaturization is a must as well. VHF transceivers convention for packaging is a back-pack size. That is to enable an infantry combat individual to carry it in action. So, its value increases exponentially with its size decrease [8]. Especially in case of the vast increase in the need to minimize transceiver further more than what is needed by the human soldier. That is due to the appearance of new applications demanding minimal and minimal sizes of transceivers. For example, the newly exposed flying quadrotors, small, agile robots that swarm, sense each other, and form ad hoc teams – for construction, surveying disasters and far more.

Although the production volume needed for such a device to be used in a military environment is not necessary high, it is still extremely important to go implement such a communication system in house for two main reasons:

- **In the past, such devices were imported. This means that all coding, security codes were all known to parties outside the Egyptian authorities. This represent a huge threat in critical situations. Moreover, any update or improvement to the system must be obtained from the same source, who can provide them or not based on many factors. Owning our own design will help Egypt become more independent and will also pave the way for many other military devices.**

- **Our main target of this proposal is for military applications, but the same communication system mentioned above can be useful as well in many other venues either exactly the same or with very little modifications. Oil mining companies can use it in desert-like places where not communication means are available. It makes the environment safer for all employees. Tourists and tourist guides can find it handy as well when visiting places without any communication means available, enhancing our tourism and opening new venues in this regard. More details will be available in section 13.**

Table 1: Typical Receiver and Transmitter Specifications

Receiver Specifications	
Receiving Sensitivity	$\leq$ 0.3uV (SINAD =10dB)
Audio output	5mW(rated), 50mW (max)
Audio distortion	$\leq$ 5%
Audio response	300 ~ 3000Hz, Less than 6 dB at 1KHz variation
IF rejection	$\geq$ 80dB
Image rejection	$\geq$ 70dB
Transmitter Specifications	
Modulation frequency offset	
• Analog voice modulation frequency offset	5.6 $\pm$ 1 kHz (rated)
• Digital voice modulation frequency offset	7 $\pm$ 1 kHz (rated)
• Pilot modulation frequency offset	3 $\pm$ 1 kHz
Pilot frequency	150 $\pm$ 2Hz
Transmitting power	6W-1dB (High power) $\geq$1W (Low power)
Frequency stability	$\leq \pm$ 3$\times$10E-6

3.3 System Requirement

Requirements of the system can be divided into general requirements, and technical communications requirements. General requirements include:

1. Operating frequency: In most devices. 30MHz-88MHz range is used. The more range, the harder it is for the jammer and the more secure the system is.

2. Weight: The lighter the better. This device is carried by a soldier all the time. In order for it not to be a liability, weight is an important factor in the design.

3. Dimension: Same as weight, this factor is important to facilitate its usage.

4. Antenna size: Must be chosen appropriately for portability purposes as well as frequency selection.

5. Supply voltage: Rechargeable batteries are favorable in these applications; recharge rate is a crucial design parameter that will have to do mainly with the power consumption of the transceiver as well all other supporting circuits.

6. Operating Modes:

   (a) Clear voice at the fixed frequency.

   (b) Digital security voice at the fixed frequency

   (c) Clear voice and digital security voice at the frequency-hopping state

   (d) Data transmission at the fixed frequency

   (e) Data transmission at the frequency-hopping state

Other requirements have to do with the transmitter and receiver specifications. Table 1 shows a typical receiver and transmitter specifications for similar modules.

Figure 2: MPS produced by Dynalog (India) limited

3.4 Existing Solutions

Due to the confidential nature of the topic, work of that nature is not usually published in scientific journals. In this section we are reporting a few examples that are used in similar ways to our target example. Few examples can be found commercially.

3.4.1 Codan 2110M HF

Codan 2110M [9] is a Manpack system that provides voice transmitter and reception as well as GPS capabilities. Frequency ranges are from 1.6 to 30 MHz Tx, 250 kHz to 30 MHz Rx. A five-Kgs weight device is produced.

3.4.2 Falcon II

Falcon II [10]device sends both voice and data up to 9600 bps. It coves frequency ranges from 1.6 MHz to 60 MHz. It has multiple products with different output power capabilities and thus different range of operations. Some products has some built-in testing capabilities. A sensitivity of -113 dBm was achieved in a 2.7KHz SSB system.

3.4.3 MPS

MPS is an integrated solution with LCD screen produced by Dynalog (India) limited. It uses a 12 VDC power supply and weights about one-Kg [11]. The product is shown in Figure 2.

3.4.4 RESOLVE EW

A similar integrated equipment is this handheld device. The RESOLVE EW Manpack is 100% UK state-of-the-art field proven electronic surveillance and attack systems. It is used to provide direction finding, to fix targets using angle of arrival, and to be mounted onto any vehicle of opportunity [12].

3.4.5 Wireless Manpack by Saabgroup

Claims to be the first man portable, smaller, and more powerful Manpack systems. It is only used for training purposes but can be generalized with more powerful devices for field trips. It increases the coverage area by 200% to be up to 6 Kms. The device weights about 1 Kg including the battery

4 Preliminary Results

A successful first version prototype has been implemented on board with discrete components. Due to the nature of the project of being confidential, not many results may be shared in this proposal. **We are going to omit the parts including specifics about the design and only keep the general architecture. Such specifics include frequency bands, exact filter selections in the receiver side, transmitter filters distribution, ... etc. Knowledge of such information would result of non-usefulness of the device when adopted by any military institute. Similar to the commercial examples shown in section 3.4 no internal design details are available. Only top level specifications.** The system specification resembles that of the general specification in section3.3. The block diagram of the transceiver is shown in Figure 3: Transceiver Block Diagram. The system can be divided as follows:

1. The user interface unit
2. Power amplifier and harmonic filters unit
3. RX/TX switch and antenna matching unit
4. Receiver front end unit
5. Analog-to-digital converter unit
6. RSP (Receiver Signal Processor) unit
7. DSP kit.
8. Power Management unit.

It is worth mentioning that the "Frequency hopping Manpack Transceiver" is a challenging system and involves a lot of DSP, communications design as well as the circuit design side of it. Another team in Cairo University is working on the systems side solving all DSP issues, modulation, demodulation, synchronization, frequency hopping and other similar issues. System requirements are provided and tested on a PCB prototype. One of our team members is also working tightly with the systems group and is the bridge between the two groups. Since the scope of the research project is to improve the Analog/RF section and integrate it on chip, its main building blocks are briefly discussed next.

4.1 Project Phase I (PCB-Version)

This version is already implemented, fabricated, and characterized.

4.1.1 Transmitter Path

The design of the transceiver architecture is governed by the following:

1. Conventional super-heterodyne designs are problematic when the RF bandwidth is relatively wide compared to the carrier frequency. In the typical case the RF frequency range covers a wide frequency ratio, making it very difficult to use multiple conversions front-end.

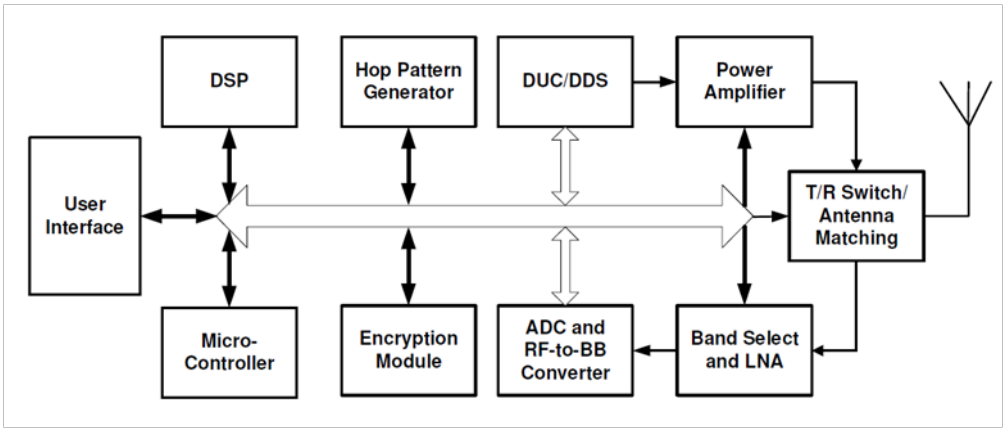

Figure 3: Transceiver Block Diagram

2. The frequency bands lie in the range of IF frequencies for the mobile communication systems, with several off-the-shelf chips available for IF-to-baseband conversion used in the base stations for these systems and having the frequency agility necessary to handle multi-user signals. Such chips can be used to handle the frequency-hopped signal. This was adequate for this discrete-components project.

3. The use of a programmable DSP for base-band signal processing and coding functions adds to the flexibility of the system in facing various jamming and interferences found in the tactical communications environment.

4. Using this architecture with its flexibility and software upgradeability is a good base for future development of more sophisticated versions of the transceiver.

A functional block diagram of the implemented transceiver is shown in Figure 3. The transceiver configuration control and user interface is done using a microcontroller. In the transmitter path, source coding, encryption and channel coding functions are done in the programmable DSP. The resulting data stream is passed to a digital up converter chip for modulating its Direct Digital Synthesizer (DDS) signal. The DDS takes its frequency control from the hop pattern generator, which is implemented in FPGA as a plug-in module. The resulting hopped signal is amplified by the power amplifier and passed to the antenna through the Transmit/Receive (T/R) switch.

4.1.2 Power amplifier and harmonic filters unit

The power amplifier receives a synthesized low-power signal and delivers the required high power, while meeting the spurious emission requirements (Harmonic distortion suppression $>$ 60 dB). A Class AB wide-band power amplifier is used to have a relatively higher efficiency. Unfortunately, second-order harmonics lie in band. A solution to this problem is implemented by using a switched bank of low-pass filters. The cut-off frequencies of the filters shall be designed to suppress the second and higher harmonics of the band of interest.

4.1.3 Modulator/Frequency Synthesizer

Direct Digital Synthesizer (DDS) technique is used for the transmitter frequency synthesizer because of its capabilities of high hopping rate and almost zero frequency-switching transients.

Two main parameters specify the synthesizer:

- The frequency range: defined mainly by the sampling clock.

- The spurious responses: defined by the DAC resolution and linearity.

A discrete component of a DDS is used. It covers the required frequency range and has a spurious free dynamic range of 70 dB is available.

The output analog interpolating filter is used to reject this alias while passing the required frequency range with negligible attenuation.

4.1.4 Receiver Path

The RF front end is a low-noise amplifier (LNA) and a band selection filter. This is followed by analog-to-digital conversion (ADC) with its driver. The ADC feeds the digital receive signal processor for conversion to complex base-band equivalent signal. The latter signal is fed at an appropriate rate to the DSP, which performs the energy detection, synchronization, decoding decryption and anti-jamming measures functions.

4.1.5 Receiver front-end unit

The receiver front end board is composed of a pre-selection filter, covering the whole band, a low-noise amplifier (LNA), a bank of band selection filters, which are switched together with the ADC/RSP clock and the RSP NCO frequency to constitute the down conversion stage to the zero-IF band. The RF front end is designed to satisfy the following requirements:

- Low noise amplification of the RF signal from the sensitivity level to a level sufficient to drive the ADC without producing noticeable quantization noise.
- Linear amplification of the signal up to the maximum expected level with enough linearity.
- Anti-aliasing filters are used to reject aliasing components before going into the ADC.

4.1.6 RX/TX switch and antenna matching unit

The antenna matching units designed to maintain two tasks:

1. To switch between the Tx/Rx operation modes. This is done to guide the RF signal between two paths, either to the Rx front-end board or from the PA board. For this task, an RFIC switch is used to control the Tx/Rx mode. The selected switch is SPDT switch with two controls that is why two complementary signals are used to control the mode of operation.
2. To match the antenna impedance, which varies considerably over the operating frequency range, to the nominal 50 ohms impedance of either the power amplifier in transmit mode or the receiver pre-selection filter in the receive mode.

4.1.7 Antenna

The application dictates a wideband whip and telescopic antenna of length < 1.5 m. An antenna of this length is very hard to match over the entire frequency range. The gain of the designed antenna is low at the low end of the frequency range and gradually increases at the higher end. Two solutions could be sought in the detailed design. Inductive loading may be used to reduce the length and VSWR over the required bandwidth [13]. The antenna is a whip or telescopic antenna that can be plugged to the transceiver chassis. A transient suppressor is used after the antenna plug to protect the transceiver circuits against electromagnetic transients. A wideband antenna-matching is implemented to match the widely varying antenna impedance over the hopping frequency range to nominal 50-Ohm impedance, with a VSWR < 3.5.

Table 2: Integrated System Specifications

Metric	Specification	Units	Comments
Frequency range	30 - 500	MHz	
Hopping rate	$>$ 300	hop/sec	
Power supply	5	V	
Modulation schemes	AME/FM/SSB/CW		
Receiver sensitivity	-117	dBm	For all supported Modulation schemes
SNDR	10	dB	Signal to (Noise + Distortion) ratio at the receiver output
Image rejection	$>$ 85	dB	
Transmitter output peak power	20	W	
Carrier leakage	$<$ -60	dBc	Relative to average inband output power
Side band rejection	$>$ 60	dBc	Relative to average inband output power
Transmit Intermodulation distortion	$<$ -70	dBc	Relative to average inband output power
Error Vector Magnitude (EVM)	$<$ 10	%	Equivalent to 99% modulation accuracy
Frequency Stability	$<$ 1e-6	Hz	
Frequency offset	$\pm$1	kHz	

4.1.8 Propagation

Different propagation models are illustrated in the literature such as Longley-Rice Propagation model [14] and Okumura's model [15]. For a 2-m antenna height, both median and ground wave attenuation are around 30 dB above 30MHz. This assumption was taken through the design and to be constant across the entire frequency band.

4.2 Project Phase II (Integrated-Version)

This is the new version targeted by this proposal. It is a fully integrated solution for the transmitter and receiver.

4.2.1 System architecture:

Table 4.2.1 shows the full system specifications.

These specifications are used as the starting point for the system level design procedure and to generate block level specifications. Since the Frequency range is extended to 500MHz, the same architecture used in Phase I cannot be used. It relies on the ADC only in the down-conversion process. This will overload the ADC sampling ratio, resulting in a power-hungry and hard-to-implement ADC. On the other hand, a frequency band of 30-500MHz bandwidth cannot be covered accurately by a single frequency synthesizer and a single down-conversion stage.

A double down-conversion system is used instead. Figure 4: Proposed Transceiver Architecture shows the complete transceiver architecture. The DAC converts the digital signal to its analog form. A LPF is followed to reject all the out-of band harmonics generated by the DAC

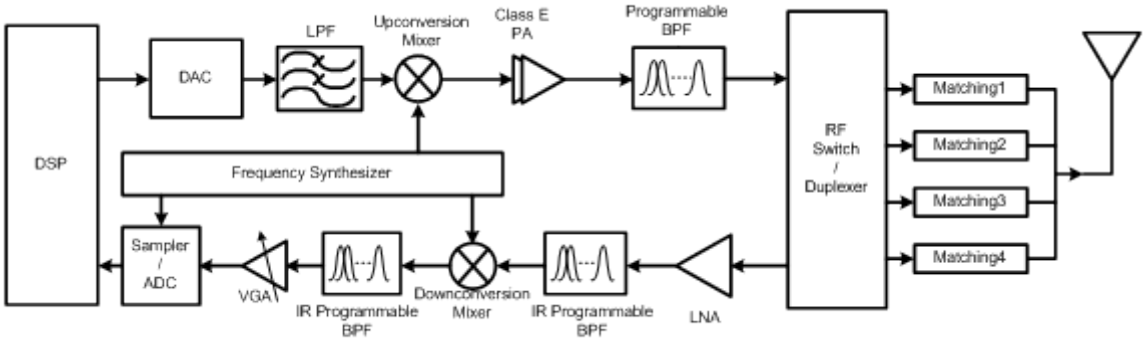

Figure 4: Proposed Transceiver Architecture

and thus reduce the linearity requirements on the mixer and PA to meet the power spectral mask of the transmitted signal. The signal is then up-converted using a mixer followed by a class E power amplifier. A programmable BPF is then added to reject all the harmonic distortion introduced by the Mixer and PA to guarantee a transmitted signal compliant with the power spectral mask required. An RF switch is used to choose the proper matching network corresponding to the instantaneous transmitted channel.

A duplexer is inherently added to the RF switch to select between the operation in the transmit or receive mode. In the receive mode, the RF switch is tuned to the proper matching network, then it passes the received signal to the LNA. The first down-conversion stage is implemented by the image-rejection programmable BPF and its following mixer. Another down-conversion stage is implemented by another image-rejection programmable BPF and sub-sampling ADC. A Variable Gain Amplifier (VGA) is inserted to adjust the signal level to the optimum dynamic range of the ADC. A detailed description of the critical blocks and their specifications are described next. These are preliminary results for the system design methodology.

4.2.2 Antenna matching circuit

In the multi-board version (Phase I), a single matching circuit is used as an RF switch to switch between transmit and receive modes because multiple matching circuits was hard to implement. This single matching circuit was implemented on the expense of the VSWR of the antenna; leading to lower efficiency at the transmitter side and lower received signal at the receiver side.

For the integrated version (Phase II), it becomes even more difficult to cover the whole new band (30-500MHz) with one matching network. Here comes one of the benefits of the fully on-chip solution. Sub-band matching circuits are used to reduce the VSWR across the whole range of operation. It consists of four matching circuits; each operates at a different frequency sub-band. These sub-bands overlap to cover the entire 500MHz band. Figure 5 shows the effective filtering response of each matching circuits. Switching occurs between them depending on the channel to be submitted and its sub-band and thus its optimum matching network. Similar circuits have been implemented for different antennas rather than different frequencies of operations, but the idea of multiple matching still holds [16]. Matching should be done for maximum power transfer when connected to a 50Ω antenna.

4.2.3 RF Switch/Duplexer

On-chip duplexers are essential blocks when designing a fully integrated transceiver in order to share the antenna. In the multi-board system (Phase I), on-board RF switches are used to multiplex between the transmitter and receiver sides. The switching rate is relaxed since it deals

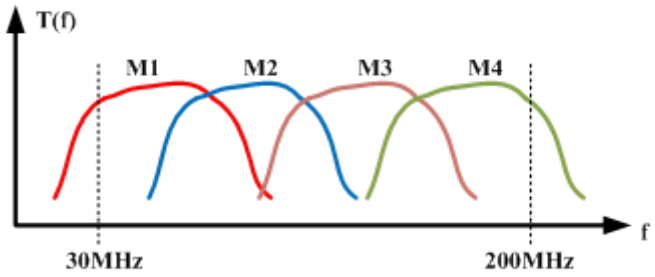

Figure 5: Matching Effective Filtering

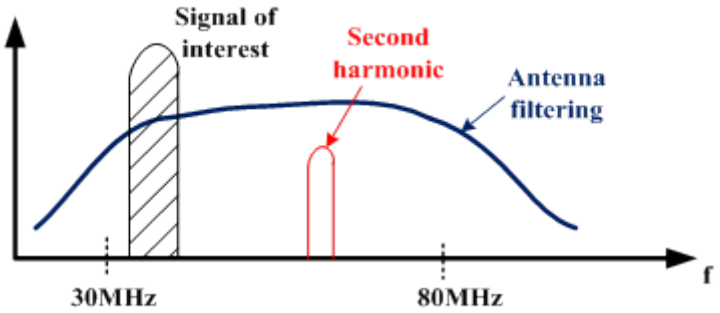

Figure 6: Signal plus Distortion passing through the antenna

with the device speed changing from transmitter to receiver in a half-duplex system. Available commercial RF switches/Duplexers highly distort the signal, thus reducing the transceiver efficiency and reduce the battery life. Low frequency channels are transmitted with their harmonics as it will pass through the antenna effective filtering, as shown in Figure 6. This is not the case in high frequency channels.

In the on-chip version, the duplexer is implemented on chip together with the RF switch required by the antenna matching circuit. RF switch requirements is shown in Table 4.2.3. Super conducting duplexers have been implemented in the literature at the same VHF frequency range [17, 18]. Similar on-chip structure can be implemented.

4.2.4 High-Efficiency, highly-linear power amplifier module

Linearity requirement in the transmitted signal is tight as described before. Harmonic distortion in the output signal is required to be 70dB lower than the fundamental. Power efficiency is also an important metric to the power amplifier block. In the multi-board version described in section 4.1.2, the power amplifier was design on a board level with discrete components using three stages in cascade:

1. Preamplifier stage: amplifies the signal on a low power level. The output power of this stage is in the level of 20mW.

Table 3: RF switch specifications

Metric	Spec.	Units	Comment
Frequency range	30-500	MHz	Whole range of operation
Speed	300	hop/sec	Assuming transmit/receive toggling per hop
Max. attenuation	2	dB	results in 2dB Noise Figure in the receive path
Max. Power transfer	20	W	To withstand the transmitter maximum power

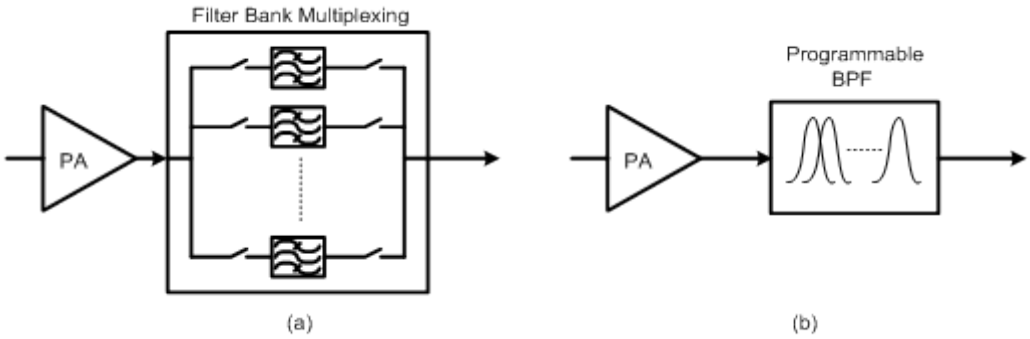

Figure 7: Block Diagram of the proposed power amplifier

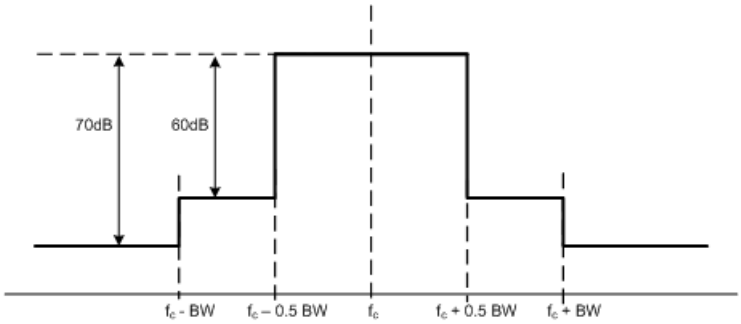

Figure 8: Power Spectral Mask (PSM) of the transmitted signal

2. Power amplifier stage: consists of a class AB power amplifier stage and transmits power in the Watt range. Different power settings are already built in the original system. The efficiency of this stage is lower than 10%.

3. Filtering Stage: a bank of filters following the power amplifier is used to suppress high-level harmonics to satisfy the system requirements. Three filters were constructed with different cut-off frequencies. Multiplexing is done using mechanical relays which are known to be very slow switching components. These relays cannot be used to support hopping, thus one filter is chosen at a time, limiting the hopping range to the filter bandwidth. If the hopping range has to increase, a wider filter is chosen sacrificing the power spectral mask by transmitting higher out-of-band distortion. Hence, other techniques must be used to improve the system performance.

In this on-chip version, efficiency in the range of 30-50% is targeted while keeping the distortion level within the acceptable ranges. A VHF power amplifier with an efficiency of more than 40% is presented by Motorola, Inc. [19]. One of the candidate topologies is the Class-E power amplifier with a bank of switched filters and matching circuits [20]. Once implemented on chip, one programmable filter will be used instead of the filter bank, as shown in Figure 7: Block Diagram of the proposed power amplifier. Switching between different bandwidth settings can be as fast as the hoping rate, hence improving the distortion all the time. The major design challenge in this solution is the expected bulky components especially for the low-frequency ranges. These bulky components will remain off-chip to preserve on the programmability option. Figure 7 shows the expected block diagram of the solution. The power spectral mask of the transmitted signal, derived from the system specifications, is shown in Figure 8. PA requirements is shown in Table 4.2.4.

Table 4: Power Amplifier specifications

Metric	Specification	Units	Comment
Frequency range	30-200	MHz	Whole range of operation
Efficiency	30-50	%	
PSM	Figure 8	dBc	
Modulation Accuracy	99	%	

4.2.5 Receive Chain: LNA, Programmable anti-aliasing filter, and ADC in the receiver

In The multi-board version, the input range is divided into multiple frequency bands as mentioned in section 4.1.5. Sub-sampling is used with different sampling frequencies for different bands to down-convert the analog signal to a digital one using a high-resolution Analog-to-Digital Converter (ADC). Filters are used to avoid aliasing as shown in the figure. Off-chip filters and on the shelf ADC is used for that purpose. Total power consumption of the receiver is 400mW.

The target is to integrate the whole receiver on a single chip. Few ideas can be adopted to improve the receiver performance and reduce the power consumption. Some known competing systems consume less than 200mW in the receiver **(the Israeli counterpart system)**. The target power consumption is below 80mW. System modifications on the architecture will be implemented to optimize the power usage. In the on-chip version, the bandwidth is extended to 500MHz. Using the same architecture will require higher sampling rates for the ADC and higher order filters. Alternatively, a two-step down-conversion is used. The first down-conversion stage uses an image rejection filter followed by the mixer. While the second down-conversion stage uses a higher-Q filter followed by sub-sampling ADC. The first stage divides the entire band into (n) sub-bands, while the second stage divides every sub-band into (m) smaller bands, as shown in Figure 9. In each stage, the more the number of sub-bands, the more the frequencies required by the synthesizer (f_o), the higher the quality factor (Q), the lower the sampling frequency of the ADC, the more relaxed ADC design. System and circuit level simulations will prove and help in finding the optimum number of sub-bands in the receiver.

Optimizing the receiver front-end design will lead to better sensitivity of the receiver. This in turn will lead to smaller transmitted power and hence improve the overall system power consumption. This is beneficial when dealing with handheld devices to improve the battery life time. A similar standard is the TV tuner standard which has almost the same frequency range of operation and deals with the same challenges of wide band. Multiple TV tuners are presented in the literature with 3dB of noise figure in the VHF band and a total power consumption on 203mW [21, 22].

4.2.6 Frequency Synthesizer

Responsible of generating all the channel frequencies and should have a fast settling time compared to the hop rate. It has to generate all frequencies required for stage1 and stage2 down-conversions. The frequency synthesizer will be fully integrated on-chip except of the crystal frequency reference oscillator and loop filter components. Similar frequency synthesizers operating in the same frequency range with 10KHz frequency increment are presented in the literature [23] . Also, others with dual loops and dual Voltage Controlled Oscillators (VCO) are used to cover wide ranges of frequencies in the VHF range [24]. The VCO running frequency will be designed to be different of the PA transmitted carrier frequency to avoid VCO Pulling, especially that the transmitted power is high. I/Q modulation is used to reduce out-of-band spurious emission in the transmit chain and improve image rejection in the receive chain. This

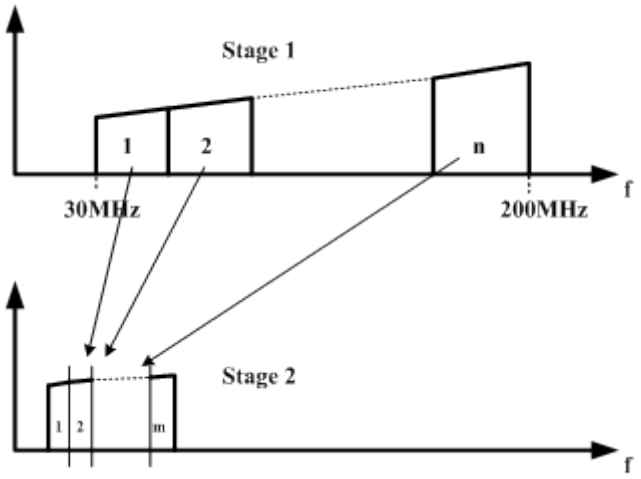

Figure 9: Main Idea of the proposed down-conversion scheme

adds a new requirement to the synthesizer to generate quadrature signals. The I/Q phase mismatch should be below 3 degrees, while the gain mismatch should be below 5% to achieve both the required EVM and the required image rejection.

4.2.7 Received Signal Strength Indicator (RSSI) Unit

Received signal strength indicator (RSSI) is a block in the receive chain detects the power level in any band of interest. This block helps achieve multiple functions on the system level as follows:

1. Listen to channels before transmitting to avoid jammers.
2. Sends feedback signal to the transmitter to reduce/increase transmitted power and thus optimize power consumption if needed.
3. Adjust the receiver gain by controlling the VGA to meet the optimum dynamic range of the ADC.

5 Research Outcomes (Discrete versus Integrated)

One of the targets of this work is to create a fully integrated system of the Manpack device. The outcome of this proposal is intended to be a prototype of an on-chip version of the transmitter and receiver circuits. A huge improvement is expected just by turning the entire system from being a discrete-component-based system on multi-boards to an integrated on-chip system on a single board. In this section we **are showing few advantages we are envisioning from transforming the Manpack system into a fully integrated Manpack system. Advantages include size, security, easy to package and many more things.**

5.1 Size of the final product

As shown in section 4 the original device is built using eight different boards (units). Figure 10 shows a typical Manpack device that was manufactured using a similar technology as our first PCB-based prototype [9]. The size of such device is in the order of a bulky laptop or bigger. In this proposal, the target is to eliminate four of these boards at least. Two more boards can be eliminated as well in the integration but this is outside the scope of this proposal. Our target is to obtain

Figure 10: Original Manpack Device

an equipment in the size of only a hand-held device making it much easier to carry and handle which is important in military applications as well as civilian ones. This reduces the product weight and thus increasing its mobility. This is a very basic feature that is needed by military forces [8]. An example of a reduced weight and integrated solution is already in the market by DYNALOG. It achieved a weight of approximately 1 Kgs and a dimensions 170mm x 45mm x 136mm [11].

5.2 Final product assembly and maintenance

One important aspect in any product is how much time it takes to assemble in the production line and more importantly the time it takes to maintain the device if needed. The more components we have the harder it is to debug in case of failures and the more prone to errors and faults.

5.3 Security

This actually the most important point especially in military environment. As mentioned before the design details must not be known to unwanted parties for security purposes. Knowing the important frequency bands will facilitate the job of a jammer leading to a less secure device. Integration helps in this aspect greatly. A discrete-component device will be easy to test and reverse engineer. All the building blocks are commercial and their data sheets are available. This is considered a very critical weak point in such an application. Enemies can then know all the technical details of the device. On the other hand, a fully integrated system will make the reverse engineering job much more difficult, improving the security of the device. Thus the frequency planning and hoping rates will not be disclosed.

5.4 Power consumption

Since all the building blocks are commercial units and are not designed specifically for this application, they have many general features that are running in the background and is not needed by this application. These unnecessary features are consuming static DC power during operation. Also, each chip has an overhead power management units, Interfaces, and protection circuits that are consuming a constant power during the operation. Eliminating the useless features and reducing all the overhead circuitry to be only in one chip, an expected reduction of 5x of the power consumption is expected in the new system.

5.5 Cost

For mass production, the product cost will drop by 10x. **The major cost is the external components required for each chip to operate properly in spite of its application or architecture (power supply components and AC coupling capacitors). Therefore, the more the chips the more the external components required and thus the less cost-effective solutions. On top of that, the more integrated solution the less the overall silicon cost. (for mass production, the cost per silicon area is not linearly increasing).**

5.6 Performance

1. Signals traveling from one board to another or for long distances on the same board experience a lot of noise coupling from the surrounding environment.

2. The system architecture is designed and optimized based on the available commercial components, not the other way around. This results in a not-so-optimized system for the required application. Different optimum architectures were not implemented due to the lack of the corresponding building blocks.

3. All the system specification can be met and even boosted to a higher level using on-chip implementation.

4. Sub-band matching is feasible in the on-chip solution which improves power transmitted and received levels. This saves power and increases the battery life.

5. Wider range of operation (30-500 MHz) with faster hopping rate increases the security and robustness to jammers.

5.7 On-Chip Solution for the whole transceiver

One of the major issues of fully integrated system solutions is how to share the same chip between noisy and quiet blocks. For example, in our case building the transmitter and the receiver on the same chip is a challenging task. Substrate coupling, noise coupling are all common problems that must be studied in order to successfully put together a complete system. This step is crucial and part of the difficulty is that there are not many CAD tools that accurately model these effects. Hence most of the work will rely on previous experience of the team members and first prototype chip measurements

6 Research Methodology

The problem in hand consists of few challenges that can be stated as follows:

1. Circuit design Challenge: Some of the problems facing the project are circuit design related where proper circuit architectures must be selected to perform the required specification with the lowest cost possible (area, power consumption, etc).

2. Integration issues: One major challenge in the design is to integrate different parts together on a single chip. Noise coupling, sensitivity and many other effects must be studied carefully in order to have a complete on-chip solution without sacrificing performance.

3. Fabrication and Testing: This is concerned with the layout of the system that will be sent for fabrication at one of the international foundries. Testing is a non-separable task from the design and layout of the system since this is the ultimate goal. Testing needs to be planned properly in order to facilitate the debugging process. The system must be testing using some high-tech equipment and will be conducted using printed circuit boards as means of integrating with the external world.

In order to achieve that, CAD tools will be used extensively through-out the project. Tools that will be used do include Cadence and Mentor tools for simulation, layout and PCB fabrication. Cadence tools licenses are purchased and available through a deal with Europractice.

A top-down design methodology provides the following benefits: First, it will establish the feasibility of design goals early in the design cycle before significant expenditures are made. Second, architectural exploration is feasible where block parameters are determined so as to optimize overall system performance. Third, different alternative implementations of each block can be evaluated and decided. The fact that the implementation of each block is verified in the context of the whole system accentuates the role of the system model as a formal communication medium among the physically far designers involved in the project so that interface problems, that appear only late during integration or assembly of blocks, are eliminated. Design time is reduced because blocks can now be designed in parallel. Changes are facilitated because their impact can be readily evaluated using the system model. The behavioral model should be "pin-accurate" and should account for some effects as: process variations, supply and device noise, and environment conditions (e.g. temperature).

In this work the PI and co-PIs will be responsible to prepare the top-level system specifications and lead all the efforts in all block levels as well as system-level integration. Beside the PI and co-PIs, a full-time research assistant will be trained to lead the project and be responsible of all minor and major details. Such a project with such depth needs a very systematic methodology to achieve the target system in the target time frame. In this section we are presenting our research methodology while mentioning some design milestones.

6.1 Top-level system design and modeling in Cadence

A top-down design approach will be used in this project. Circuit requirements will be extracted from the system level design to match the chip design capabilities. Different architectures will be studied, compared and considered to accomplish the required specifications on chip. This phase consists of system level simulations as well as some small-scale circuit simulations to prove the usability of the different ideas. New ideas will be developed on the system level to satisfy the requirements while minimizing the system complexity. This phase is the heart of the project since it serves as the foundation of the whole project. Verilog-A models will be used to model all blocks in order to facilitate coming tasks.

In this phase, the exact architecture will be outlined taking into consideration the input from the systems group. The PI and both co-PIs will lead this effort with the help of the full-time RA in the systems side and one part-time researcher in the circuits and modeling side.

Expected duration: 3 months

6.2 Schematic and Circuit design

Schematic/Circuit design phase is responsible of the implementation of the system level architecture and will transform it into feasible and optimum circuit design solutions. Innovations on this level are also required to produce a feasible, small-area, low-power, low-complexity design. Low power techniques will be employed to mitigate these issues. Schematic circuit design will be performed by Cadence tools (spectre). At the end of the design of each block, a thorough design review will be conducted by the whole team to further improve individual circuit designs.

This phase is the core of the whole project. Each block will be investigated and designed. Four tasks will be designed in parallel. Each task will be led by one of the professors guiding one of the researchers as shown in Table 10. Each circuit will be designed and simulated under corners and different scenarios. These tasks are summarized as:

- **Power amplifier and RF switch**
- **Filter banks of Tx and Rx paths and Variable-gain amplifier (VGA) of the Rx path.**
- **Low-noise amplifier (LNA) and Mixer for the Rx path.**
- **Analog-to-digital converter (ADC) in the receiver path.**
- **Digital-to-analog converter (DAC) and a frequency synthesizer for both the Tx and Rx paths. An extra task will be built upon availability. We believe that these two blocks only require engineering effort rather than research. PI and co-PIs have extensive experience in these areas and can accomplish the designs themselves without the help of the researchers if needed.**
- **Risk mitigation plan: Each building block will be designed and placed in the system with enough observable points (points of measurements) to be able to test the block separately and characterize its performance. Enough controllable points will be added as well to be able to bypass the faulty block and continue with the whole chain characterization.**

The work in this phase will be conducted by the junior researchers under supervision of the PI and co-PIs.

Expected duration: 7 months

6.3 System Integration on Transistor Level

After individual blocks design, the integration phase will start right away. System level simulations where all blocks are used on a circuit level. Simulations will be performed using Cadence transistor simulation tool (spectre). In this phase, layout floorplanning will be developed where

special care must be taken to isolate different blocks and to optimize critical path in the chip, minimize layout parasitics effect on the system performance. This step is crucial since this is what gets fabricated rather than what is simulated under ideal conditions.

PI and co-PIs will have a greater role in this phase since this is a step that requires more experience in detecting potential realistic problems/issues not caught in simulations.

Expected duration: 2 months

6.4 Chip Layout

In this stage, the layout of the individual building blocks will start. The layout of each block will be the responsibility of the schematic designer of that block. Layout check tools, such as DRC (design rule check) and LVS (layout versus schematic) will be performed to make sure that the layout meets the foundry rules and that the layout exactly matches the block schematics. The layout will be performed using Cadence layout tools. Similar to the circuit design phase, layout will undergo thorough design reviews to improve the overall quality of work.

Similar to system-level integration, layout is a process that requires experience to avoid corrupting the circuit performance without catching it in simulations. Different blocks have different issues in layout. For example, noise isolation, parasitic estimations are very critical in the RF part of the system. Layout matching is extremely critical in the layout of ADCs, and so on. System integration is as crucial as the individual block layout since these are errors that are usually not modeled in schematic simulations and can only be prevented rather than simulated.

Expected duration: 4 months

6.5 Post-layout simulation of the individual blocks and the whole system

After the layout of each block is completed, the parasitics of the layout will be back annotated to the schematic so post-layout simulation can be performed. Degradation in block performance will be quantified and check if blocks specifications are still met with sufficient margin. If one of more of the block specifications is no longer met, further tuning of design parameters will be needed. Block post-layout simulation will be performed using Cadence schematic and simulation tools. Chip post-layout simulations is usually not attainable due to the size of the project. We usually omit this step or use a simplified procedure instead.

Expected duration: 1 month

6.6 Submission of layout file (GDS) for fabrication and PCB preparation

The GDS-II file of the system layout will be generated to be submitted to the foundry for fabrication. The fabrication cycle usually takes 3-4 months. During this period, the team will take the necessary steps to prepare for the measurement phase for the individual blocks and assemble different external components necessary for the blocks operation. This phase is a very good opportunity to document most of the design details for future purposes as well as to include in the final report.

Expected duration: 3 months

6.7 Chip Measurement

The chip turn-around time is in the time frame of 3-4 months. Few of the team members will be responsible of testing each individual block, characterize it and compare its performance with the simulated one. Measurement of the whole system is also done in this phase to compare the performance with the expected one and propose solutions for any mismatch. Debugging the circuit in the lab is one of the most challenging tasks since probe points are very limited.

Expected duration: 3 months

6.8 Report Writing and Documentation

In this phase a complete documentation of the system will be done. These documentations will help improve our design process for future projects. Report writing and documentation can be done in parallel with the PCB preparation step.

Expected duration: 1 month

7 Project Impact

This project is of great use for the Egyptian community. Apart from the many applications that will be mentioned in the marketing analysis section 13, the first version (described in section 4) of this project has been developed in collaboration between our department and the "arming and reinforcement section" in the Egyptian military (2003-2011). In the past, such Manpack devices were imported from foreign countries where all coding and security protocols remain unknown to the Egyptian side. The project mentioned above was able to provide the same module to the Egyptian army with more competitive prices and at the same time keep the know-how and security modules built in house. Many phases are already executed including product sampling, field testing and final production phase already started.

The main problem of the existing 100%-Egyptian-made solution is that volume and complexity of the system since all circuits are built using discrete components on printed circuit boards. This causes difficulty in reproducing the module as well as difficulty in improving and upgrading the system.

This proposal in intended to:

- Provide a much more efficient Manpack system than the one already existing. Improved frequency ranges are targeted.
- Improve the form factor of the final product by reducing the internal component number and sizes though integration.
- Lower the cost of the solution
- Increase the productivity volume by simplifying the module

Support letters from Egyptian army officials and Egyptian authorities can be furnished upon request.

8 Work Packages and Gantt Chart

Work in this project is divided into work and logical packages that are tied together with strong ties. Each package is self-sustained based on the results of the previous ones. Most time periods ends with a report that summarizes the findings and results of the work done. A final report at the end of the project will describe in details all the results (simulations and testing), documentation and manuals related to the work done in the project period.

Work can be summarized as follows:

1. Top level system design and modeling in Cadence
2. Block-Level Circuit Design and Simulation
3. Layout, Post-Layout Simulations and 1st PCB Design
4. Transistor-Level System Integration 6.3
5. Measurements and Characterization of the first Chip and Layout of the Final Chip
6. Final PCB Design, Fabrication, and Documentation
7. Final Measurements and Characterization and Paper Writing

Table 5 shows the work distribution over the span of 24 months (project duration) and the deadlines for submitting the period reports. Different milestones are shown. In the first year, most of the architecture and circuit design challenges will be solved. In the second year, fabrication, testing and integration issues will be faced and tackled for sub-blocks level and system level.

Table 5: Gantt Chart

	Tasks/ Activities	Start	End	Duration (Days)	% Completed	Working Days	Days Complete	Remaining Days	September-12	October-12	November-12	December-12	January-13	February-13	March-13	April-13	May-13	June-13	July-13	August-13	September-13	October-13	November-13	December-13	January-14	February-14	March-14	April-14	May-14	June-14	July-14	August-14
	Tasks/ Activities	Start	End						Month 1	Month 2	Month 3	Month 4	Month 5	Month 6	Month 7	Month 8	Month 9	Month 10	Month 11	Month 12	Month 13	Month 14	Month 15	Month 16	Month 17	Month 18	Month 19	Month 20	Month 21	Month 22	Month 23	Month 24
1	**Top level system design and modeling in Cadence**	M1	M3																													
1.1	System Level Architecture Choices	M1	M1																													
1.2	Verilog-A modeling	M2	M2																													
1.3	System Level Simulations	M2	M3																													
	Report 1	M3	M3																													
2	**Block-Level Circuit Design and Simulation**	M4	M0																													
2.1	Individual Block System Architecture Study and Choice	M4	M5																													
2.2	Schemtic and Circuit design and Transistor-level simulations on block level.	M5	M9																													
2.3	Corner Simulations and Statsitical Analysis	M10	M10																													
3	**Transistor-Level System Integration**	M11	M12																													
3.1	Transistor-Level System Simulations	M11	M12																													
3.2	System modifications to meet the required specifications	M12	M12																													
	Report 2	M12	M12																													
4	**Layout, Post-Layout Simulations**	M13	M17																													
4.1	System Layout Floorplanning	M13	M13																													
4.2	Individual Block Layout and Physical Verification	M14	M15																													
4.3	Full Chip Integration	M16	M16																													
4.3	Post Layout simulations	M16	M17																													
	Report 3	M17	M17																													
6	**PCB Design, Fabrication and Documentation**	M18	M20																													
6.1	PCB Design	M18	M18																													
6.2	PCB Fabrication	M19	M19																													
6.3	PCB Assembly	M20	M20																													
6.4	Documentation	M18	M20																													
4	**the Chip**	M21	M23																													
5.1	Functionality Testing of Individual Blocks	M21	M21																													
5.2	Performance Testing of blocks and System	M22	M23																													
5.3	Debugging possible errors	M23	M23																													
	Report 4	M23	M23																													
6	**Final Stage**	M24	M24																													
6.1	Paper Writing	M24	M24																													
	Final Report	M24	M24																													

9 Management Team

This project will conducted under the supervision of a high-profile team from Electronics and Communications Engineering Department, Faculty of Engineering, Cairo University. Along with four full and part time graduate research students who will be working and helping in the project, three professors with different skill sets and expertise will be leading the project.

Professor Dr. Magdi Fikri, B.Sc. 1963 Cairo University, M.Sc. 1970 Cairo University and PhD 1978 from Bradford University, UK. Dr. Magdi Fikri is an expert of telecommunications systems and served as the PI for more than ten successful research and industry projects mostly in cooperation with different Egyptian institutes (military and civilian) as well as different NTRA, ITAC and Schlumberger projects. Dr. Magdi's research interest include Speech and image signal processing. - Wireless Communication Systems. - Signal Processing for Communications. - Software Defined Radio - Power Line Communications. - Microprocessor applications in measurements and control and Digital communication systems. He occupied numerous important positions in Egypt and acted and the consultant of many important projects well. See more details in the short Curriculum Vitae attached.

Dr. Mohamed M. Aboudina, B.Sc. 2000 Cairo University, M.Sc. 2002 Cairo University and PhD 2008 University of California, Los Angeles. Dr. Aboudina is currently an Assistant

Professor at the Department of Electronics and Communications at Cairo University, Egypt. He has PhD in integrated circuits and systems from University of California, Los Angeles (UCLA). He has large industrial experience in the design of Analog circuits; specifically oversampling ADC for high-speed and high-resolution applications, Nyquist-rate data converters, high-speed analog building blocks for hard drive read channel applications and power management units (DC-DC converters and LDOs). He has more than 7 years of industrial experience in US companies (Marvell, Newportmedia Inc., Mentor Graphics and Vidatronic, Inc.). He is an IEEE member and has several published conference and journal papers.

Dr. Faisal A. Hussien, B.Sc. 2000 Cairo University, M.Sc. 2003 Cairo University and PhD 2009 Texas A&M. Dr. Hussien is currently an Assistant Professor at the Department of Electronics and Communications at Cairo University, Egypt. He has PhD on analog and mixed-signal circuit design from Texas A&M University (TAMU), Texas, USA. He has more than 5 years of industrial experience in US based companies (Texas Instruments, Dallas, TX and Vidatronic Inc.). He has extensive experience in power management circuits (LDOs and DC-DC converters). He worked in RFID passive tags as one example of batteryless circuit. He has 4 journal and conference papers. He is an IEEE member.

10 Management Structure

Table 6: Management Structure

Task Name	Advisors	Researchers
System-Level Design	Dr. Magdi Fikri Dr. Mohamed Aboudina Dr. Faisal Hussien	RA1
System-Level Verifications	Dr. Faisal Hussien Dr. Mohamed Aboudina	RA1
Power Amplifier	Dr. Faisal Hussien	RA1
Tx Filter Banks	Dr. Faisal Hussien Dr. Mohamed Aboudina	RA1
Matching Network	Dr. Faisal Hussien	RA2
Rx LNA and mixer	Dr. Faisal Hussien Dr. Mohamed Aboudina	RA2
Rx Filter banks	Dr. Mohamed Aboudina	TA1
Rx ADC	Dr. Mohamed Aboudina	RA3
Frequency Synthesizer	Dr. Faisal Hussien Dr. Mohamed Aboudina	TA2 + RA4
DAC + upconversion mixer	Dr. Mohamed Aboudina	TA3

11 List of Deliverables

11.1 Legalities with NTRA

We have talked to NTRA personnel regarding the legalities and ownership of the IP of this project by the end of it. They expressed flexibility in this regard given the confidentiality of the project details and information.

11.2 Deliverables

This project can be divided into few milestones. Each one can be considered a deliverable. In this section we present these milestones with the expected dates of submission in Table 11.2.

Table 7: List of deliverables

Month # 6	System Level Architecture Design with all required block specifications and intial circuit architectures with preliminary results.
Month # 12	Circuit level architectures, design and transistor-level simulations of all blocks. Report will include corner simulations under different design conditions (Supply variations, temperature variations, device models ... etc).
Month # 18	Top-level simulations, Chip Floorplan, block-Level Layout, Top-level layout, post-layout simulations and GDS of the sent chip.
Month # 24	Final System Measurement Results of the fully integrated transceiver. The report will be showing the results obtained from the bench testing and comparison with the simulations expectations and Final Report.

12 Required Facilities

The Research project will undergo many phases; each requires its own tools/facilities to be appropriately executed. In all the phases, office space is required and is already available.

1. System level design phase: Software tools:
   (a) **Matlab/simulink (Required).**
   (b) **Elanix Systemview (Required).**
2. Circuit design Phase. CAD tools required:
   (a) Circuit level simulator – Cadence Virtuoso schematic entry and Spectre/APS simulation tool (Available).
   (b) Layout Virtuoso editor by Cadence tool (Available). Cadence tools are available via Europractice-IC to our department for research and teaching purposes. So, its budget is not included.
3. Testing Preparation Phase: PCB fabrication tools:
   (a) PCB schematic and layout Editor (Available).
   (b) PCB fabrication Machine (Available). PCB tools are available in in the department for research purposes. So, its budget is not included.
4. Characterization Phase:
   (a) Power supplies and Signal Generators (Available)
   (b) Network analyzer for filter characterization (Available)
   (c) **Logic Analyzer for ADC characterization (Required)**
   (d) Spectrum Analyzer for PA characterization (Available)

13 Market Analysis and Business Plan

13.1 Viable Customers

13.1.1 Army

CU-COMM is the market name we chose for the frequency hopping Manpack system. The Egyptian Army is CU-COMM's main customer. This is because it is one of the essential elements of the battle. No communication among soldiers in the battlefield means their death. Therefore, a reliable, secure, wide range, light weight, and low power telecommunication transceiver is a must for them. In addition to that, it is considered as a matter of national security to them to have such a sensitive device designed inside Egypt. That is to avoid the risks of various intrusion ways that may be attached to any commercially imported device. Tracking of such transceiver is a piece of cake for its designer. CU-COMM may be considered a start for a long road of innovation in the Egyptian army. That is due to the fact that most of the recent military applications depend on a reliable, secure, wide range, high data rate communication link available to be set between the base and any unmanned vehicle, small robot, or even aircraft. So, having a nationally designed transceiver gives the push for such further development. Other friend countries present also viable customers to the product.

13.1.2 Oil Fields

No doubt that Oil industry in Egypt is one of the most important businesses. That is in addition to our neighboring fields in the Arab Gulf. Any Oil field operating company needs special telecommunications solutions whether in sea or land. Such solutions are like man-to-man communication inside the field which is usually out of urban telecommunication services coverage. Headquarters-to-field communication is also a major problem that faces such organizations. Such communication may be manager-to-operation member or Control Room-to-Oil field machinery. CU-COMM is considered a very low cost solution for such problems especially in case of using civilian specifications other than that of the army. We mean by civilian specifications less power levels in order to avoid interference with neighboring users, i.e. other Oil field companies. Low cost is relative to the two-way communication system alternative that costs them constructing communication towers, regular maintenance, power generators... etc.

13.1.3 Ambulance and Fire Fighting Vehicles

They use it to provide coverage for them in suburban areas where there is no signal for the ordinary two-way radio communication systems.

13.1.4 Entertainment

It may be used also in applications like in Safari rides and Close-to-Shore Sea cruises. Most of these activities are done in places disconnected from the world and the only solution to connect to others is by satellite phones that may be considered very expensive. So, CU-COMM comes with a low cost and easy to use solution to such problem.

13.2 Customer value related to service innovation

Table 8: Customer Value

Customer Value Elements	Implementing to CU-COMM
Results Produced for the Customer	At the end of the day, the customer will be satisfied that he was able to fulfill his needs in his telecommunication transceiver: • security via frequency hopping, • wide coverage via VHF range usage, • high data rate via multiple channel usage, • low cost via lowering its cost 10x, • small size via chip-wise design, and • low-power consumption via on chip power consumption decrease techniques.
Product Quality	All the above mentioned needs are satisfied in addition to the high quality design and most important the inherent quality for the military partner of having such a sensitive device to be designed in Egypt.
Price to the Customer	Product price which is aimed to be in the range of 4000-5000 EGP
Costs of acquiring the service	Zero as there's no costs of acquiring that product except of its price
Customer Value	$\frac{Results Produced for the Customer + Process Quality}{Price to the Customer + Costs of acquiring the service}$ Since the numerator is much more than the denominator, the received value will be high in the range of 10 k

13.3 Four P's for Marketing the Product

Table 9: Marketing Four P's

Product	
Brand Name	CU-COMM
Features	Fully Integrated Frequency Hopping Man-Pack Transceiver
Packaging	Reinforced metal chassis for Military usage
	Light weight polymer chassis for civilian applications
Quality level	It's very high to achieve maximum fulfillment for the main customer (the Armed Forces).
Returns	It's allowed only in case of first calibration failure.
Services	Maintenance is insured for civilian users in the first year from purchase date.
Sizes	One size is available.
Warranties	Warranty is given all customers purchasing it from the mass production facility which is aimed to be one of the army's facilities.
Price	
Discounts	5% - 10% in case of mass bargains
List price	10000 – 15000 L.E.
Place	
Business Partners	Chip fabricator (blind manufacturing), NTRA (development sponsor), and the Armed Forces (mass producer)
Channels	Direct market on the roads and through multimedia (internet and TV)
Distributors	Armed Forces Production Organization Facilities
Inventory	50% of demanded quantity is always available to avoid any shortage on delivery to agents
Locations	Armed Forces Production Organization Facilities
Promotion	
Advertising	Advertising through the internet
Customer Service	It's provided on demand with extra cost like preliminary technical training
Direct Mail	It's sent to Oil companies, allied countries

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