

Analog Integrated Circuits

Lecture 5,6: Layout Considerations

ELC 467 – Spring 2013

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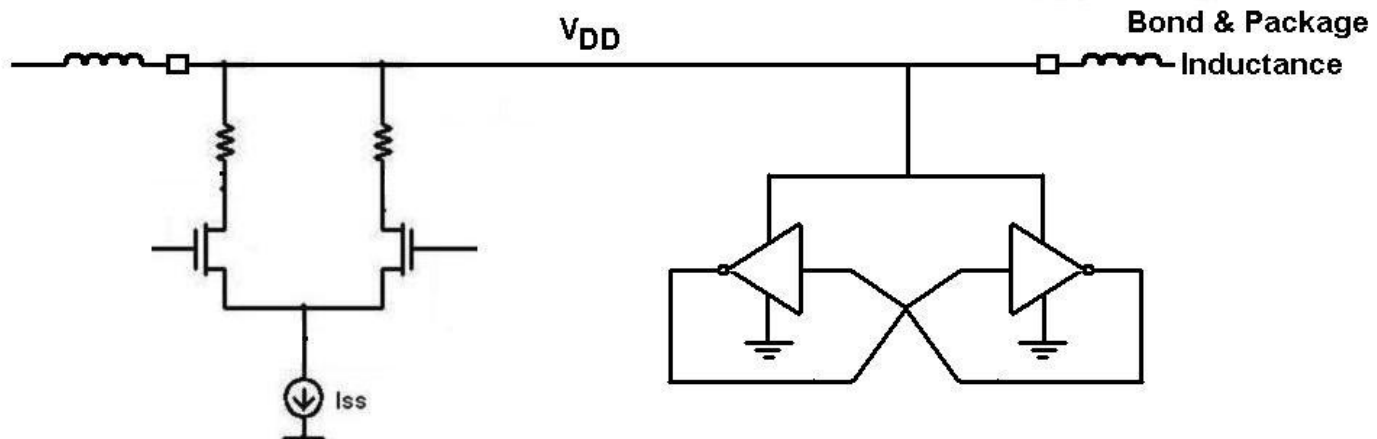
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Outline

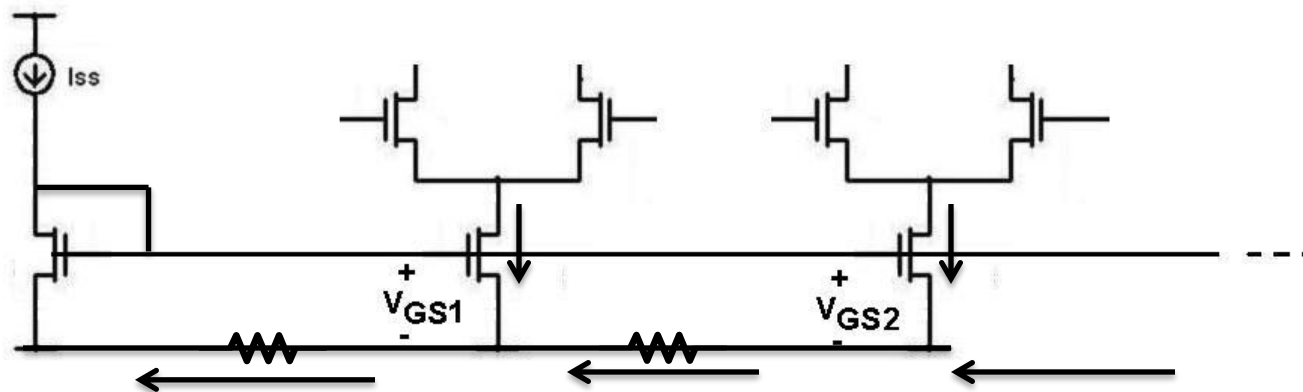
- Layout Considerations
 - Basic Issues
 - MOS Layout
 - Matching
 - Guard Rings
 - Shielding
 - Output Buffers
 - Floorplanning

Analog vs. Digital Supplies



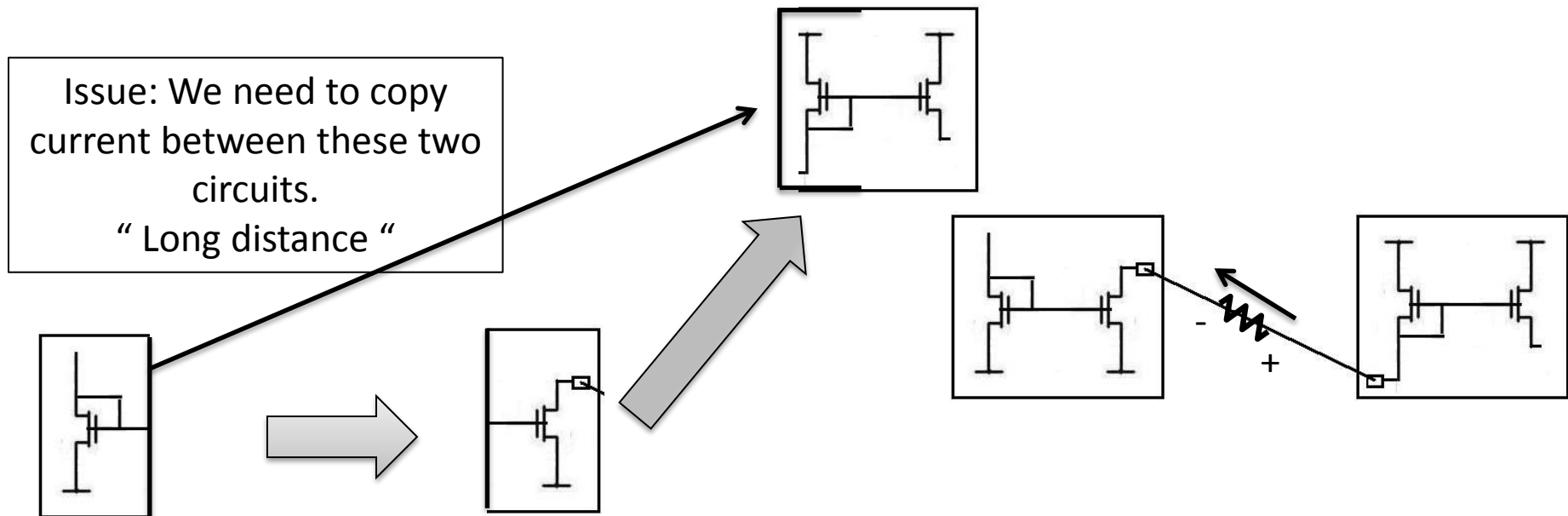
- If Digital is switching at high speeds, it might be favorable to separate analog and digital supplies.
- What about analog and digital ground pads?
 - Different grounds might experience different circuit transients → Different “Ground Bounce”.
 - If we have a signal going from one domain to another (referred to one ground), the signal might be interpreted wrong if the second ground has drastically different ground bounces.
 - Proper level shifters must be used because both grounds will not track each others noise/ripples.
 - Level Shifters are only used for digital signals.

DC voltage drop



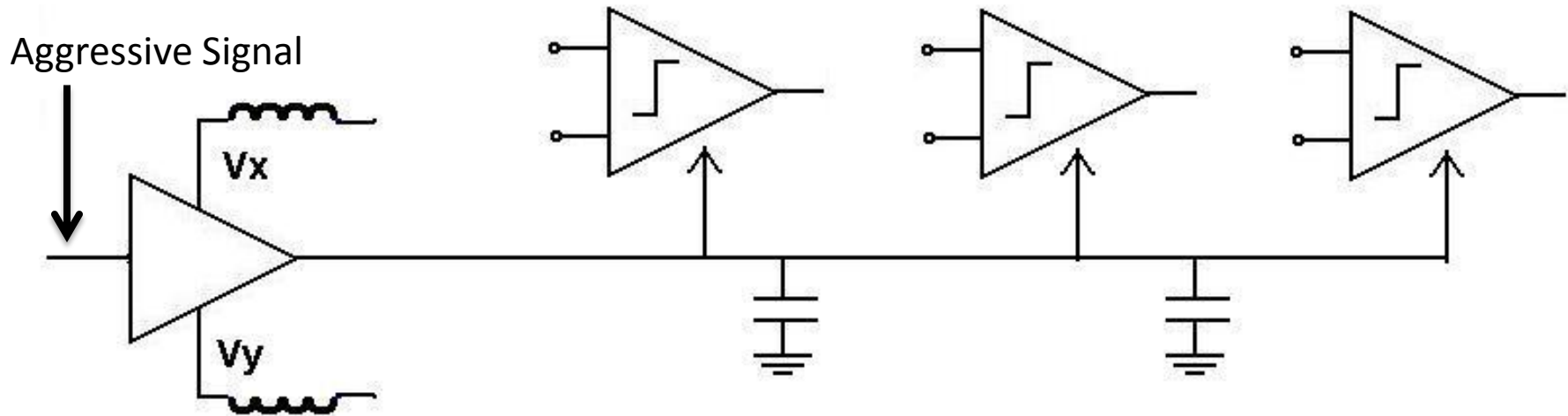
- VSS voltage gradient can cause systematic errors between different current source values.
- In the above circuit, the ideal case would be that all current mirrors carries the same current value, but due to the IR drop this is not happening.
- **Question: In General, should we route voltage or current between the current source and the mirror?**

DC voltage drop



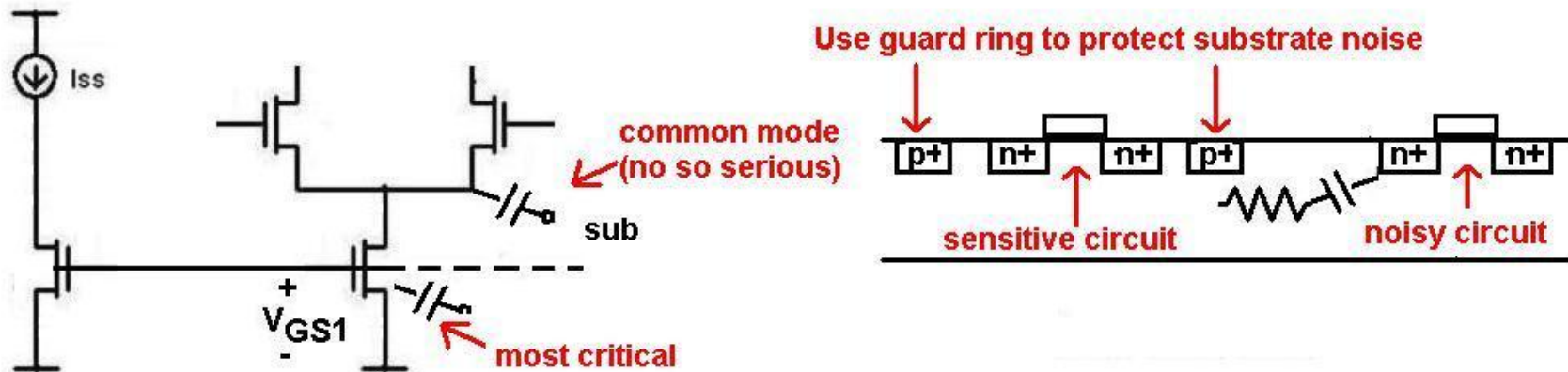
- Question: In General, should we route voltage or current between the current source and the mirror?
- Where should we place the circuit in the middle? Close to which of them?
- **Important: Voltage is always referred to another node (reference) while current is not !!**
- Answer: Route the current.
- Which Transistor gets affected if we have an IR drop in the long connection?
 - Bottom Transistor → Can go out of Saturation → Current value will be incorrect.

Substrate Coupling



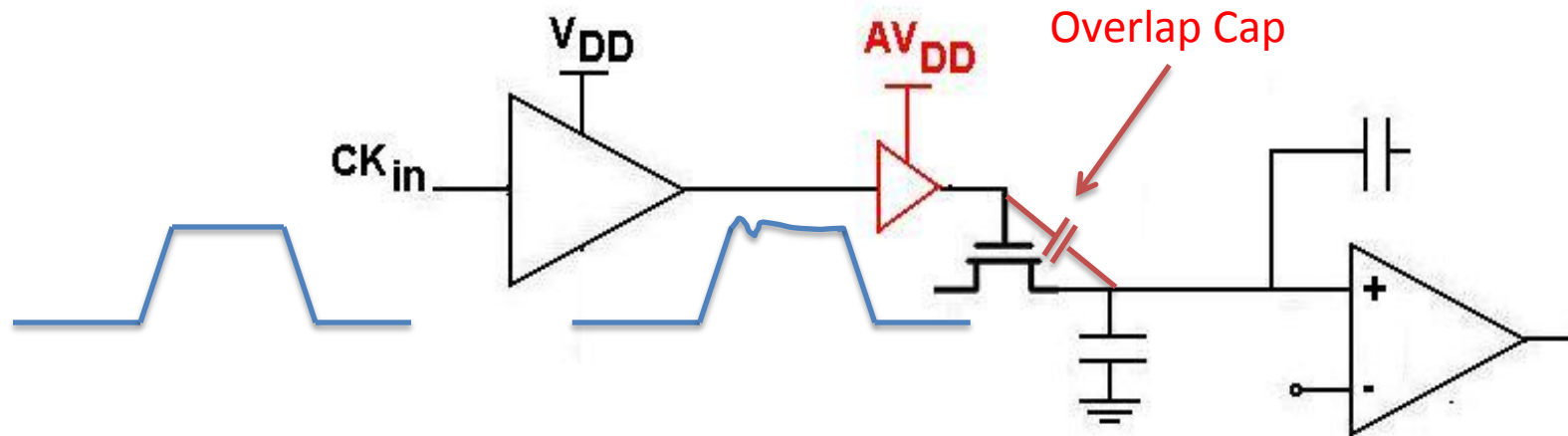
- Clock traveling from the clock driver to all circuits on the chip might cause noise (glitches) injected to the substrate.
- Substrate is common between all circuits (analog and digital).
- Noise will couple from the source of noise to all circuits.

Clock Noise Coupling – Substrate Coupling



- Different arguments for connecting substrate (Substrate ties/contacts and NWELL ties/contacts) to analog ground and digital ground. Not clear. But the best way is to have a low-inductance connection to substrate.

Clock Noise Coupling – Supply Coupling



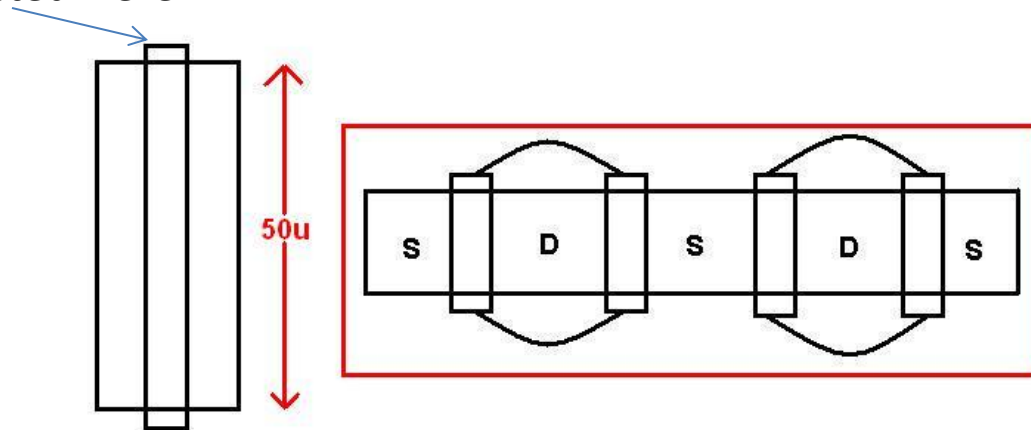
- Buffers used to buffer strong digital signals are usually very noisy and contribute heavily to the bounces/noise to their supplies (V_{DD}).
- In circuits like switched-capacitor circuits that use clock as one of the inputs are usually very sensitive to noise.
- Using CK signal directly from the noisy buffer (V_{DD}) will cause noise from the noisy clock signal to couple to the sensitive circuit through any parasitic cap like the overlap capacitance.
- Solution: Need a buffer from a clean supply (AV_{DD})

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- MOS Layout
- Matching
- Guard Rings
- Shielding
- Output Buffers
- Floorplanning

Gate Resistance

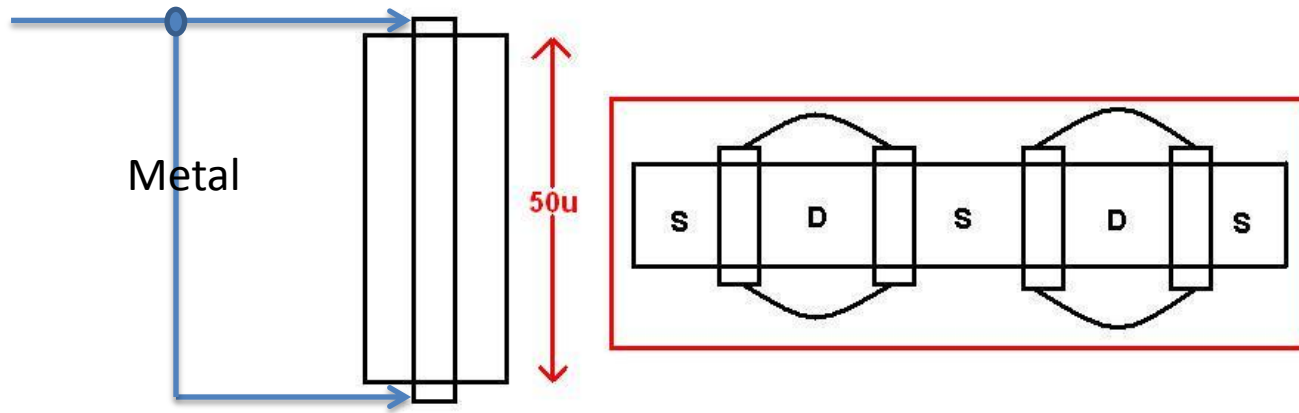
Signal Connected Here



- Gate resistance is critical when choosing number of fingers.
- If the signal is connected to the top side, and since the gate has a capacitance to ground
 → Signal Experience Delay to reach the other side of the gate.
 - $R_{gate} = R_{sheet} \times \text{No of squares} = R_{sheet} \times \frac{W}{L}$.
 - $C_{gate} = C_{ox} \times WL$
 - $\text{Delay} = \frac{R_{gate} \times C_{gate}}{3}$
- Gate is made of Silicide poly (~8-10 Ohm/square) – Minimum possible poly resistor
- Routing Poly (outside of the transistor) is made of non-silicide poly (~ 300 Ohm/square)
 – Best possible resistor in most technologies. (linear and match relatively well).

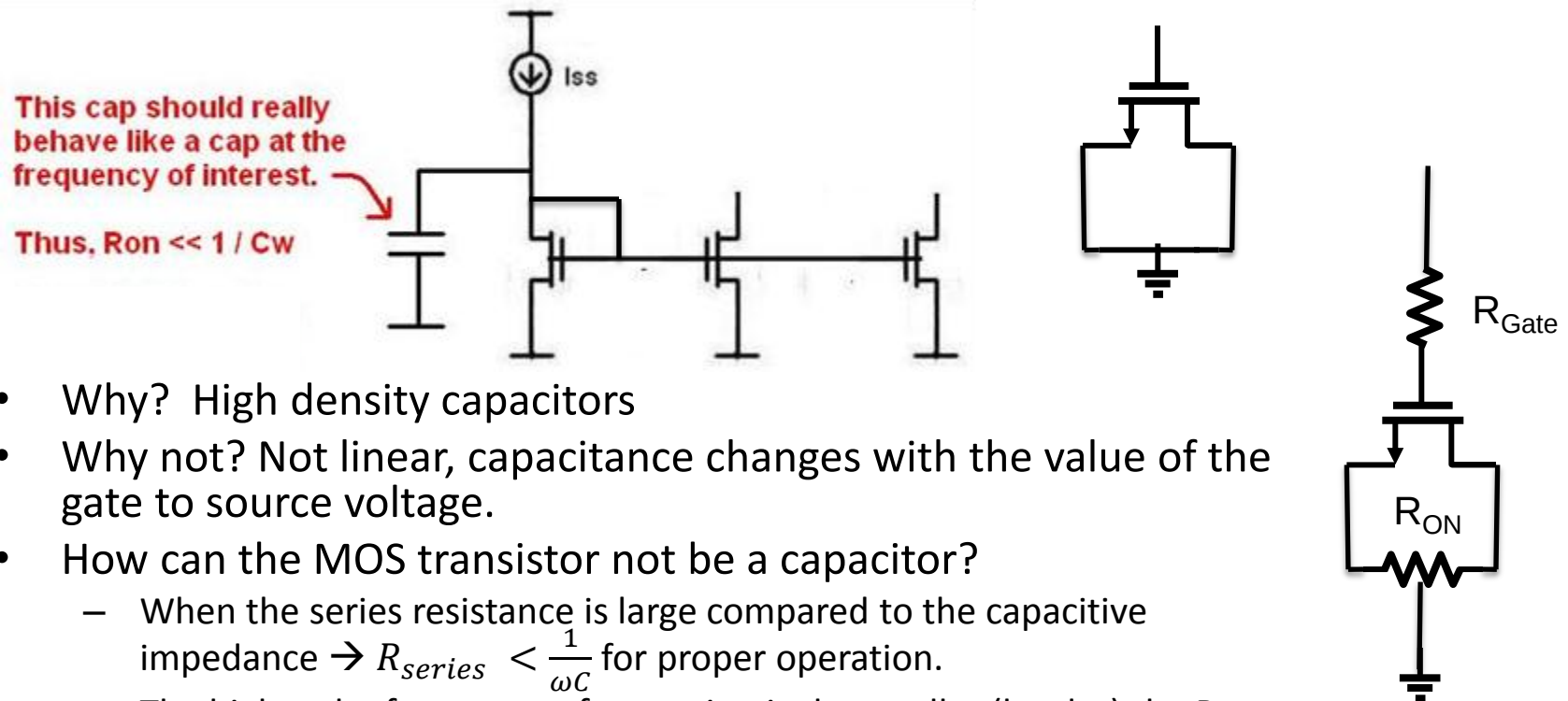
Gate Resistance

Signal Connected Here



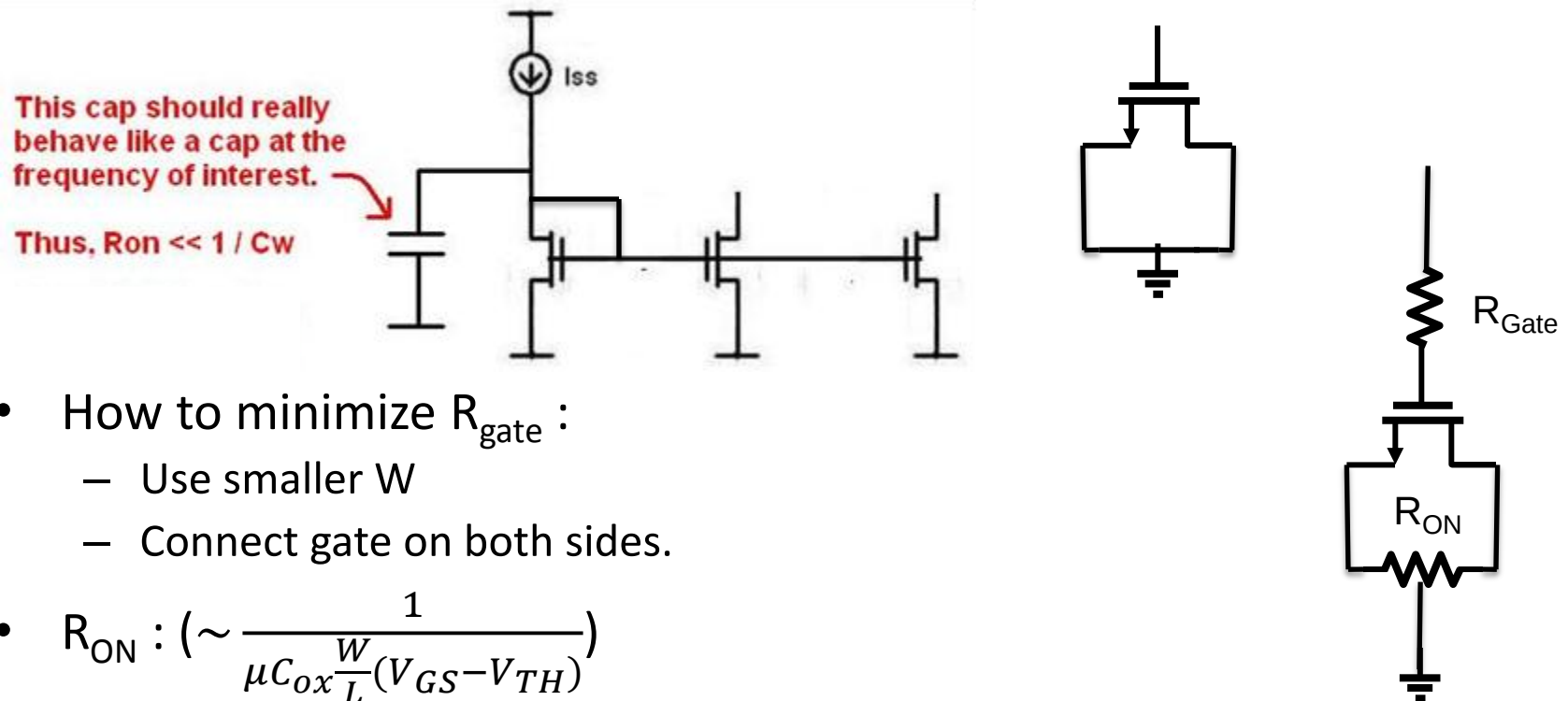
- How to reduce this delay effect?
- Option 1: Connect the same gate from both sides using a Metal layer (very small resistivity $\sim 50\text{mOhm/quare}$)
 - Worst case delay: $Delay = \frac{R_{gate} \times C_{gate}}{12}$ (@ the middle point).
- Option 2: Split the single finger into multiple fingers (total $W = W_{\text{finger}} \times \# \text{ of fingers}$) $\rightarrow$ Worst case resistance reduces linearly with the number of fingers.

MOS Transistor working as a capacitor



- Why? High density capacitors
- Why not? Not linear, capacitance changes with the value of the gate to source voltage.
- How can the MOS transistor not be a capacitor?
 - When the series resistance is large compared to the capacitive impedance $\rightarrow R_{series} < \frac{1}{\omega C}$ for proper operation.
 - The higher the frequency of operation is the smaller (harder) the R must be.
- Resistive components:
 - Gate Resistance (R_{gate})
 - Channel Resistance (R_{on})

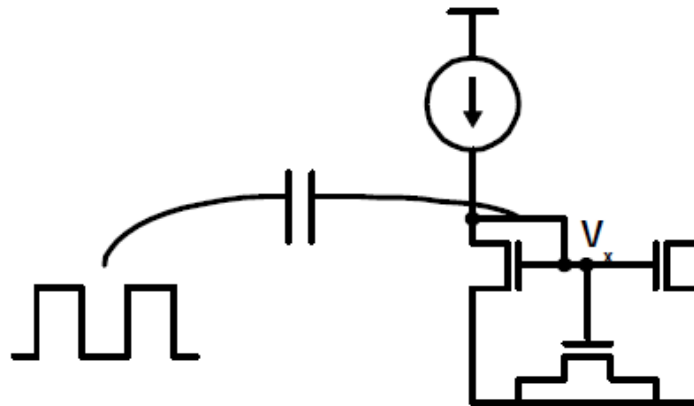
MOS Transistor working as a capacitor



- How to minimize R_{gate} :
 - Use smaller W
 - Connect gate on both sides.
- $R_{ON} : (\sim \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})})$
 - For a fixed gate capacitance: Use smaller L
 - Effective resistance = $R_{ON}/12$
- $R_{series} = \frac{R_{Gate}}{12} + \frac{R_{ON}}{12}$

MOS Layout

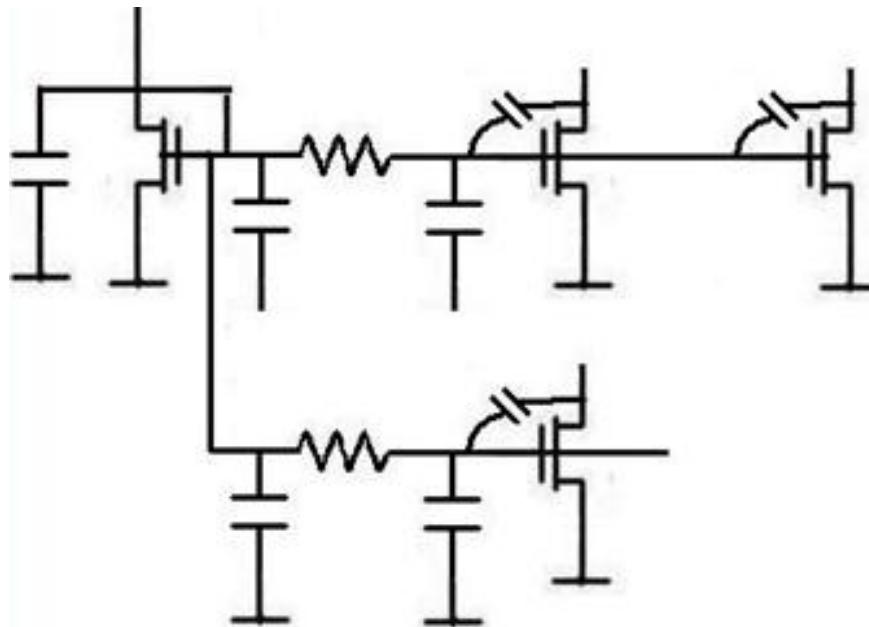
MOS cap.



- What if noise couples to this Gate point, Do we need Fast or Slow settling?
 - Do we add so much capacitance at this node to make it hard for the node to move?
 - Or, Do we remove all the cap and reduce the node resistance so much ($\frac{1}{gm}$) to allow it to recover fast.
- If noise is random: we need to add as much cap as possible.
 - Slow settling
- What if noise deterministic:
 - We can design the node to be fast and settle quickly.
- In case of the slow settling (with cap), and the existence of bond wire inductance in the ground wire ringing in the gate node might exist (underdamped second order system)
- sometimes deliberately choose a low Q capacitor (allow for R_{series}) to dampen ringing due to bond wire inductance at ground bond wires.

MOS Layout

Bias lines



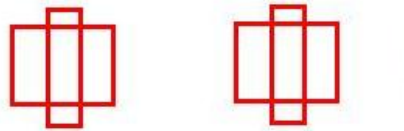
- To reduce the amount of parasitic coupling, insert resistors on bias lines. (RC filter)
- Issue: R must be very large. Not area efficient !!

Outline

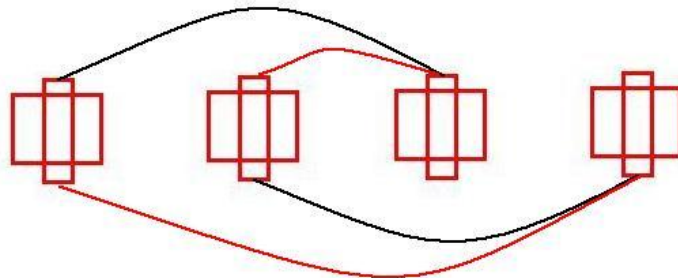
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Matching Introduction

- Transistors poorly match if placed in random positions.
- Transistors must be placed in the same orientation.



- Make the surroundings of transistors the same.
- Cross connect to cancel linear gradients.
- Linear gradient is a slight change in transistor parameters that happens either in the x-direction or in the y-direction or both (mainly due to oxide thickness and doping gradient errors)



Which connection (red or black) is less sensitive to mismatch?

Common Centroid (Any component)

- Determine groups of matched components
 - Depends on circuit function
 - All transistors in a mirror
 - Diff-pair and load in an amplifier
- Divide into segments
 - Based on unit elements, if there is a common divisor
- Coincidence
 - Center of all matched devices should coincide, at least approximately
- Symmetry
 - Along X and Y axis.
 - Symmetry lines of “ABAB” pattern do not line up! (A and B represent fingers of transistors, resistors, capacitors, or any matched components).

Common Centroid (Any component)

- Dispersion
 - Segments of each device should be distributed throughout the array as uniformly as possible
- Reduces sensitivity to higher order (nonlinear) gradients
 - One dimensional examples
 - ABBAABBA: 3 repetitions
 - ABABBABA: 1 repetition
 - Has higher dispersion (preferable)
- Compactness
 - Make array as compact as possible and approximately square
 - 2D patterns achieve best symmetry
 - X symmetry comes from inter-digitation, and does rely on unit device symmetry
 - Example patters

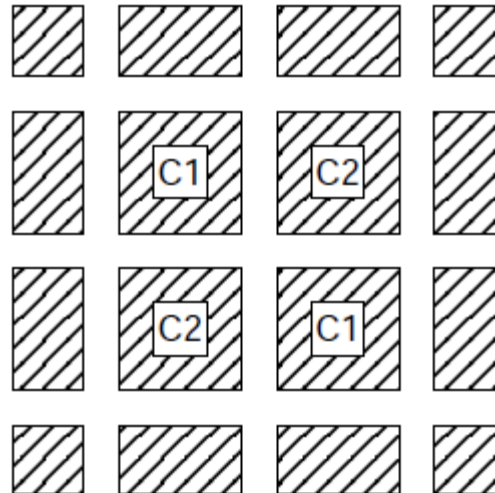
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Matching Dummies

- Need to add dummy components on the edge of the array in order to match all boundaries of all units of C1 and C2 → Better matching.



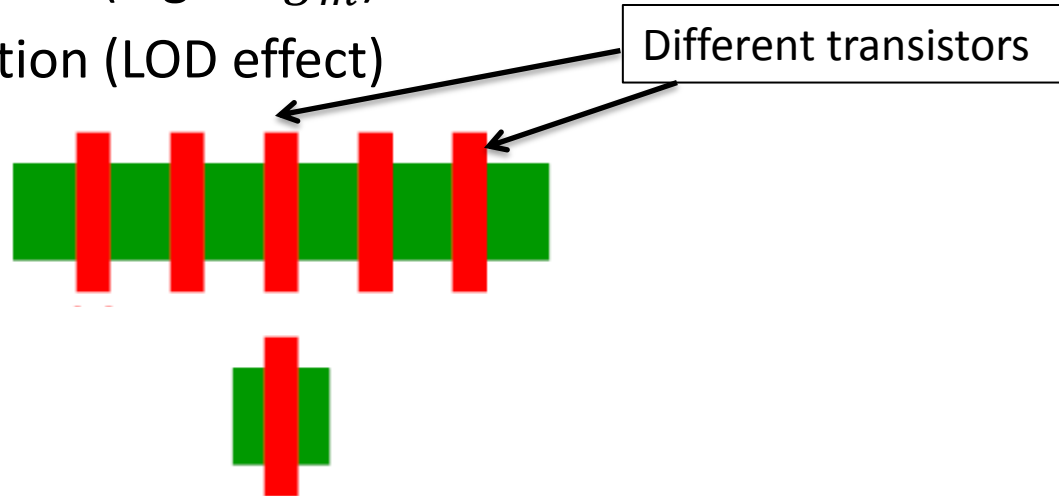
- Same for resistors. We need to add dummies on all sides.
- Watch out for capacitor mismatch due to routing imbalance.

MOS transistors

- Sources of layout proximity effect
 - Well proximity effect
 - Unintentional stressors: Shallow trench isolation (LOD effect)
- Well proximity:
 - $|V_T|$ increases if FET is too close to resist edge due to dopant ions scattering off resist sidewall into active area during well implants
 - $|\Delta V_T|$ (threshold voltage offset) depends on:
 - FET channel distance to well mask edge
 - Implanted ion species/energy
 - $\mu \downarrow, L_{eff} \uparrow, R_{extension} \uparrow \Rightarrow I_{dsat} \downarrow$
- Well mask symmetry now critical for MOSFET matching
- Place transistors as far as possible from the WELL edge, or add “dummy fingers” (Next slide).

Matching MOS transistors

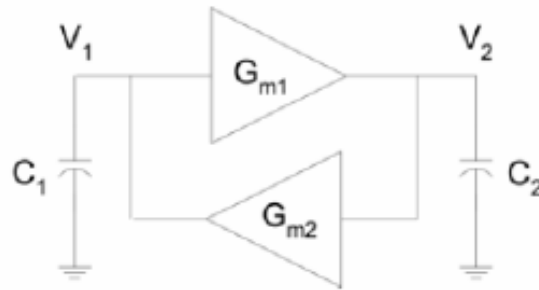
- On the same OD, if all transistor fingers are biased the same (same V_{GS}), they are all expected to create the same current → What happens in sub-micron technologies is that they will not. Fingers in the middle are different (higher g_m) than those on the sides.
- Shallow trench isolation (LOD effect)



- Need to add dummy fingers on the same OD on both ends.
- Dummy fingers are not connected to real transistors but are just placed in the layout to improve matching, LOD effects ... etc.

Routing Imbalance

- A common problem in sensitive differential balance is the imbalance between capacitance on both sides → Causing dynamic offset.
- Regenerative latch



- $C_1 \neq C_2$ causes dynamic offset

Basic Rules

- Use the same W, L, # of fingers and dummies and use M unit devices to generate current ratios (takes out ΔW and ΔL effects)
- Use number of fingers that are even, preferably factors of 4.
- Use common-centroid, or nearly common-centroid, layout (takes about systematic gradients, e.g. oxide thickness and doping)
- Use dummy devices at the edges of the array (takes out etch loading effects)
- Keep matched devices away from power sources (>50mW)
- Ensure clean and well balanced routing
 - Avoid having contacts/vias or irregular metal routing patterns over matching sensitive devices
- Route currents to bridge long distances, not voltages - IR drops can cause big systematic mismatches

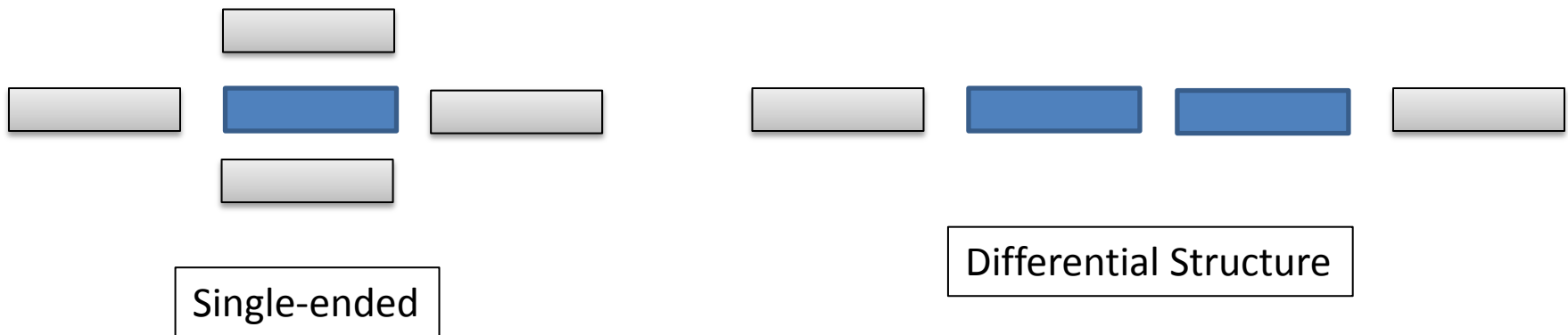
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- Guard Rings can be built by: N+, P+ or N-WELL
- In most modern CMOS technologies, the substrate has a low resistivity. As a result, the distance between analog and digital blocks has little effect on the amount of coupled noise.
- Distance and guard rings can help reduce coupling significantly (in case of high-resistivity substrate)
- Must connect guard rings to quiet, dedicated potentials
 - Otherwise they may inject noise from this noisy guard ring!
- Isolation and coupling effects are highly layout dependent
 - If substrate coupling is critical, the designer should invest a good amount of time to think about potential issues and

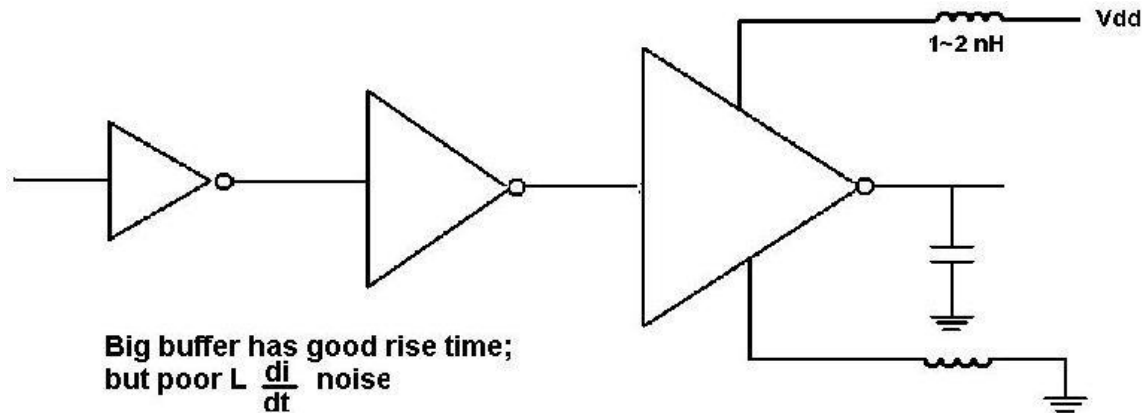
Shielding

- Can attenuate capacitive coupling by shielding sensitive signals with traces running along their side, or underneath
 - Usually creates additional capacitive load!



- For differential signals, it is often sufficient to route the traces close to each other and make sure that any coupling will appear as a common mode signal
- Obvious guideline
 - Keep digital signals away from sensitive analog nodes
- In SC circuits, most sensitive nodes to watch out for are charge conservation nodes (e.g. op-amp inputs)
 - Any moving node that couples in via parasitic cap will modulate charge and therefore inject noise...

Output Buffers (mainly for digital signals)

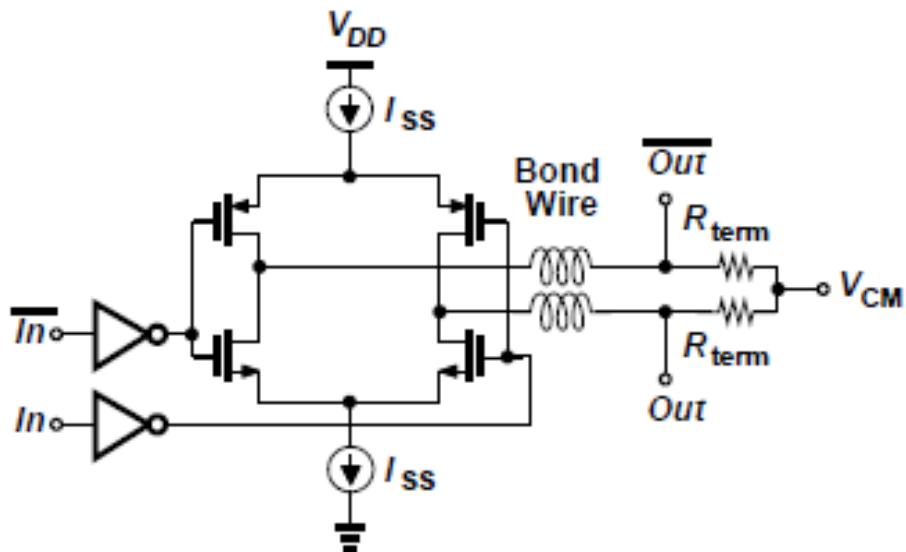
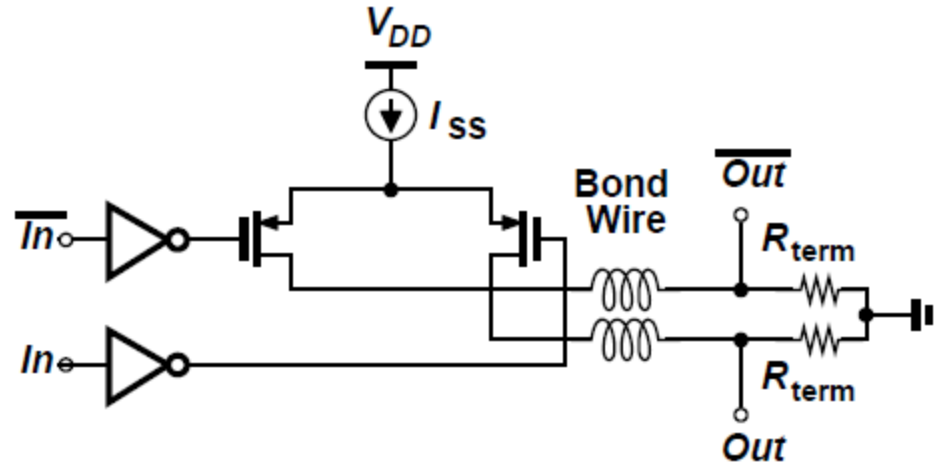


Big buffer has good rise time;
but poor $L \frac{di}{dt}$ noise

Need to simulate with bond wire inductance to Vdd

- Don't make the driver too large!
- If possible, make the driver differential.
- If possible, reduce the output swing.

Output Buffers-Examples



LVDS outputs

Outline

- Basic Issues
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- **Floorplanning**

Floorplanning

- A common mistake is to do a great job of laying out lots of little cells but then make a big mess when pulling the design together.
- A good floorplan is essential to being able to quickly make a good layout with few iterations.
- A floorplan is an evolving document that helps the designer organize the chip into pieces that fit together well
 - Don't be afraid to change it as you go along and discover new issues, just start out with one so you don't miss the obvious things that can be very painful later.
- When generating a floorplan, keep the ultimate test setup in mind
 - If you have to cross sensitive and noisy signals, it's best to do it on chip where you only get a few femto Farads of coupling rather than doing it on the board where you will get much more coupling.

Floorplanning

- Bond wire and package traces have inductance and resistance.
- By putting multiple pins in parallel, you can reduce these parasitics.
 - Unfortunately, mutual inductance of neighboring pins fights the reduction. The inductance of two adjacent pins is about 0.7 times that of one, and for three pins, you get about 0.5 times the inductance of one pin.
- Final bit of advice: Know when to stop! You can easily get so carried away with these issues that your layout takes a very long time to complete
 - The key is to do what is right for an application
 - An RF mixer should minimize capacitance
 - A 14-bit A/D converter needs well a very balanced layout
 - Use your own judgment and ask critical questions!
 - Layout is a mix of art, experience and science.

ADC Floorplan

